TLK2521 2.5Gbps Backplane Transceiver Evaluation Board (EMV)

Thomas Neu High Performance Analog

ABSTRACT

This application report focuses on the use and construction of the TLK2521 evaluation module (EVM). This document provides guidance on proper use by showing possible device configurations and test modes. It also provides design, layout, and schematic information, including specific construction recommendations. Information in this guide can be used to assist the customer in choosing the optimal design methods and materials in designing a complete system.

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Introduction

The Texas Instruments (TI) TLK2521 evaluation module (EVM) board is used to evaluate the TLK2521 SERDES device. The evaluation board can be used for evaluation and testing. It can be used as a reference for high-speed design and routing.

The evaluation board enables the designer to connect a LVTTL bus and provide parallel data to the device that can be serialized and transmitted across a differential pair at speeds up to 2.5Gbps. The serial channel provides an effective payload of up to 2.25Gbps (2.5Gbps with start/stop bit)

TLK2521 EVM Board Configuration

TLK2521 Evaluation Kit Contents

1. TLK2521 Evaluation Board
2. TLK2521 Evaluation Board Documentation (this document)

Description

The TLK2521 evaluation board gives the developer various options for operation, which are jumper selectable. See the TLK2521 datasheet for recommended operating conditions. The board is pictured in Figure 1.

The evaluation board requires only one single power supply. It is powered through two banana jacks, *VDD* and *GND,* and operates at nominal 2.5 Vdc.

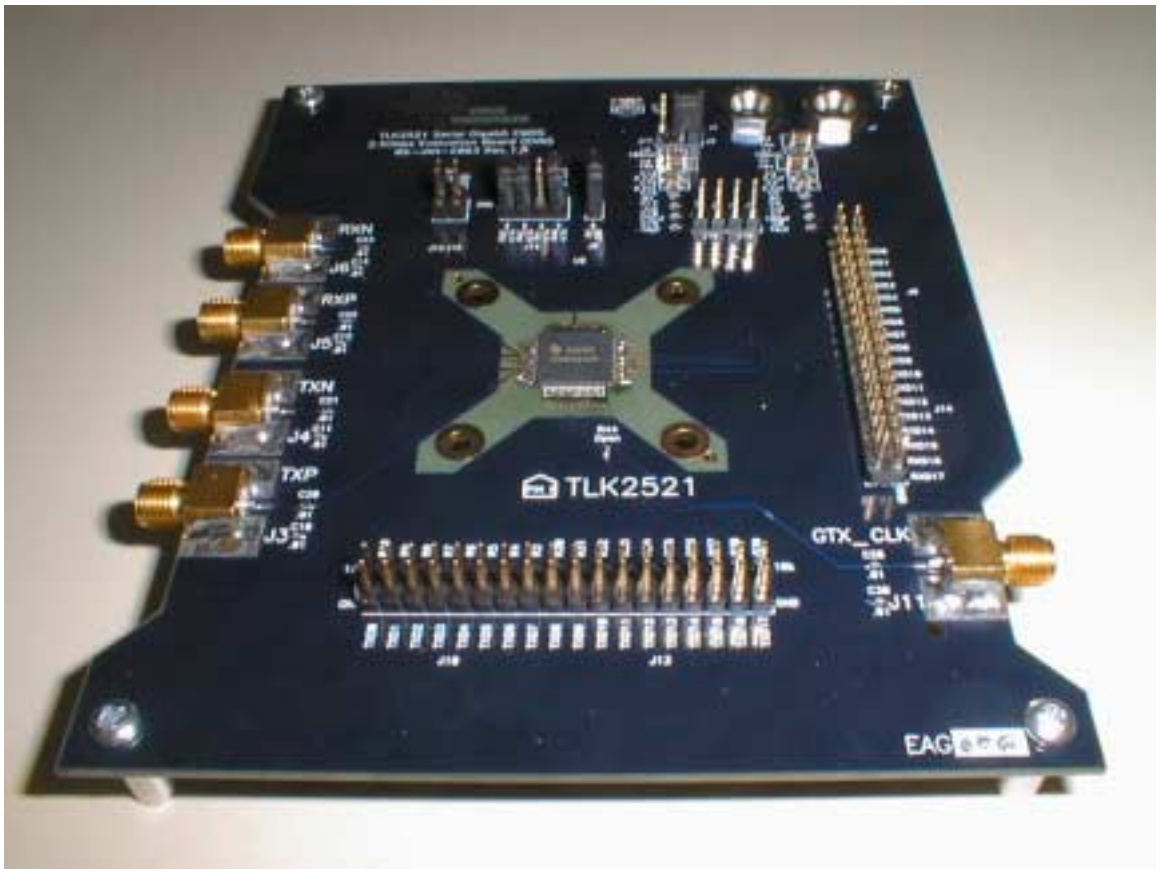
The parallel interface of TX and RX consists of 18 LVTTL data signals together with the synchronous transmit clock GTX_CLK. The LVTTL transmit (reference) clock is supplied through a SMA connector labeled *GTX_CLK*.

Headers are provided for the parallel transmit and receive channel. The TXD header has a pull-up resistor connected to each signal pin. Additionally the RXD and TXD header contain signal pins adjacent to ground pins to provide a reference for measurements (RX) but also to enable the user to setup a data pattern (TX). Furthermore, the RXD signals may be looped back to the TXD header using a coax cable assembly or the loopback board. When using cable assemblies care must be taken to ensure that the cable lengths are correctly matched to prevent cable skew.

The high-speed serial data stream is transmitted and received through four SMA connectors labeled TXP, TXN, RXP and RXN. These PECL-compatible differential signals, called VML signals, are transmitted through single ended coaxial cable for either data loopback, connection with another EVM board or test equipment. Since the TX signals are ac coupled, a direct or attenuated connection to an oscilloscope is possible resulting in a voltage swing around zero. Additionally, the serial receiver is also ac coupled and internally biased to provide the correct common mode dc level regardless of the input dc level. This also provides an easy connection to either test equipment or optical transceivers.

The LVTTL reference clock (GTX_CLK) is connected through a SMA connector labeled GTX_CLK. The clock signal is externally dc coupled to the device.

Figure 1. TLK2521 Evaluation Board



Default Configuration

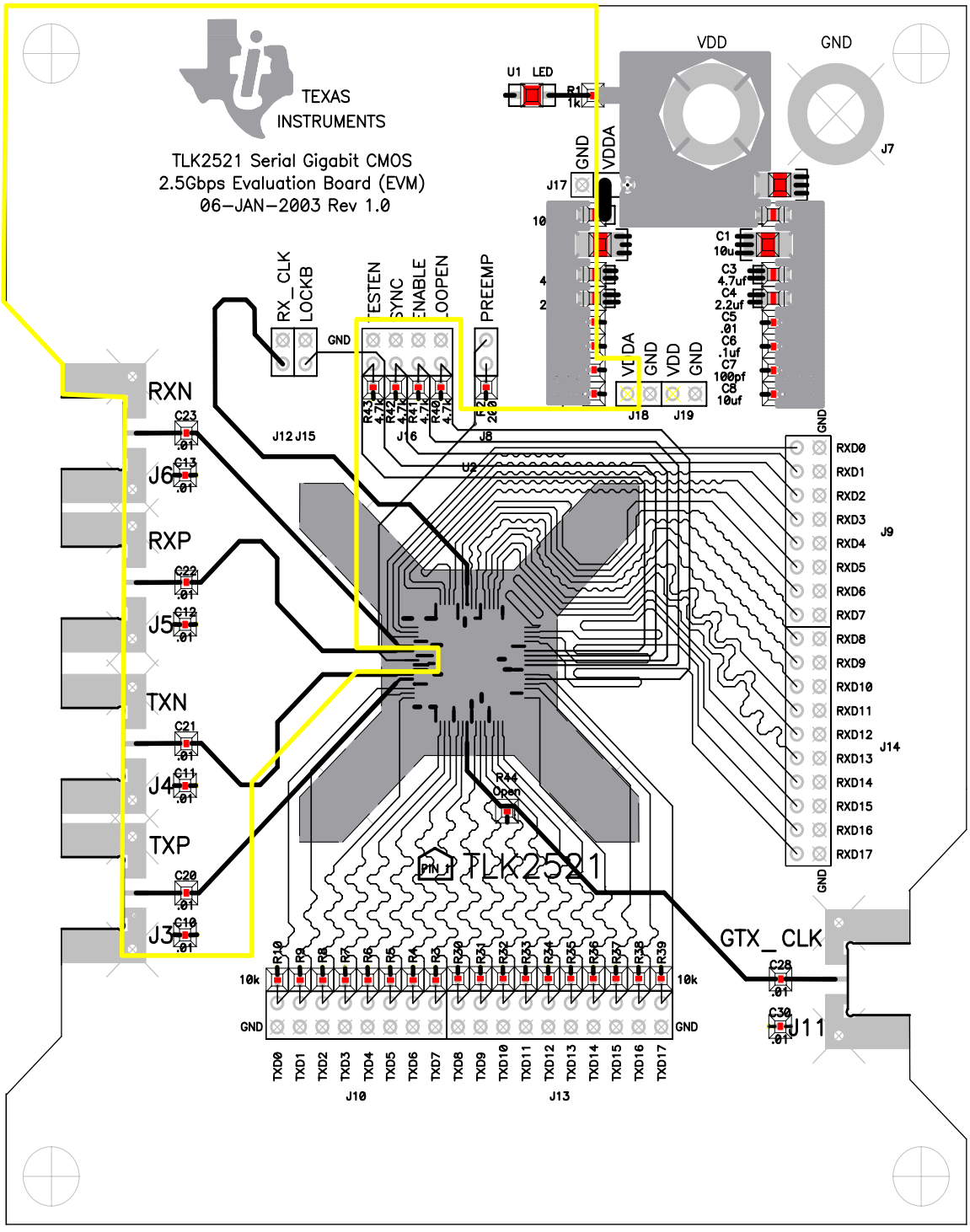
The TLK2521 is shipped with the default transceiver configuration shown in Table 1. This default setup puts the device in full duplex transceiver mode. In this mode data can be transmitted from board to board or externally looped back.

Designator	Function	Condition
J16	TESTEN	Jumper installed (logic 0) - Test mode enable Disables the TLK2521 test mode. This is for production testing only.
J16	SYNC	Jumper installed (logic 0) – Fast synchronization Disables the fast synchronization mode. When high, the transmitter will substitute the 18 bit pattern with 111111111000000000 so that when the start/stop bit are framed around the data the receiver can immediately detect the proper deserialization boundary. This is typically used during initialization of the serial link.
J16	ENABLE	Jumper not installed (logic 1) – Device Enable Enables the TLK2521 for normal operation.
J16	LOOPEN	Jumper installed (logic 0) - Internal Loop Enable Disables the parallel internal bop back mode. When high, the parallel transmit data are directly routed internally to the RXD outputs.
J8	PREEMP	Jumper installed (logic 1) – Preemphasis enable Enables preemphasis on the serial TX outputs.

Note: For details, see TLK2521 Datasheet

Table 1: Default EVM board Configuration

Figure 2: Board Layout Description

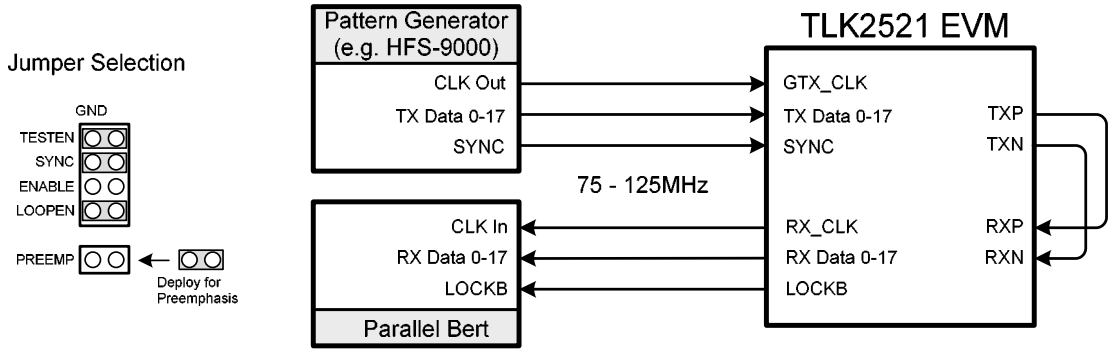


Test and Setup Configurations

The following configurations are used to evaluate and test the TLK2521 transceiver.

The first configuration is a serial loopback of the high-speed signals as shown in Figure 3 below. The serial loopback allows the designer to evaluate most of the functions of both transmitter and receiver sections of the TLK2521 device. To test a system, a pattern generator provides a predefined parallel bit pattern to the TLK2521 device through the parallel connectors TD0-TD17.
Additionally, the synchronization pin SYNC is controlled by the pattern generator to initialize a fast synchronization. The TLK2521 device encodes (adding start/stop bit), serializes and presents the data on the high-speed serial pair. The serial TX data is then looped back to the receiver side and the device deserializes, decodes and presents the data on the receive side RD0-RD17. The data and synchronization indication (LOCKB) are received by the BERT, compared against the transmitted pattern and monitored for valid data and errors. If any bit errors are received, a bit error rate is evaluated at the parallel receive BERT.

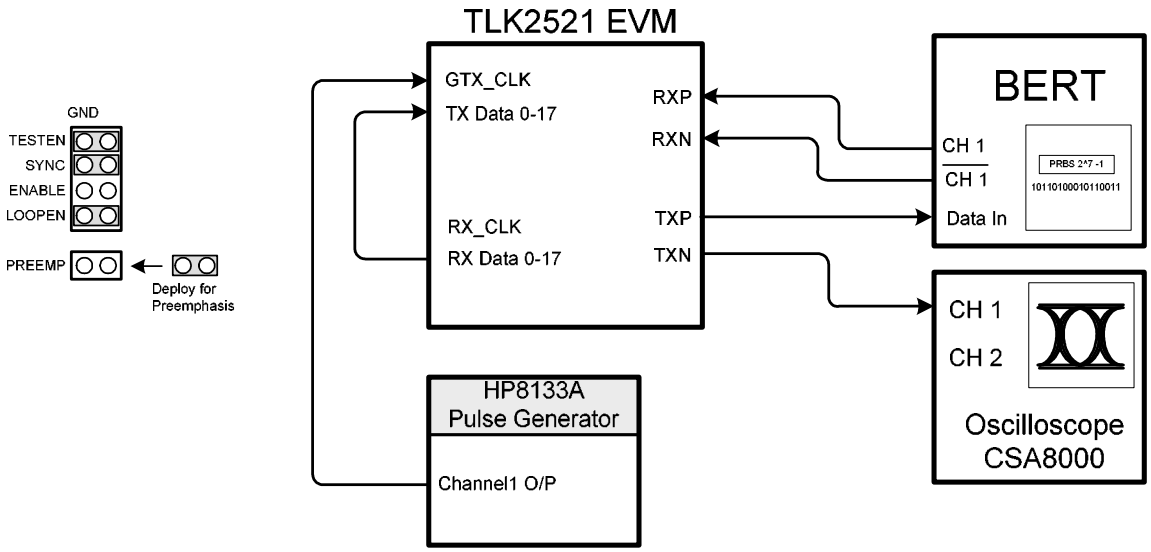
Figure 3: TLK2521 Serial Loop-back Test Configuration



The TLK2521 can also be tested with a BERT. However, the 01 start/stop bits need to be inserted in the serial data stream so that the TLK2521 can recover the byte boundaries correctly. The parallel output data can be looped back to the parallel inputs using the loopback board or cables but the parallel RX data could also be verified with e.g. a logic analyzer.

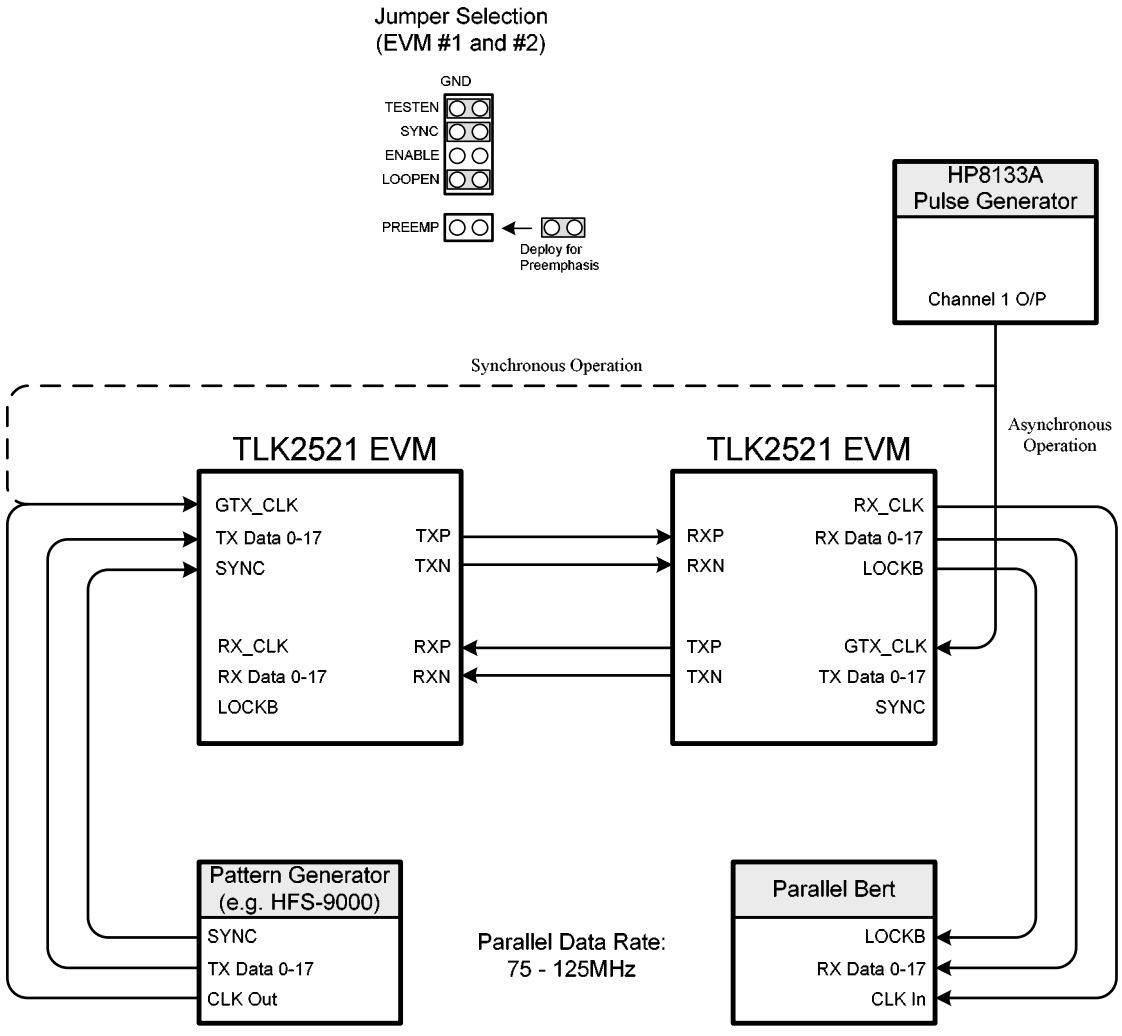
The parallel loopback works only in synchronous operation, RX data must have the same frequency as the GTX_CLK and the phase of the GTX_CLK needs to be adjusted to accommodate the setup/hold times of the TLK2521.

Figure 4: TLK2521 Parallel Loop-back Test Configuration



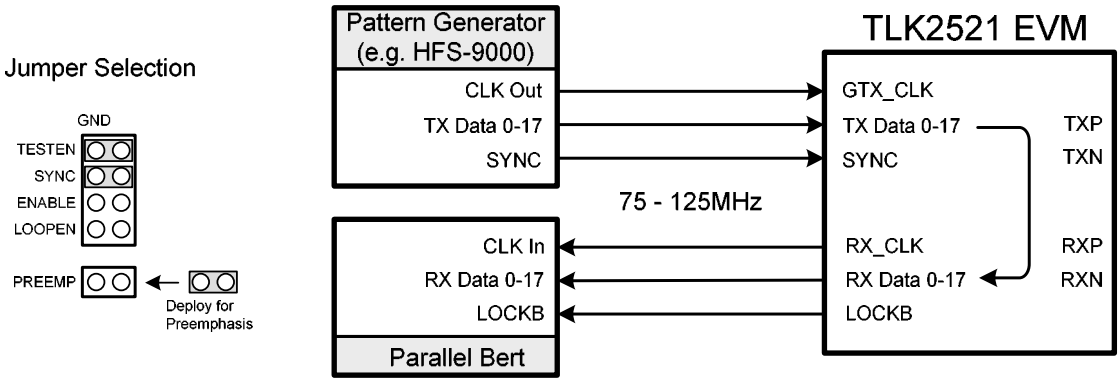
A board to board communication link is a practical method of evaluating the TLK2521 in a system like environment as shown in Figure 3. A pattern generator can be used to provide the data to the TLK2521 transceiver. The output data of the second TLK2521 can be validated with a parallel BERT or a logic analyzer. The pattern generator needs to configure the SYNC signal for data transmission before any data is sent. On the receive side, the LOCKB indicates if the receiver of the TLK2521 has acquired bit synchronization. The GTX_CLK for both TLK devices must have the same frequency within 200 PPM for asynchronous operation. Synchronous operation can be achieved by using either the pattern generator clock or a synchronized pulse generator to supply GTX_CLK to both boards.

Figure 5: Board to Board Test with two TLK2521 EVMs



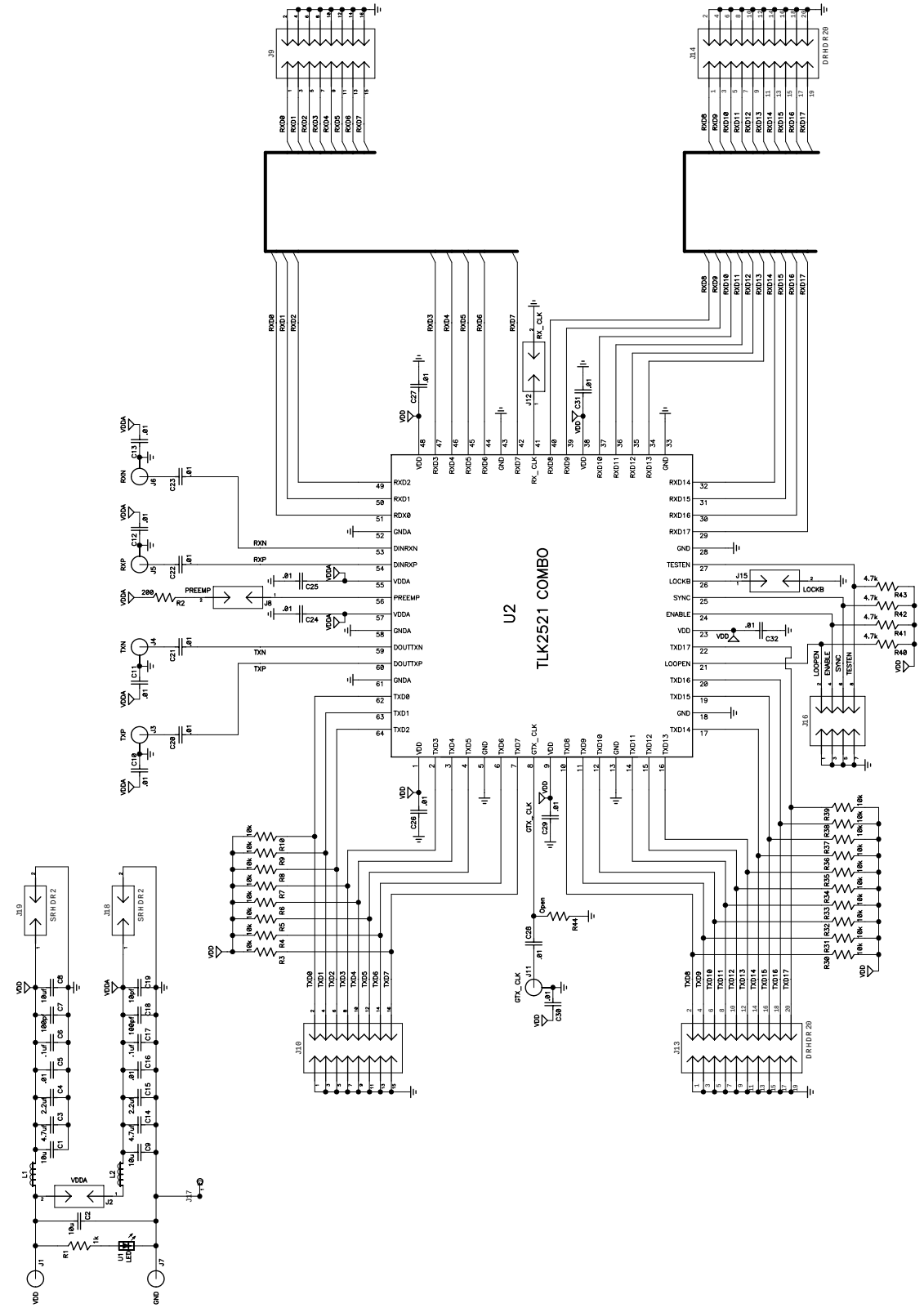
The TLK2521 can be tested without exercising the serial side. In the internal loopback mode (Loopen), parallel TX data stream is routed internally to the parallel RX data output bus. This enables the designer to verify the parallel data bus in a system environment where no serial loopback is available.

Figure 6: TLK2521 Parallel internal Loop-back Test Configuration



PCB Construction and Characteristics

Figure 7: Schematic



Material Listing

Table 2. TLK2521 Evaluation Board Materials Listing

Item	Count	ComponentName	RefDes	Value	PartNumber	Vendor	ManufacturerPart#	Manufacture
1	2	BJACK_PLATED	J1,J7		J147-ND	DigiKey	108-0740-001	Johnson Components
2	18	CAP0402	C5,C10-13,C16,C20-26,C28-32	0.01u	PCC1738CT-ND	DigiKey	ECJ-0EF1E103Z	Panasonic
3	2	CAP0402	C6,C17	0.1u	PCC1731CT-ND	DigiKey	ECJ-0EF1C104Z	Panasonic
4	1	CAP0402	C8	10u				
5	1	CAP0402	C19	10p	PCC100CQCT-ND	DigiKey	ECJ-0EC1H100D	Panasonic
6	2	CAP0402	C7,C18	100p	PCC101CQCT-ND	DigiKey	ECJ-OEC1H101J	Panasonic
7	1	CAP0603	C27	.01u				
8	2	CAP0805	C4,C15	2.2u				
9	2	CAP0805	C3,C14	4.7u	PCC1842CT-ND	DigiKey	ECJ-2YF1A475Z	Panasonic
10	3	CAP1206	C1,C2,C9	10u		DigiKey		Panasonic
11	1	DRHDR8	J16		S2011-04-ND	DigiKey	PZC04DAAN	Sullins Electronics
12	2	DRHDR16	J9,J10		S2011-08-ND	DigiKey	PZC08DAAN	Sullins Electronics
13	2	DRHDR20	J13,J14		S2011-10-ND	DigiKey	PZC10DAAN	Sullins Electronics
14	2	F-BEAD 0805	L1,L2		240-1018-1-ND	DigiKey	HIZ0805E601R-00	Steward
15	5	SMA END-LAUNCH	J3-6,J11		142-0721-881	Avnet	142-0721-881	Johnson Components
16	1	RES0402	R1,R8,R50,R57,R99,R106,R148,R155	1K	P1.0KLCT-ND	DigiKey	ERJ-2RKF1001X	Panasonic
17	4	RES0402	R40-43	4.7K	P4.7KJCT-ND	DigiKey	ERJ-2GEJ4751X	Panasonic
18	18	RES0402	R3-10,R30-39	10K	P10.0KLCT-ND	DigiKey	ERJ-2RKF1002X	Panasonic
19	1	RES0402	R2	200	P200LCT-ND	DigiKey	ERJ-2RKF2000X	Panasonic
20	1	RES0402	R44	OPEN				
21	1	TLK2521	U1		TLK2521	TI	TLK2521	Texas Instruments
22	1	SRHDR1	J17		S2105-02-ND	DigiKey	PRPN021PAEN	Sullins Electronics
23	7	SRHDR2	J2,J8,J12,J15,J18,J19		S2105-02-ND	DigiKey	PRPN021PAEN	Sullins Electronics
24	1	CMD28-21	U1		L62711CT-ND	DigiKey	CMD28-21SRC/TR8/T1	Chicago Miniature Lamp, Inc.

Miscellaneous

25	4	STANDOFF			4830K-ND	DigiKey	4830	Keystone Electronics
26	4	Machine Screw			H146-ND	DigiKey	PMS 440 0050 SL	Building Fasteners
27	8	Shorting Jumper Configuration	J8, J12, J15, J16 1-2, J16 3-4, J16 5-6, J16 7-8, J17		S9002-ND	DigiKey	SSC029YAN	Sullins Electronics Corp

Board Construction

The TLK2521 EVM board was designed specifically to optimize high-speed signal performance. Power supply noise reduction can have a primary impact on device performance. The sensitive VDDA power supply, which drives the high-speed I/O, is separated and filtered from the VDD section. To provide high frequency decoupling for each power plane, every power plane maximizes its area adjacent to a ground layer with minimal spacing. Power planes are used to create low inductance paths for the TLK2521's current needs. No GND and analog GND separation is used on the EVM board.

Eliminating deviations from 50Ω in the serial line path also impacts signal integrity. The SMA connections use end launch SMA's with manually shortened posts. These provide structural rigidity for connections while minimizing impedance discontinuities.

The Impedance of the microstrip line is affected by the line width and separation from the reference plane. The microstrip line widths of the high-speed serial lines have been matched to the SMA post's width. Additionally the lengths of all the serial lines as well as all parallel TX and parallel RX lines were matched to ± 1mil.

Blocking caps can be used in series in the serial lines if a DC-balanced data stream is sent. Otherwise the capacitors will completely charge or discharge and data transmission is not possible. Therefore 0Ω Resistors are installed instead but the option for AC-coupling is available. The resistor/cap pads on the serial lines introduce a degree of discontinuity, but the mismatch is generally less than 10%. Carefully matching the resistor/cap pads and dimensions to the microstrip line width helps to minimize the discontinuity.

In order to optimize the performance of the TLK2521, the path of the GTX_CLK was optimized. Signal reflections were minimized using end launch SMA connectors. Vias were avoided completely by using only microstrip traces on the top layer.

The EVM board uses loosely coupled 0.020" microstrip lines for the high-speed signal propagation. Either microstrip or stripline are suitable, although routing and line width transitions must be considered. The reference planes do not contain any breaks or gaps over the high-speed lines.

Figure 8. Board Layer Stack-up

6 Layer FR4 Polyclad
Overall thickness to be 0.063 ± 0.005 Thick
1oz Cu starts on Inner layers
H oz Cu. starts on Outer layers

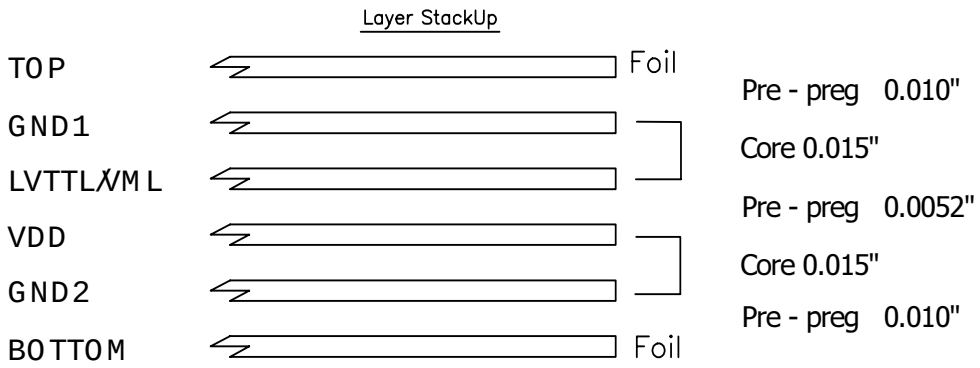


Figure 9. Board Construction Top Layer

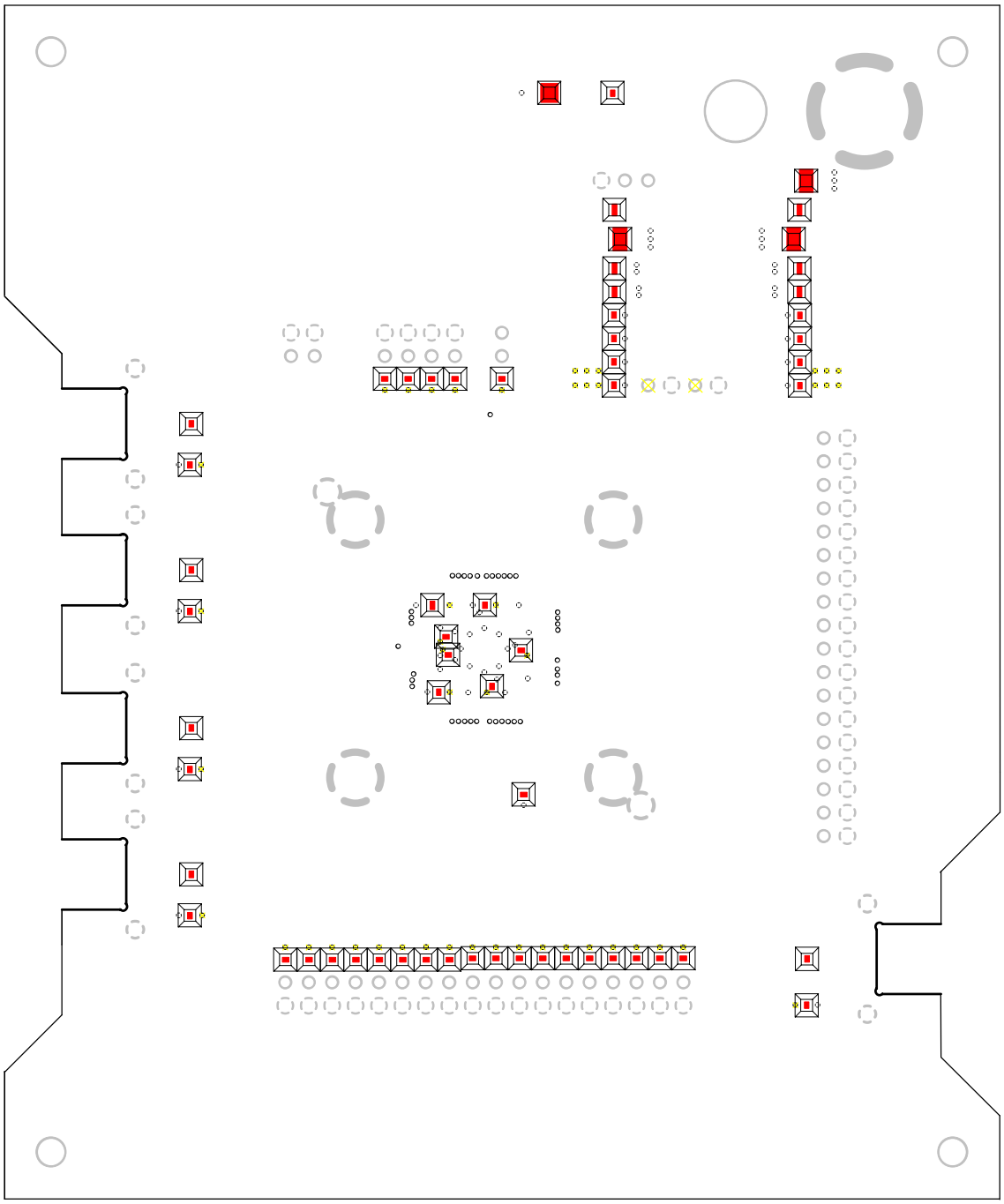


Figure 10. Board Construction GND Layer 1 and 2

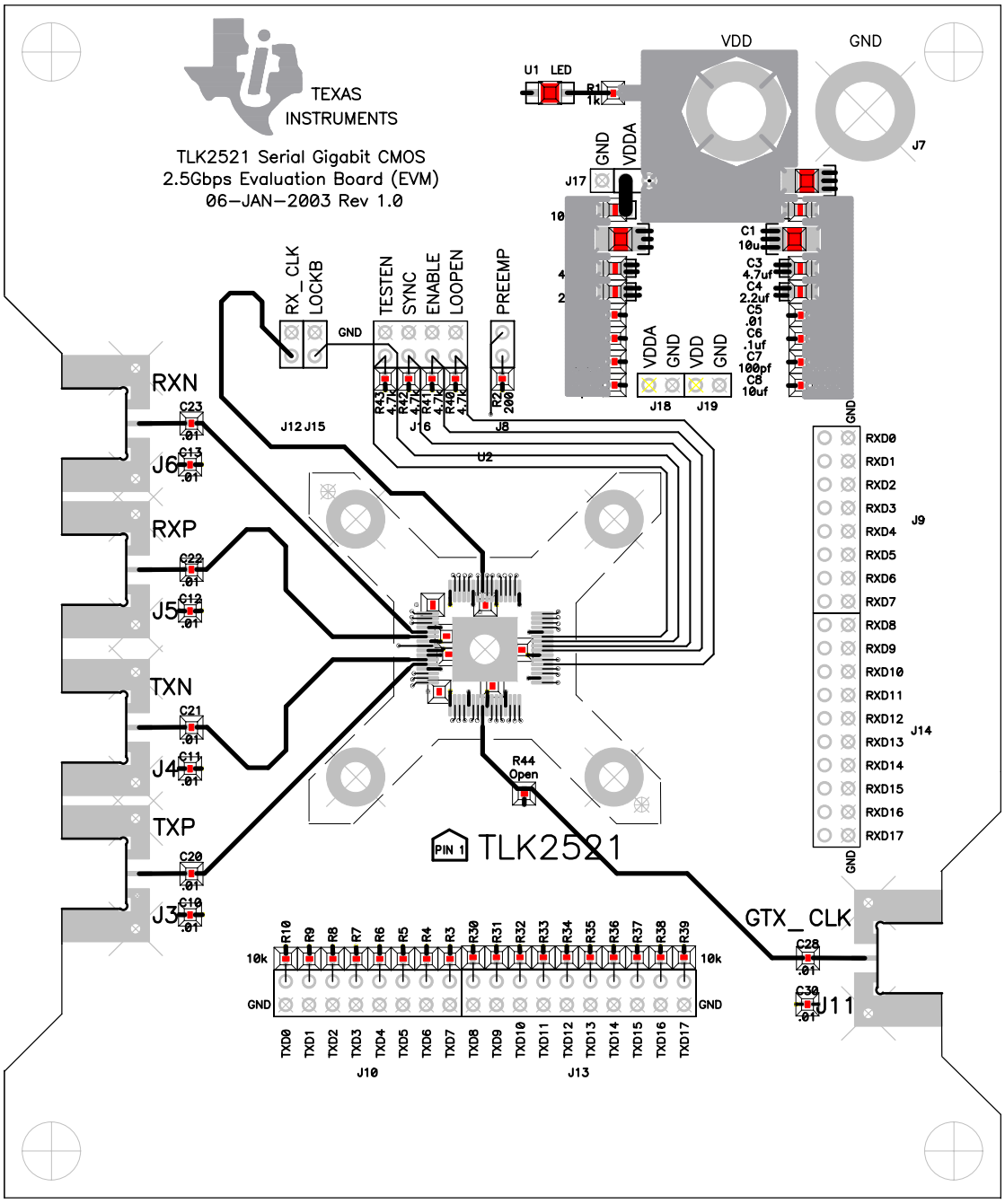


Figure 11. Board Construction LVTTL/VML layer

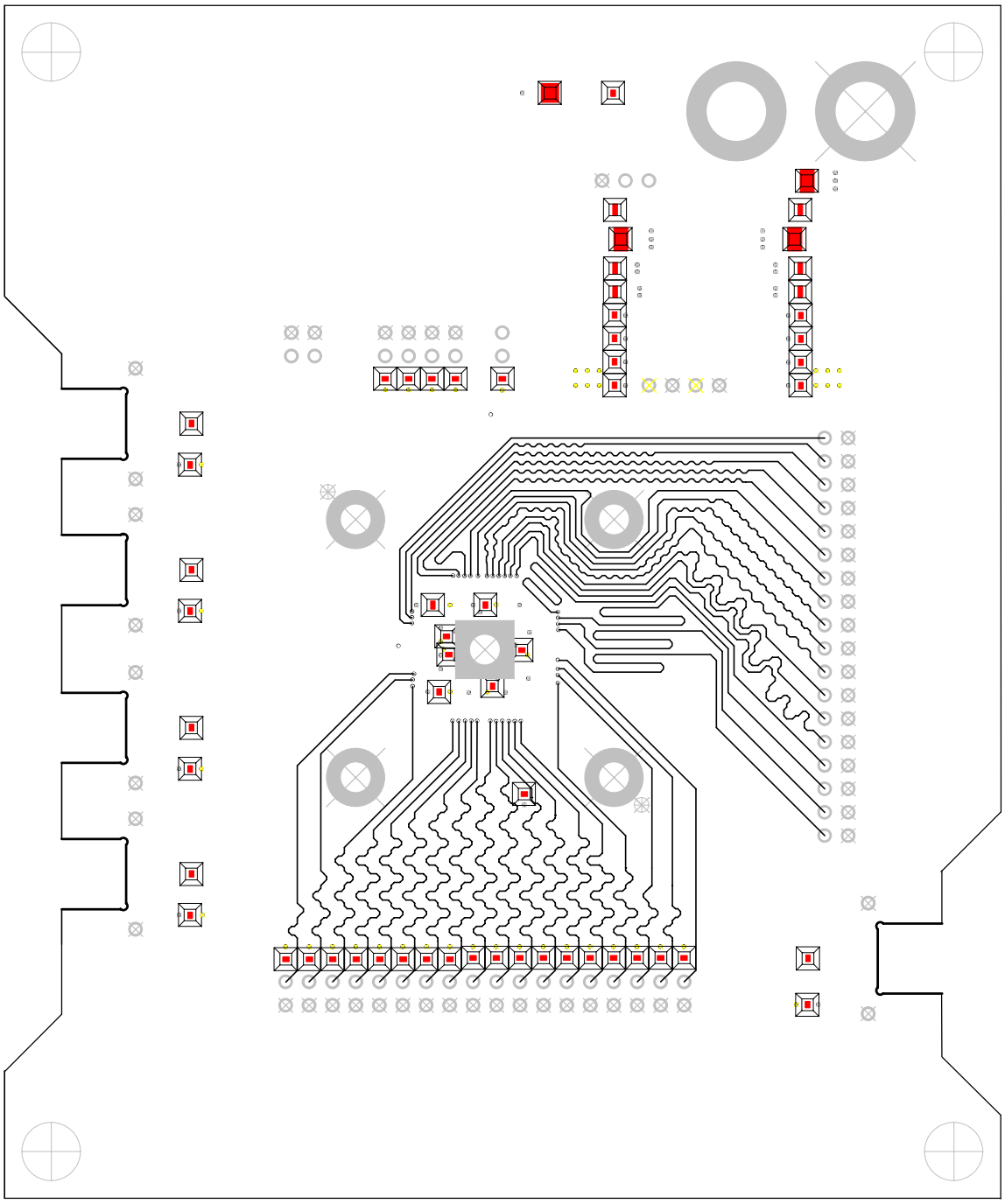


Figure 12. Board Construction VDD Layer

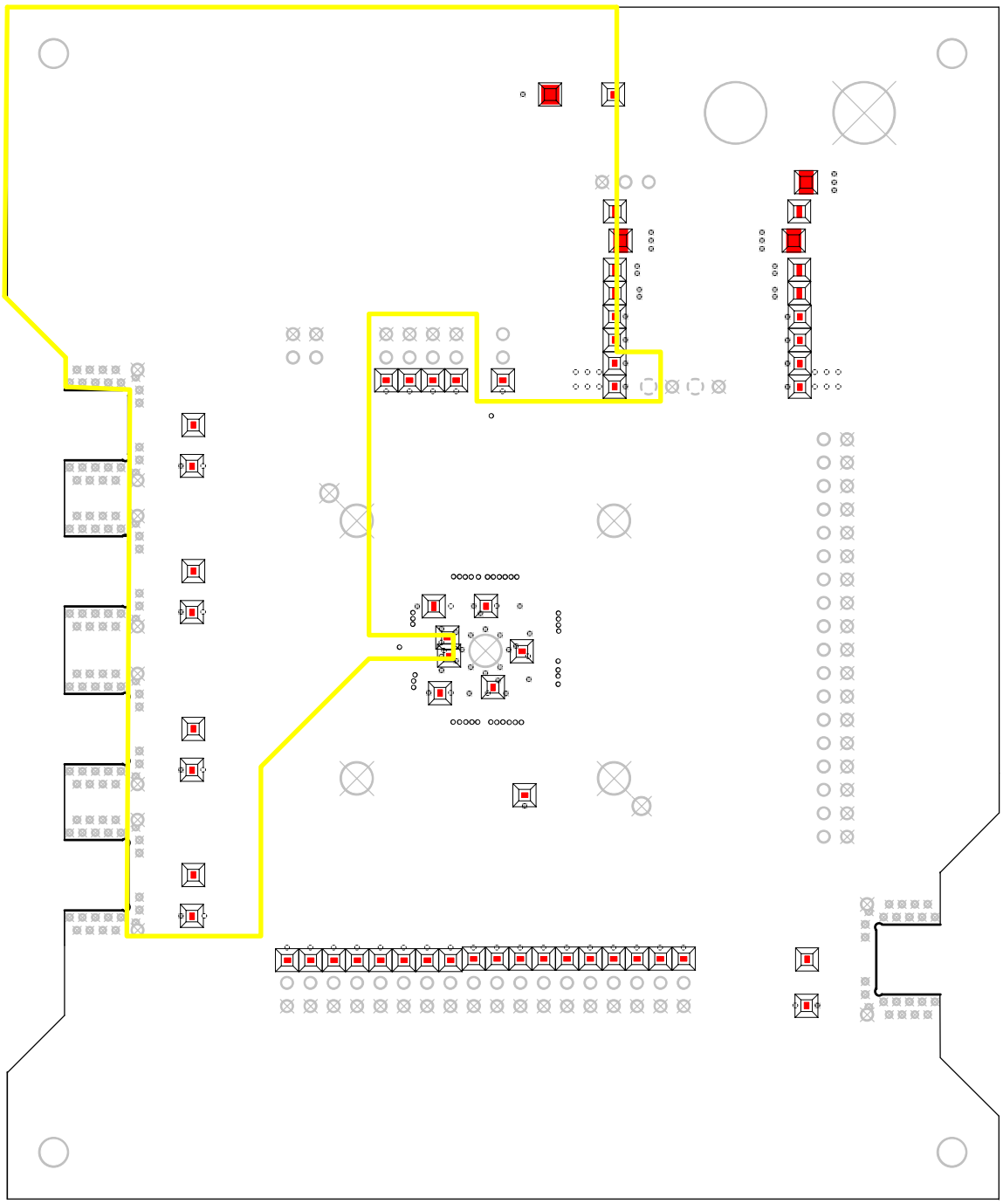


Figure 13. Board Construction Bottom Layer