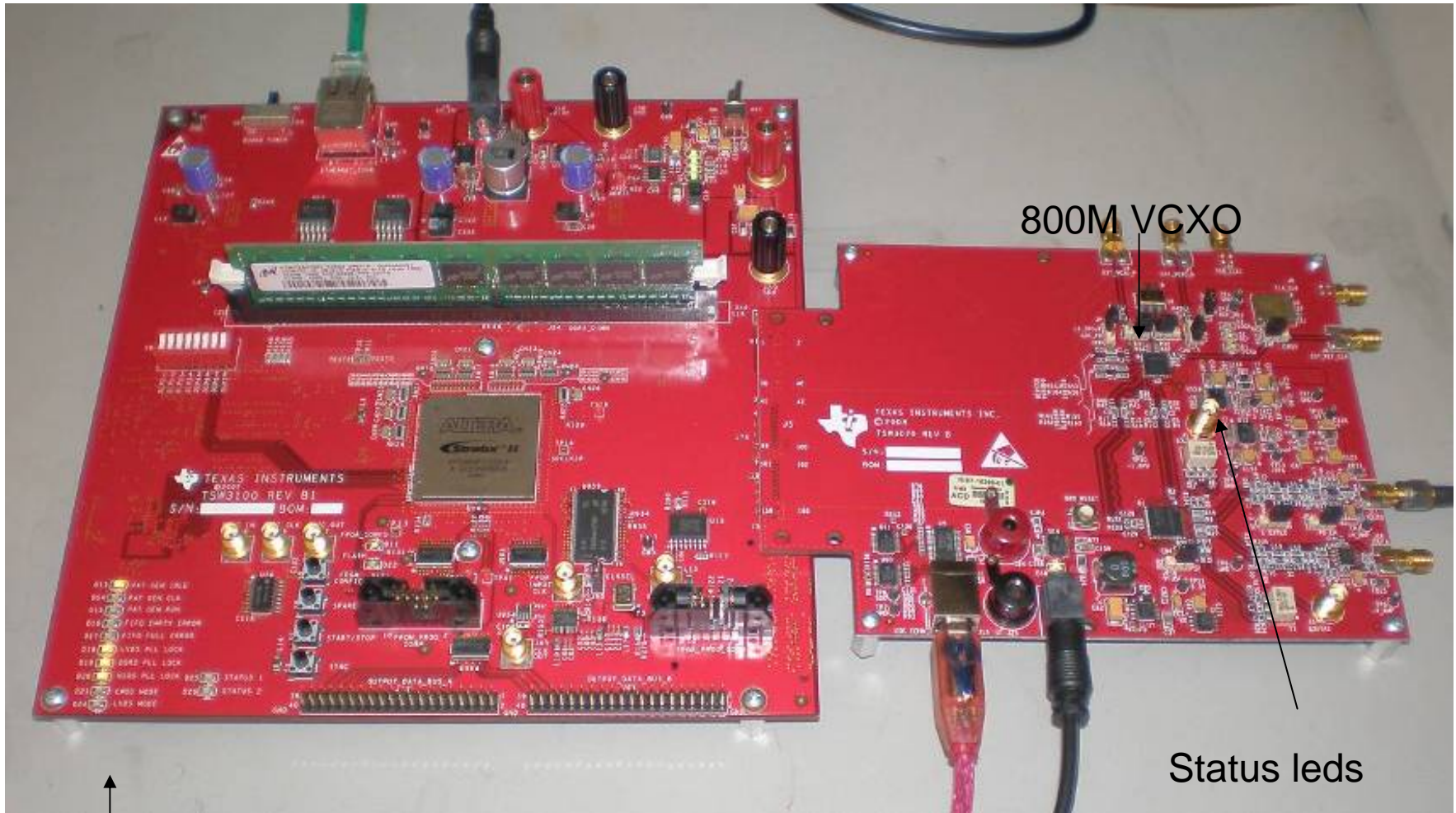


# TSW3070 Setup Procedure

- Connect TSW3100 and TSW3070 as shown.
- Start up the DAC5682 GUI and TSW3100 Tone GUI

# Default power up status

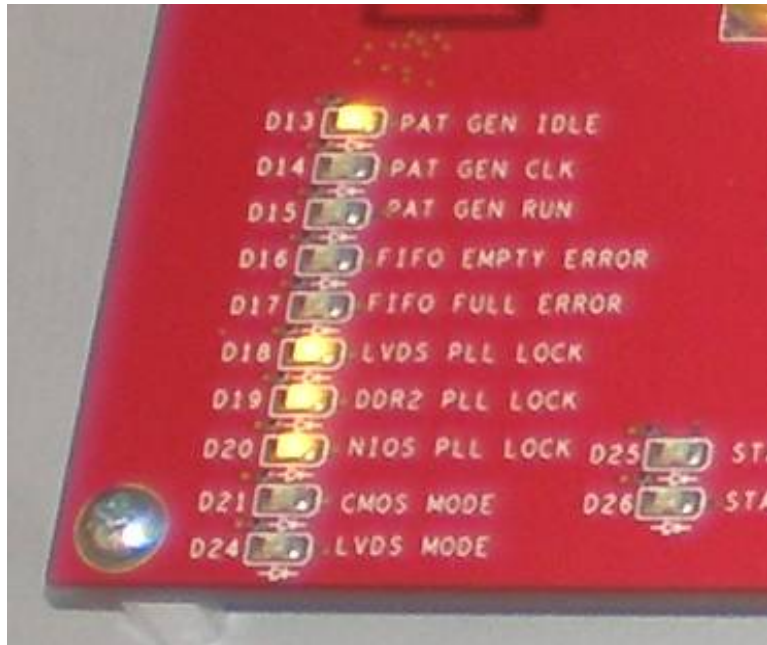


Status leds

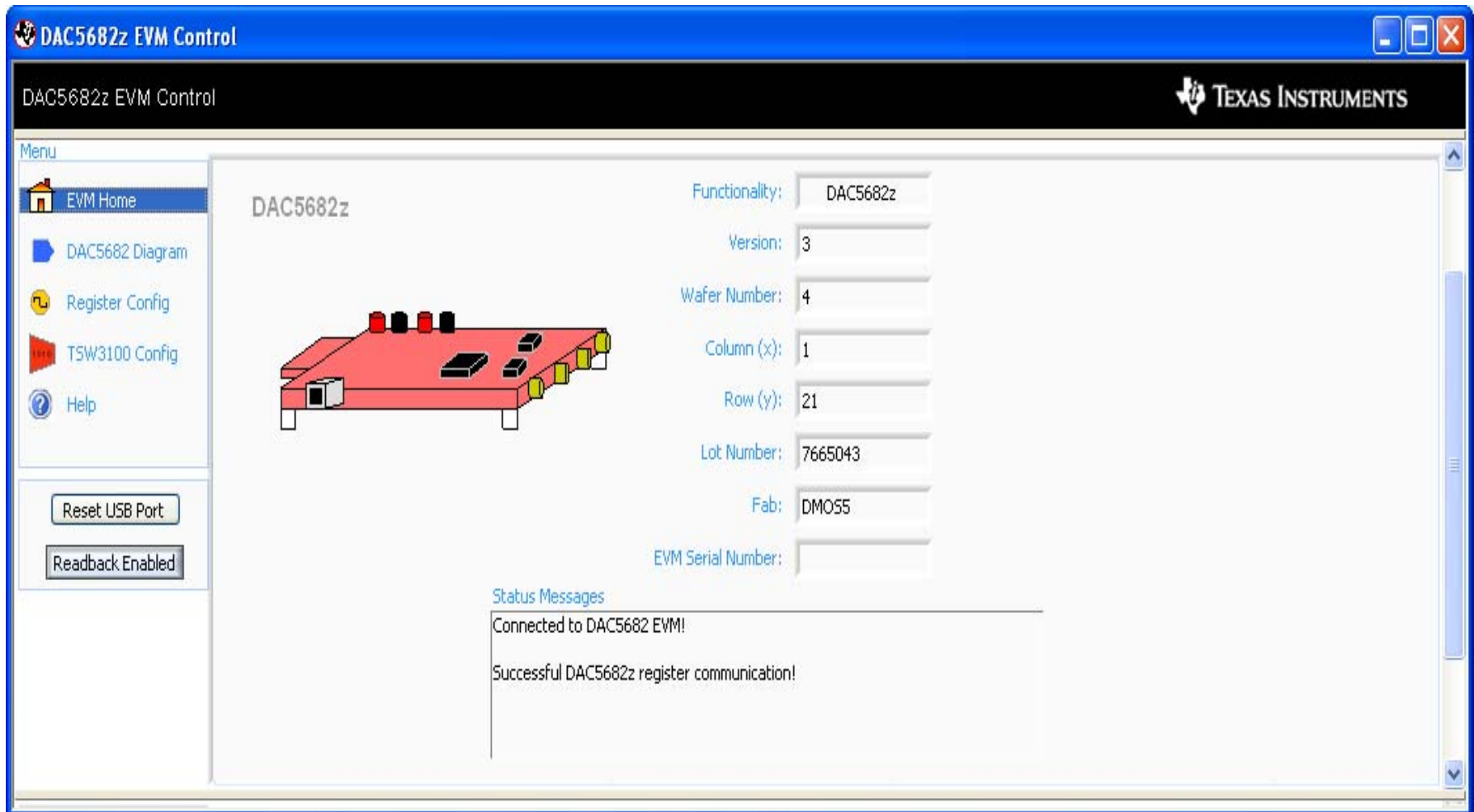
800M VGXO

Status leds

# Default TSW3100+TSW3070 LEDs



# Default GUI settings



The screenshot displays the 'DAC5682z EVM Control' software interface. The window title bar reads 'DAC5682z EVM Control' and features the Texas Instruments logo in the top right corner. The main content area is divided into several sections:

- Menu:** A vertical sidebar on the left contains navigation options: 'EVM Home' (selected), 'DAC5682 Diagram', 'Register Config', 'TSW3100 Config', and 'Help'. Below the menu are two buttons: 'Reset USB Port' and 'Readback Enabled'.
- DAC5682z:** A central area showing a 3D perspective view of the red printed circuit board (PCB) with various components.
- Parameters:** A list of configuration fields on the right side:
  - Functionality: DAC5682z
  - Version: 3
  - Wafer Number: 4
  - Column (x): 1
  - Row (y): 21
  - Lot Number: 7665043
  - Fab: DMO55
  - EVM Serial Number: (empty field)
- Status Messages:** A text area at the bottom right displaying two messages:
  - Connected to DAC5682 EVM!
  - Successful DAC5682z register communication!

# Default GUI settings for DAC and CDCM

**DAC5682z EVM Control**

version 3 functionality DAC5682z

**DAC5682z Register Configuration**

PLL enabled  PLL Sleep  PLL Lock  PLL reset

VCO Frequency 1x M value 1  
PLL Gain (MHz/V) 85 N value 1  
PLL Range (MHz) 262 - 485

DLL enabled  DLL Sleep  Auto-DLL  DLL Lock  DLL restart

DLL Delay (deg) 90  
DLL fixed current delay (ps/uA) -3.43  
DLL inv clock normal

Format 2's complement  
reverse bus normal  
swap data disabled  
same data disabled  
FIFO offset 0

digital logic enabled  
interpolation 2x  
CM0 mode Bypass  
CM1 mode Bypass  
digital delay 0 clock delay 0

DAC mode dual DAC  
Offset disabled  
offset sync

DACA Sleep  
 DACB Sleep  
DACA Gain 15  
DACB Gain 15  
Offset A 0  
Offset B 0  
DAC A LPF enabled  
DAC B LPF enabled

SLFST error mask  
FIFO error mask  
Setup/Hold Error mask  
SLFST error reset   
FIFO error reset   
Setup/Hold error reset   
SDO Normal

serial interface 3-pin  
software sync   
sync source hard sync  
hold sync enabled  
clk div sync enabled  
FIFO sync enabled  
ATEST ATEST disabled  
self test disabled  
FA002 disabled  
Fuse A disabled  
Fuse B disabled  
Send All   
Read All   
Load Regs   
Save Regs

**Reg Value Hex**

00	00000011	0x03
01	00010000	0x10
02	11000000	0xC0
03	01110000	0x70
04	00000000	0x00
05	00000000	0x00
06	00001100	0x0C
07	11111111	0xFF
08	00000000	0x00
09	00000000	0x00
0A	00000000	0x00
0B	00000000	0x00
0C	00000000	0x00
0D	00000000	0x00
0E	00000000	0x00
0F	00000000	0x00

**CDCM7005 Register Configuration**

M & N Selection Auto  
Ref. Freq (MHz) 10  
VCO Freq (MHz) 983.04  
M Divider 125  
Output Freq (MHz) 983.04

PLL Settings  
FB\_MUX 1  
Phase Shift /16  
N Divider 1536

**Output Settings**

Y0 Output (Unused)  
Y0 Divider 1 Y0 Level LVPECL 3-state Y0A  
Y1 Output (SMA Outputs)  
Y1 Divider 1 Y1 Level LVPECL 3-state Y1B  
Y2 Output (TSW3100)  
Y2 Divider 8 Y2 Level LVPECL active Y2A  
Y3 Output (DCLK)  
Y3 Divider 1 Y3 Level LVPECL 3-state Y3A  
Y4 Output (DAC5682 CLK)  
Y4 Divider 1 Y4 Level LVPECL active Y4A

**CDCM7005 Operation Buffer Mode**

Send All   
Load Regs   
Save Regs

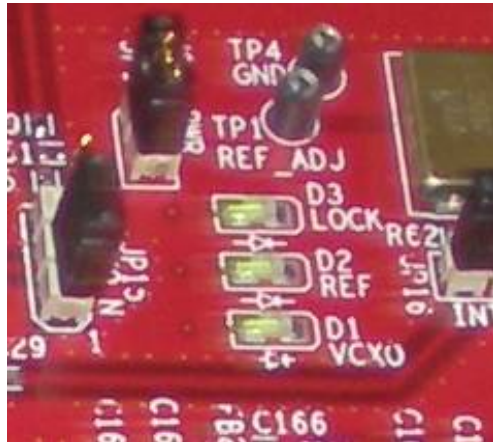
Change GUI settings to match, click SEND ALL for both, once data is loaded into TSW3100 the DLL lock will light up

The screenshot displays the DAC5682z EVM Control software interface, which is used for configuring the DAC5682z and CDCM7005 components. The interface is divided into several sections:

- Menu:** Includes EVM Home, DAC5682 Diagram, Register Config (selected), TSW3100 Config, and Help.
- DAC5682z Register Configuration:**
  - PLL:** PLL is set to 'bypassed'. PLL Lock is indicated by a red light. PLL Sleep is checked.
  - VCO Frequency:** Set to 1x.
  - PLL Gain (MHz/V):** Set to 85.
  - PLL Range (MHz):** Set to 262 - 435.
  - M value:** Set to 1.
  - N value:** Set to 1.
  - DLL:** Enabled. DLL Lock is indicated by a green light. DLL Sleep is unchecked. Auto-DLL is checked. DLL Delay (deg) is 90. DLL fixed current delay (ps/uA) is -3.43. DLL inv clock is 'inverse'.
  - Format:** 2's complement.
  - reverse bus:** normal.
  - swap data:** disabled.
  - same data:** disabled.
  - FIFO offset:** 0.
  - digital logic:** enabled.
  - interpolation:** 4x.
  - CM0 mode:** Bypass.
  - CM1 mode:** Bypass.
  - digital delay:** 0.
  - clock delay:** 0.
  - DAC mode:** dual DAC.
  - Offset:** disabled.
  - offset sync:** unchecked.
  - DACA Sleep:** unchecked.
  - DACB Sleep:** unchecked.
  - DACA Gain:** 15.
  - DACB Gain:** 15.
  - DAC A LPF:** enabled.
  - DAC B LPF:** enabled.
  - SLFST error:** mask.
  - FIFO error:** mask.
  - Setup/Hold Error:** mask.
  - serial interface:** 3-pin.
  - software sync:** unchecked.
  - self test:** disabled.
  - FA002:** disabled.
  - Fuse A:** disabled.
  - Fuse B:** disabled.
  - SDO:** Normal.
  - ATEST:** ATEST disabled.
  - Buttons:** Send All, Read All, Load Regs, Save Regs.
- CDCM7005 Register Configuration:**
  - M & N Selection:** Auto.
  - PLL Settings:**
    - Ref. Freq (MHz):** 10.
    - FB\_MUX:** 4.
    - VCXO Freq (MHz):** 800.
    - Phase Shift:** /16.
    - M Divider:** 1.
    - N Divider:** 20.
    - Output Freq (MHz):** 800.
  - Output Settings:**
    - Y0 Output (Unused):** Y0 Divider: 1, Y0 Level: LVPECL, 3-state.
    - Y1 Output (SMA Outputs):** Y1 Divider: 1, Y1 Level: LVPECL, 3-state.
    - Y2 Output (TSW3100):** Y2 Divider: 16, Y2 Level: LVPECL, active.
    - Y3 Output (DCLK):** Y3 Divider: 1, Y3 Level: LVPECL, 3-state.
    - Y4 Output (DAC5682 CLK):** Y4 Divider: 1, Y4 Level: LVPECL, active.
  - Buttons:** Send All, Load Regs, Save Regs.
- Register Table:**

Reg	Value	Hex
00	01000011	0x43
01	00010000	0x10
02	11100000	0xE0
03	01110000	0x70
04	00000000	0x00
05	00000010	0x02
06	00001110	0x0E
07	11111111	0xFF
08	00000000	0x00
09	00000000	0x00
0A	00001000	0x08
0B	00000000	0x00
0C	00000000	0x00
0D	00000000	0x00
0E	00000000	0x00
0F	00000000	0x00

**TSW3070 LED D3 should LOCK once the CDCM7005 is programmed**



# TSW3100 Tone GUI

**TSW3100\_MultiTonePattern**

**Signal Characteristics**

200 Sample Rate (MSPS) 16 Resolution  Random Seed  
.5 Backoff 2^15 Vector size  Invert

External Figure

**Signal Type**

Complex  Real

**SINC Correction**

Data Band  Enable  
0 DAC IF Min (MHz)  
200 DAC IF Max (MHz)  
1 DAC Interp

**Tone Groups**

Enable	Tone BW	#	Tone Center	Gain (dB)
<input checked="" type="checkbox"/>	1	1	25.1	0
<input type="checkbox"/>	1	1	100.1	0
<input type="checkbox"/>	1	1	100.1	0
<input type="checkbox"/>	1	1	100.1	0

**TSW3100 Control**

master  slave  LVDS  CMOS  Two's Comp  Offset Bin

LOAD and Run  Interleaved

Start Stop

192.168.1.123

**Amplitude (dB)**

**Frequency (Hz)**  $\times 10^8$

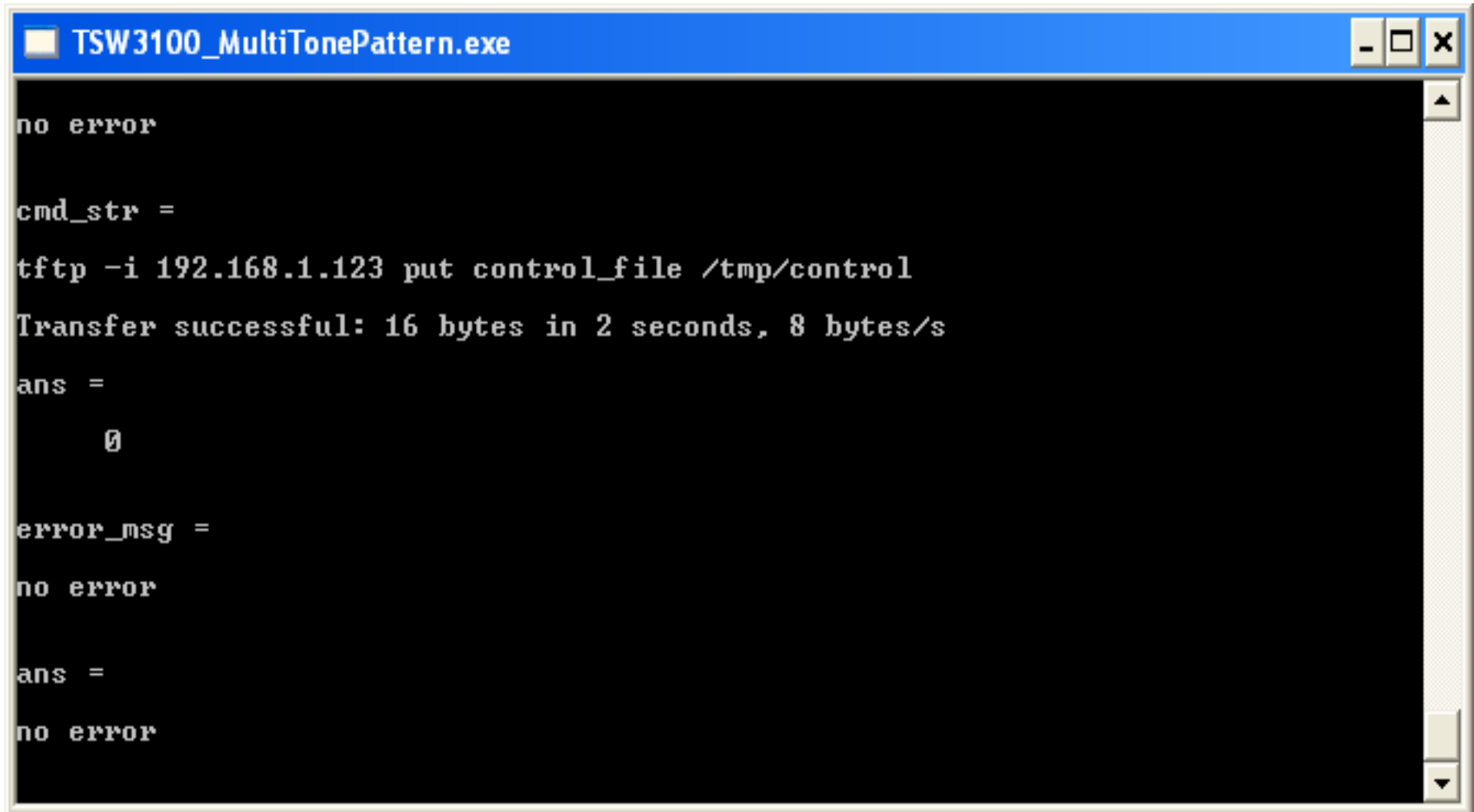
**Create and Save/Run TSW3100**

v. 1.0 (c) Texas Instruments 2007



# TSW3100 Tone GUI

## DOS window OK – no errors



```
TSW3100_MultiTonePattern.exe
no error

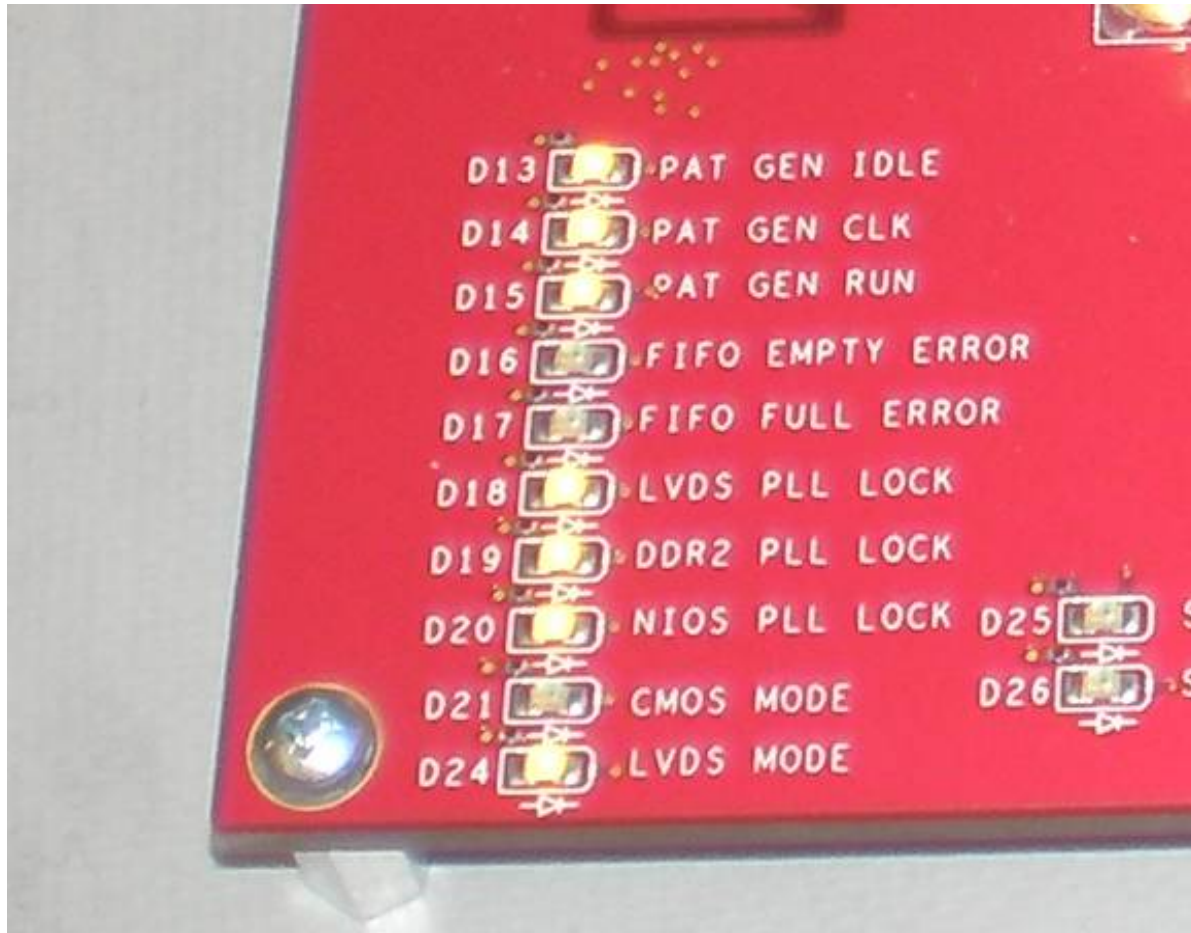
cmd_str =
tftp -i 192.168.1.123 put control_file /tmp/control
Transfer successful: 16 bytes in 2 seconds, 8 bytes/s

ans =
    0

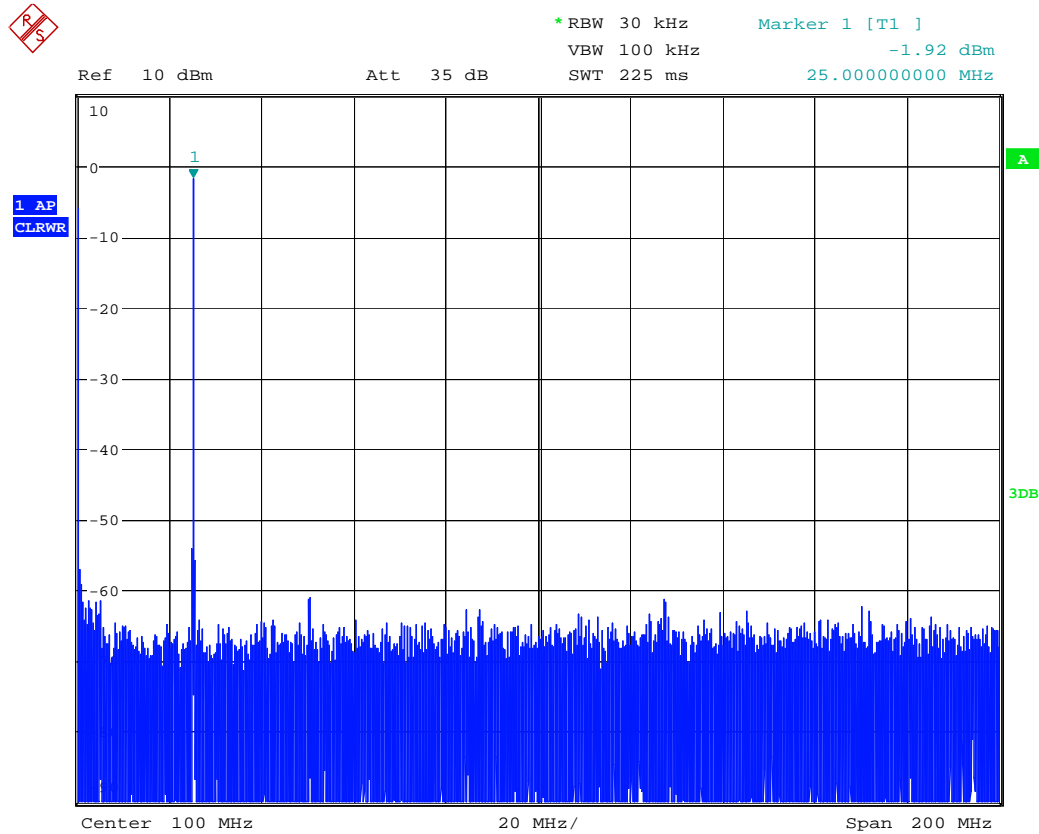
error_msg =
no error

ans =
no error
```

# TSW3100 LED status once the Tone is generated and loaded



# Spectral Plot from the analyzer showing 25M tone as expected.



Date: 3.MAR.2009 01:06:18

# Communications signal generation

- Due to the onboard VCXO of 800M, the exact sampling rates for the different communications standards will not be exactly matched.
- For example the WCDMA baseband rate is 3.84Msps. Using 4x interpolation, the datarate into the DAC is 200Msps, the closes multiple is 52x of 3.84=199.68M
- Although this is clocked into the DAC 200Msps the spectral shape will be different by less than 0.2%
- Other standards can also be generated using the various TSW3100 pattern generators, keep in mind the baseband rates, and the vector lengths when generating signals.
- For best results and to do demodulation of the generated signals, an exact frame of data is needed (vector length) and the sampling rates have to match. This will require an external clock at some clock rate that is matched to the baseband rate of the signal. For the case of WCDMA an external VCXO source based on 3.84M would be adequate. A nice number for the DAC5682 is 983.04M (256x3.84) or 491.52M (128x3.84)

# Comms Signal Generator Settings

The screenshot displays the TSW3100\_CommSignalPattern software interface, which is used for configuring a communications signal generator. The interface is organized into several functional panels:

- Test Models:** Includes radio buttons for TM1 - 64ch, TM3 - 32ch, TM5 - 30ch, TDS-CDMA, and QAM.
- Signal Type:** Includes radio buttons for Complex, Complex IF, and Real.
- Center Frequency:** Features a radio button for 16M and a checkbox for ExactFreq, with a text input field for the frequency in MHz (set to 30.72).
- Display Options:** Includes checkboxes for OCDF plot, Est. FFT Plot, IQ vs T, and a Res BW (kHz) input field (set to 30).
- Carriers:** A table for configuring multiple carriers with columns for Enable, Off Freq (MHz), Gain (dB), and SCR Code.
- Signal Characteristics:** A panel for advanced signal parameters including Chiprate (MSPS), Interpolation (NT), Vector size (K), Resolution, Backoff, and alpha, along with checkboxes for max size, time offset, Random Seed, and Invert, and a Time (ms) input field (set to 0.5).
- TSW3100 Control:** Includes radio buttons for master/slave and LVDS/CMOS, checkboxes for Two's Comp, Offset Bin, and Interleaved, a LOAD and Run button, a Stop button, and an IP address field (192.168.1.123).

A spectral plot is displayed in the center-right, showing Amplitude (dB) on the y-axis (ranging from 20 to 160) versus Frequency (Hz) on the x-axis (ranging from -1 to 1, scaled by  $10^8$ ). The plot shows a sharp peak at approximately 0.1  $\times 10^8$  Hz with an amplitude of about 145 dB. The plot title is "Res BW = 30000 Hz".

At the bottom of the interface, there is a large green "Create" button and a copyright notice: "v1.0 (c) 2001-2007 Texas Instruments".