

# ***Effect of Parasitic Capacitance in Op Amp Circuits***

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## **ABSTRACT**

Parasitic capacitors are formed during normal operational amplifier circuit construction. Operational amplifier design guidelines usually specify connecting a small 20-pF to 100-pF capacitor between the output and the negative input, and isolating capacitive loads with a small, 20-Ω to 100-Ω resistor. This application report analyzes the effects of capacitance present at the input and output pins of an operational amplifier, and suggests means for computing appropriate values for specific applications. The inverting and noninverting amplifier configurations are used for demonstration purposes. Other circuit topologies can be analyzed in a similar manner.

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## 1 Introduction

Two conductors, insulated from one another, carrying a charge, and having a voltage potential between them, form a capacitor. Capacitors are characterized by their charge-to-voltage ratio;  $C = \frac{q}{V}$ , where  $C$  is the capacitance in Farads,  $q$  is the charge in Coulombs, and  $V$  is the voltage in volts. In general, capacitance is a function of conductor area, distance between the conductors, and physical properties of the insulator. In the special case of two parallel plates separated by an insulator,  $C = \frac{\epsilon\epsilon_0 \times A}{d}$ , where  $\epsilon$  is the dielectric constant of the insulator,  $\epsilon_0$  is the permittivity of free space,  $A$  is the area of the plates, and  $d$  is the distance between the plates. Thus, in general:

- Capacitance is directly proportional to the dielectric constant of the insulating material and area of the conductors.
- Capacitance is inversely proportional to the distance separating the conductors.

Rarely are two parallel plates used to make a capacitor, but in the normal construction of electrical circuits, an unimaginable number of capacitors are formed. On circuit boards, capacitance is formed by parallel trace runs, or by traces over a ground or power plane. In cables there is capacitance between wires, and from the wires to the shield.

- Circuit traces on a PCB with a ground and power plane will be about 1–3 pF/in.
- Low capacitance cables are about 20–30 pF/ft conductor to shield.

Therefore, with a few inches of circuit board trace and the terminal capacitance of the operational amplifier, it is conceivable that there can be 15–20 pF on each operational amplifier terminal. Also, cables as short as a few feet can present a significant capacitance to the operational amplifier.

This report assumes that a voltage feedback operational amplifier is being used.

## 2 Basic One-Pole Operational Amplifier Model

The voltage feedback operational amplifier is often designed using dominant-pole compensation. This gives the operational amplifier a one-pole transfer function over the normal frequencies of operation that can be approximated by the model shown in Figure 1 (a). This model is used throughout this report in the spice simulations with the following values:  $gm = 0.1$ ,  $R_c = 1\text{ M}\Omega$  and  $C_c = 159\text{ nF}$ . With these values, the model has the following characteristics: dc gain = 100 dB, dominant-pole frequency = 10 Hz, and unity-gain bandwidth = 1 MHz.

In the schematic drawings, the representation shown in Figure 1 (b) is used, where

$$a = gm \times \frac{R_c}{1 + sR_cC_c}$$

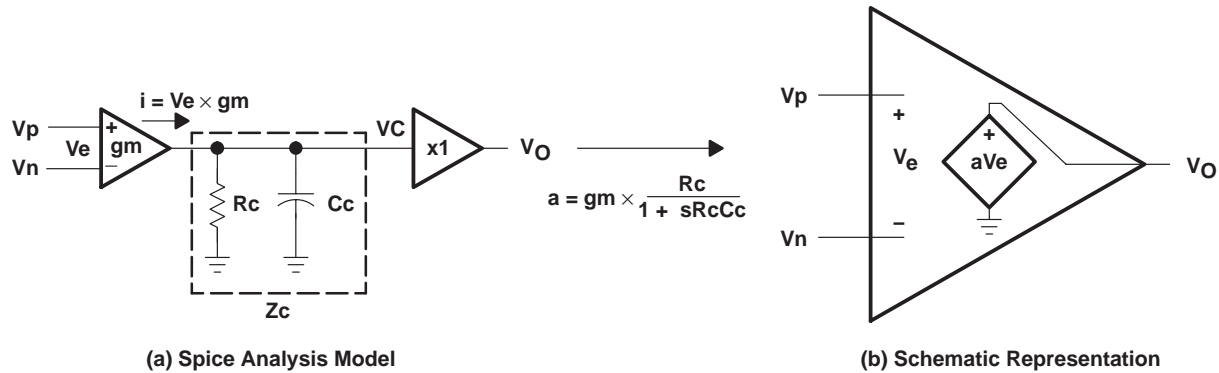


Figure 1. Basic Dominant-Pole Operational Amplifier Model

### 3 Basic Circuits and Analysis

Figure 2 (a) shows a noninverting amplifier and Figure 2 (b) shows an inverting amplifier. Both amplifier circuits are constructed by adding negative feedback to the basic operational amplifier model.

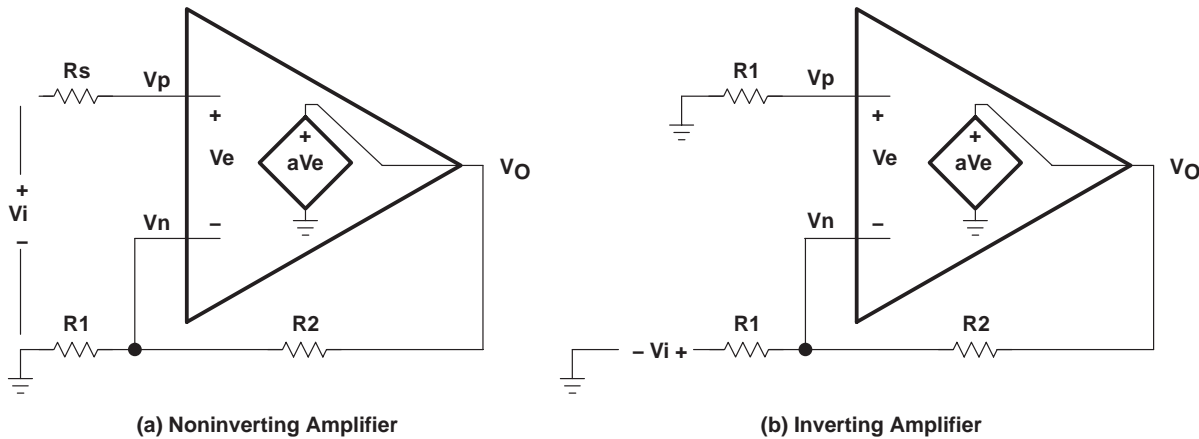


Figure 2. Amplifier Circuits Constructed With Negative Feedback

These circuits are represented in gain block diagram form as shown in Figure 3 (a) and (b). Gain block diagrams are powerful tools in understanding gain and stability analysis.

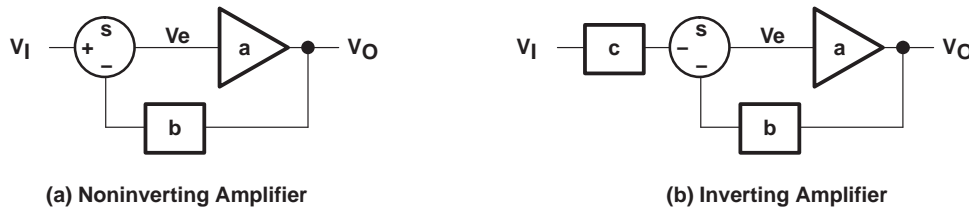


Figure 3. Gain-Block Diagrams

In the gain block diagrams:

$a = gm \times \frac{R_c}{1 + sR_cC_c}$ ,  $b = \frac{R_1}{R_1 + R_2}$ , and  $c = \frac{R_2}{R_1 + R_2}$ . Summing node *s* either inverts or passes each input unchanged—depending on the sign at the input—and adds the results together to produce the output.

### 3.1 Gain Analysis

In the gain block diagram of Figure 3 (a) (noninverting amplifier),  $V_o = aV_e = a(V_i - bV_o)$ . Solving for the transfer function:

$$\frac{V_o}{V_i} = \left(\frac{1}{b}\right) \left[ \frac{1}{1 + \frac{1}{ab}} \right] = \left(\frac{R1 + R2}{R1}\right) \left[ \frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right) \left(\frac{R1 + R2}{R1}\right)} \right] \quad (1)$$

This equation describes a single pole transfer function where  $\frac{1}{b}$  is the dc gain and the pole is at the frequency where  $\frac{1}{ab} = 1$

In the gain block diagram of Figure 3 (b) (inverting amplifier),  $V_o = aV_e = a(-cV_i - bV_o)$ . Solving for the transfer function:

$$\frac{V_o}{V_i} = -\left(\frac{c}{b}\right) \left[ \frac{1}{1 + \frac{1}{ab}} \right] = \left(\frac{R2}{R1}\right) \left[ \frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right) \left(\frac{R1 + R2}{R1}\right)} \right] \quad (2)$$

This equation describes a single-pole transfer function where  $-\frac{c}{b}$  is the dc gain and the pole is at the frequency where  $\frac{1}{ab} = 1$ .

Figure 4 shows the results of a spice simulation of the circuits with  $R1$  and  $R2 = 100 \text{ k}\Omega$ , and  $R_s = 50 \text{ k}\Omega$ . As expected, the circuit gains are flat from dc to the point where  $\frac{1}{ab} = 1$ , and then roll-off at  $-20\text{dB/dec}$ . The open-loop gain is plotted for reference.

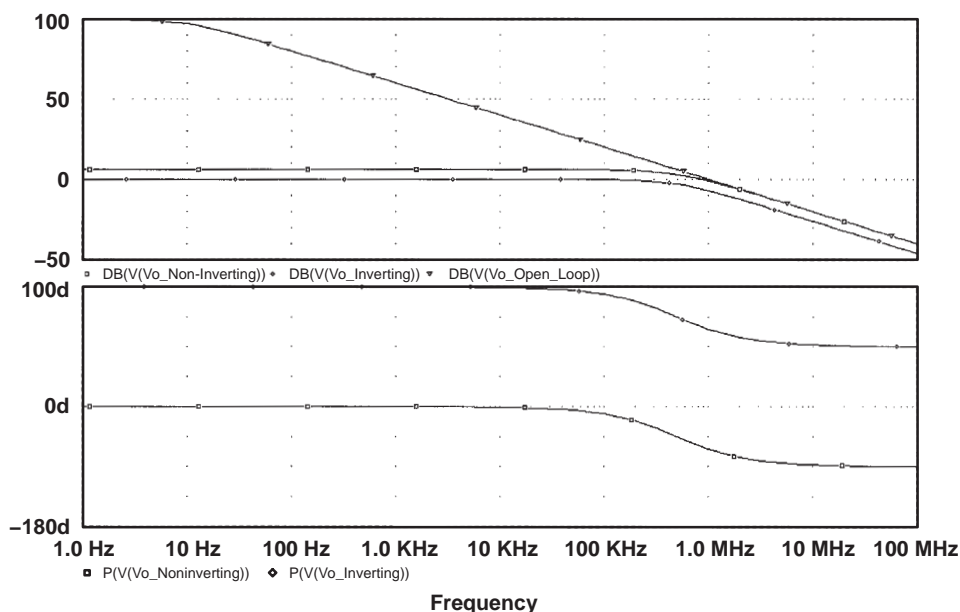


Figure 4. Spice Simulation of Noninverting and Inverting Amplifier

### 3.1.1 Stability Analysis

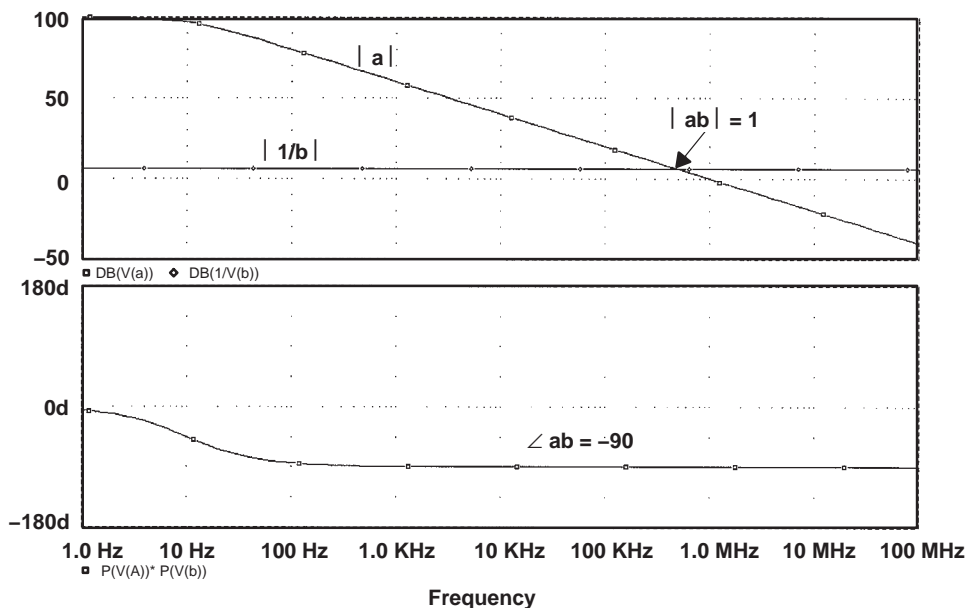
Using either gain block diagram, consider a signal traversing the loop from  $V_e$ , through the gain block  $a$ , to  $V_o$ , back through the gain block  $b$ , and the summing node  $s$  to  $V_e$ . If, while traversing this loop, the signal experiences a phase shift of  $0^\circ$ , or any integer multiple of  $360^\circ$ , and a gain equal to or greater than 1, it will reinforce itself causing the circuit to oscillate. Since there is a phase shift of  $180^\circ$  in the summing node  $s$ , this equates to:

$$|ab| \geq 1 \ \& \ \angle ab = -180^\circ \rightarrow \text{Oscillation.}$$

In reality, anything close to this usually causes unacceptable overshoot and ringing.

The product of the open-loop gain of the operational amplifier,  $a$ , and the feedback factor,  $b$ , is of special significance and is often termed the loop gain or the loop transmission. To determine the stability of an operational amplifier circuit, consider the magnitude,  $|ab|$ , and phase,  $\angle ab$ .

Figure 5 shows  $\text{dB } |a|$  and  $\text{dB } \frac{1}{b}$  plotted along with  $\angle ab$  for the one-pole operational amplifier model in either amplifier circuit with purely resistive feedback ( $R_1=R_2=100\text{K}$ ). It is obvious that the circuits are stable since the maximum phase shift in  $\angle ab$  is  $-90^\circ$ .



**Figure 5. Loop Gain Magnitude and Phase Plot**

At the point where  $\text{dB } |a|$  and  $\text{dB } \left| \frac{1}{b} \right|$  intersect,  $\text{dB } |a| - \text{dB } \left| \frac{1}{b} \right| = 0$ . This is the same as  $\log |a| + \log |b| = 0$ , and taking the antilog,  $|ab| = 1$ .

The slope of dB  $|a|$  or dB  $\left|\frac{1}{b}\right|$  indicates their phase:  $-40$  dB/dec =  $-180^\circ$ ,  $-20$  dB/dec =  $-90^\circ$ ,  $0$  dB/dec =  $0^\circ$ ,  $20$  dB/dec =  $90^\circ$ ,  $40$  dB/dec =  $180^\circ$ , etc. Since  $\left|\frac{1}{b}\right|$  is the inverse of  $|b|$ , the sign of its phase is opposite, i.e., if  $\angle b = -90^\circ$  then  $\angle \frac{1}{b} = 90^\circ$ . Therefore, a 40-dB/dec rate of closure between dB  $|a|$  and dB  $\left|\frac{1}{b}\right|$  indicates  $\angle ab = -180^\circ$  and the circuit is normally unstable. Plotting dB  $|a|$  and dB  $\left|\frac{1}{b}\right|$  on a logarithmic scale gives a visual indication of the stability of the circuit.

## 4 Capacitance at the Inverting Input

Figure 6 (a) and (b) show adding  $C_n$  to the noninverting and inverting amplifier circuits.

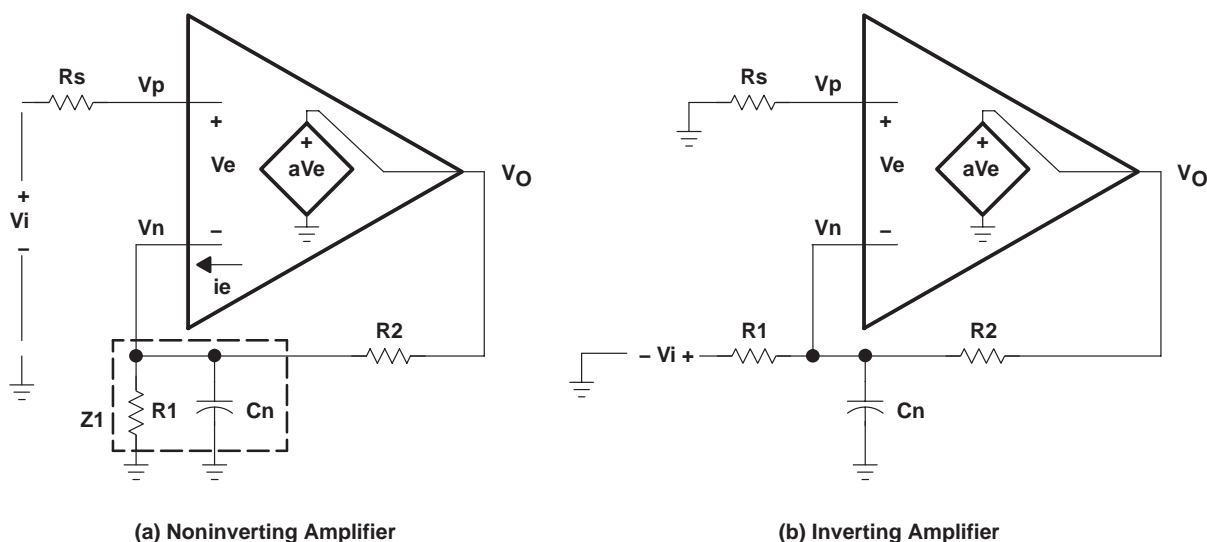


Figure 6. Adding  $C_n$  to Amplifier Circuits

### 4.1 Gain Analysis With $C_n$

Making use of the block diagrams and their related circuit solutions, determine how  $C_n$  has modified the gain block values and substitute as required.

For the noninverting amplifier shown in Figure 6 (a):

$$V_n = V_o \frac{Z_1}{Z_1 + R_2},$$

$$\text{where } Z_1 = \frac{R_1}{1 + sR_1C_n}.$$

Solving for the modified feedback factor:

$$b = \frac{Z_1}{Z_1 + R_2} = \left( \frac{R_1}{1 + sR_1C_n} \right) \left( \frac{1}{\left( \frac{R_1}{1 + sR_1C_n} \right) + R_2} \right) = \frac{1}{\frac{R_1 + R_2}{R_1} + sR_2C_n} \quad (3)$$

For the inverting amplifier shown in Figure 6 (b), writing the node equation at  $V_n$  results in:

$$\frac{V_n - V_i}{R_1} + V_n \times sC_n + \frac{V_n - V_o}{R_2} = 0.$$

Therefore,

$$\begin{aligned} V_n &= V_i \left( \frac{R_2}{R_1 + R_2 + sC_n R_1 R_2} \right) + \left( \frac{V_o (R_1)}{R_1 + R_2 + sC_n R_1 R_2} \right) \\ &= V_i \left[ \frac{1}{\frac{R_1 + R_2}{R_2} + sC_n R_1} \right] + V_o \left[ \frac{1}{\frac{R_1 + R_2}{R_1} + sC_n R_2} \right] \end{aligned}$$

As above:

$$b = \frac{1}{\frac{R_1 + R_2}{R_1} + sR_2 C_n}, \text{ and } c = \frac{1}{\frac{R_1 + R_2}{R_2} + sR_2 C_n}$$

Using these values in the solutions to the gain block diagrams of Figure 3, the noninverting amplifier's gain, with  $C_n$  added to the circuit, is:

$$\frac{V_o}{V_i} = \left( \frac{1}{b} \right) \left[ \frac{1}{1 + \frac{1}{ab}} \right] = \left( \frac{R_1 + R_2}{R_1} + sR_2 C_n \right) \left[ \frac{1}{1 + \left( \frac{1 + sR_c C_c}{gmR_c} \right) \left( \frac{R_1 + R_2}{R_1} + sR_2 C_n \right)} \right] \quad (4)$$

and the inverting amplifier's gain, with  $C_n$  added to the circuit, is:

$$\begin{aligned} \frac{V_o}{V_i} &= - \left( \frac{c}{b} \right) \left[ \frac{1}{1 + \frac{1}{ab}} \right] = - \left[ \frac{\frac{R_1 + R_2}{R_1} + sR_2 C_n}{\frac{R_1 + R_2}{R_2} + sR_1 C_n} \right] \left[ \frac{1}{1 + \left( \frac{1 + sR_c C_c}{gmR_c} \right) \left( \frac{R_1 + R_2}{R_1} + sR_2 C_n \right)} \right] \\ &= - \left( \frac{R_2}{R_1} \right) \left[ \frac{\frac{R_1 + R_2}{R_2} + sR_1 C_n}{\frac{R_1 + R_2}{R_2} + sR_1 C_n} \right] \left[ \frac{1}{1 + \left( \frac{1}{a} \right) \left( \frac{R_1 + R_2}{R_1} + sR_2 C_n \right)} \right] \\ &= - \left( \frac{R_2}{R_1} \right) \left[ \frac{1}{1 + \left( \frac{1 + sR_c C_c}{gmR_c} \right) \left( \frac{R_1 + R_2}{R_1} + sR_2 C_n \right)} \right] \end{aligned} \quad (5)$$

Figure 7 shows the results of a spice simulation of both amplifiers with  $C_n = 15.9$  nF, resistors  $R_1$  and  $R_2 = 100$  k $\Omega$ , and  $R_s = 50$  k $\Omega$ . Refer to it while taking a closer look at equations 4 and 5.

In equation 4, the first term

$$\left( \frac{R_1 + R_2}{R_1} + sR_2 C_n \right)$$

contains a zero at



$$f_z = \frac{R1 + R2}{2\pi R1 R2 Cn}$$

In the spice simulation we see effects of this zero as the gain begins to increase at around 200 Hz. In the second term of equation 4, substitute

$$Rm = \frac{1}{gm}, \text{ to get}$$

$$\left[ \frac{1}{1 + \left( \frac{Rm}{Rc} + sRmCc \right) \left( \frac{R1 + R2}{R1} + sR2Cn \right)} \right]$$

$$= \frac{1}{s^2(RmCcR2Cn) + s \left( R2Cn \frac{Rm}{Rc} + RmCc \frac{R1 + R2}{R1} \right) + 1 + \left( \frac{Rm}{Rc} \right) \left( \frac{R1 + R2}{R1} \right)}$$

Solving the characteristic equation for  $s^2$  in the denominator we find that the transfer function has a complex conjugate pole at  $s_{1,2} = -660 \pm j62890$ . Taking only the dominant terms in the equation, the double pole can be approximated in the frequency domain at:

$$P_{1,2} = \frac{1}{2\pi \sqrt{RmCcR2Cn}} = 10 \text{ kHz},$$

with the model values as simulated. At this frequency the denominator tends to zero and the gain theoretically increases toward infinity. What we see on the simulation results is peaking in the gain plot and a rapid  $180^\circ$  phase shift in the phase plot at 10 kHz. The circuit is unstable.

In equation 5, notice that the frequency effects of the capacitor cancel out of the first term of the transfer function. The simulation results show the gain is flat until the second term, which is identical to equation 4, causes peaking in the gain plot and a rapid  $180^\circ$  phase shift in the phase plot at 10 kHz. This circuit is also unstable.

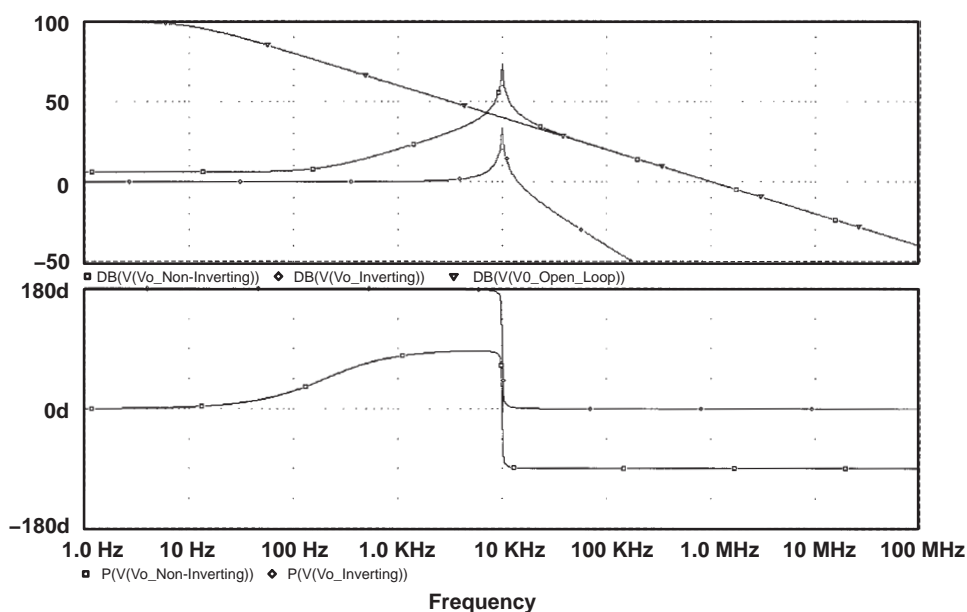


Figure 7. Spice Simulation of  $Cn$  in Noninverting and Inverting Amplifiers

### 4.1.1 Stability Analysis With $C_n$

To analyze stability with  $C_n$  added to the amplifier circuit, use the modified feedback factor,

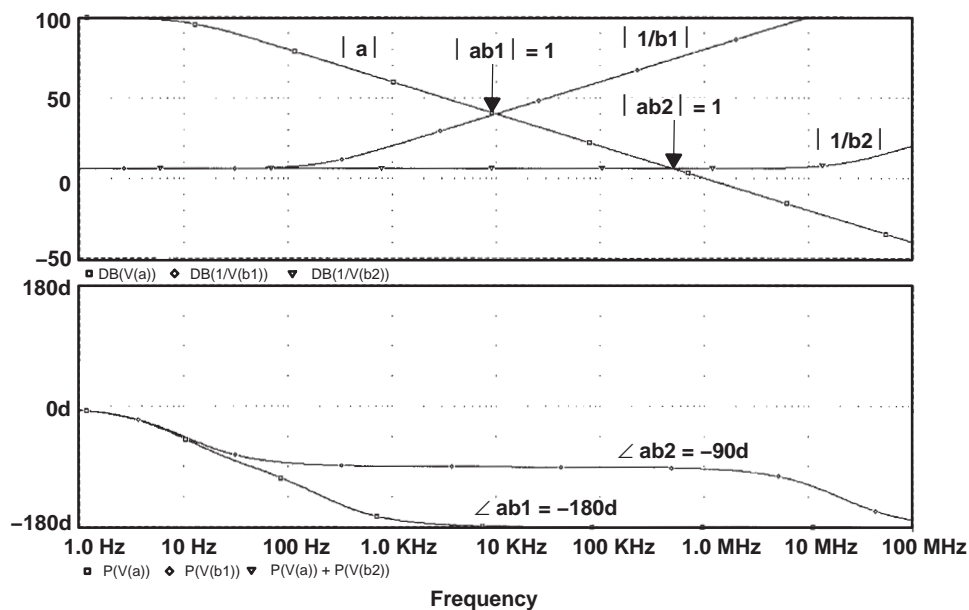
$$b = \frac{1}{\frac{R1 + R2}{R1} + sR2Cn}$$

At low frequencies, where

$$\frac{R1 + R2}{R1} \gg 2\pi fR2Cn, \quad \frac{1}{b} \cong \frac{R1 + R2}{R1}$$

and the plot is flat ( $\angle b = 0^\circ$ ). As frequency increases, eventually  $\frac{R1 + R2}{R1} = 2\pi fR2Cn$ . At this frequency  $\left|\frac{1}{b}\right| = \left(\frac{R1 + R2}{R1}\right)(\sqrt{2})$  ( $\angle b = -45^\circ$ ). Above this frequency  $\left|\frac{1}{b}\right|$  increases at 20 dB/dec ( $\angle b = -90^\circ$ ). Depending on the value of  $C_n$ , there are two possible scenarios:

1. The break frequency is below the frequency where  $\left|\frac{1}{b}\right|$  and  $|a|$  intersect. This causes the rate of closure between  $\left|\frac{1}{b}\right|$  and  $|a|$  to be 40 dB/dec. This is an unstable situation and will cause oscillations (or peaking) near this frequency. Reference  $\frac{1}{b1}$  in Figure 8 and the results of the spice simulation shown in Figure 7.
2. The break frequency is above the frequency where  $\left|\frac{1}{b}\right|$  and  $|a|$  intersect. There is no effect in the pass band of the amplifier. Reference  $\frac{1}{b2}$  in Figure 8.



**Figure 8. Loop Gain Magnitude and Phase Asymptote Plots With  $C_n$**

### 4.1.2 Compensating for the Effects of $C_n$

To compensate for the effects of  $C_n$ :

1. Reduce the value of  $C_n$  by removing ground or power plane around the circuit trace to the inverting input.
2. Reduce the value of  $R_2$ .
3. For noninverting amplifier, place a capacitor  $C_2 = C_n \frac{R_1}{R_2}$  in parallel with  $R_2$ .
4. For inverting amplifier, place a capacitor  $C_2 = C_n \frac{R_1}{R_2}$  in parallel with  $R_2$ , and place a capacitor  $C_1 = C_n$  in parallel with  $R_1$ .

Methods 1 and 2 attempt to move the effect of  $C_n$  to a higher frequency where it does not interfere with normal operation.

Method 3 is used for the noninverting amplifier. It cancels the effect of  $C_n$ .

To solve the modified transfer function with  $C_2$  in parallel with  $R_2$ , substitute  $Z_2$  for  $R_2$ , where  $Z_2 = \frac{R_2}{1 + sR_2C_2}$ , in the derivation of  $b$  so that:

$$b = \frac{V_n}{V_o} = \frac{Z_1}{Z_1 + Z_2} = \left[ \frac{\left( \frac{R_1}{1 + sR_1C_n} \right)}{\left( \frac{R_1}{1 + sR_1C_n} \right) + \left( \frac{R_2}{1 + sR_2C_2} \right)} \right] = \frac{1}{1 + \left( \frac{R_2}{R_1} \right) \left( \frac{1 + sR_1C_n}{1 + sR_2C_2} \right)} \quad (6)$$

By setting  $C_2 = C_n \frac{R_1}{R_2}$ , equation 6 becomes:

$$b = \frac{1}{1 + \left( \frac{R_2}{R_1} \right) \left( \frac{1 + sR_1C_n}{1 + sR_1C_n} \right)} = \frac{1}{\left( \frac{R_1 + R_2}{R_1} \right)} = \left( \frac{R_1}{R_1 + R_2} \right).$$

Therefore, with the proper value of  $C_2$  the effect of  $C_n$  is cancelled and the feedback factor looks purely resistive.

This works so well for the noninverting amplifier, let us investigate doing the same thing with the inverting amplifier. Placing  $C_2 = C_n \frac{R_1}{R_2}$  across  $R_2$  will cancel the effect of  $C_n$  so that  $b$  is purely resistive as shown above, but it causes another problem. Recalculating  $c$  with  $C_2$  added we find:

$$c = \frac{Z_2}{R_1 + Z_2} \text{ where } Z_2 = \frac{R_2}{1 + sR_2C_2 || C_n} = \frac{1}{\frac{1}{R_2} + sC_x} \text{ where } C_x = C_2 || C_n.$$

In the transfer function,  $\frac{V_o}{V_i} = -\left( \frac{c}{b} \right) \left[ \frac{1}{1 + \frac{1}{ab}} \right]$ , the second term is fine, but expanding out the first term we find:

$$\left(\frac{c}{b}\right) = \left(\frac{R2}{1 + sR2Cx}\right) \left[ \frac{1}{R1 + \frac{R2}{1 + sR2Cx}} \right] \left(\frac{R1 + R2}{R1}\right) = \left(\frac{R2}{R1}\right) \left[ \frac{1}{1 + \frac{sR1R2Cx}{R1 + R2}} \right]$$

Obviously we now have a pole in the transfer function at  $f_p = 2\pi Cx \left( \frac{R1 + R2}{R1R2} \right)$  that limits the circuit's bandwidth. To cancel this pole, a zero needs to be added to the transfer function. Placing a capacitor,  $C1$ , across  $R1$  will create a zero in the transfer function.

Again  $c$  and  $b$  need to be recalculated. We already have the solution in the form of equation 6, and by proper substitution:

$$b = \frac{Vn}{Vo} = \left[ \frac{\left( \frac{R1}{1 + sR1Cn||C1} \right)}{\left( \frac{R1}{1 + sR1Cn||C1} \right) + \left( \frac{R2}{1 + sR2C2} \right)} \right] = \frac{1}{1 + \left( \frac{R2}{R1} \right) \left( \frac{1 + sR1Cn||C1}{1 + sR2C2} \right)} \quad (7)$$

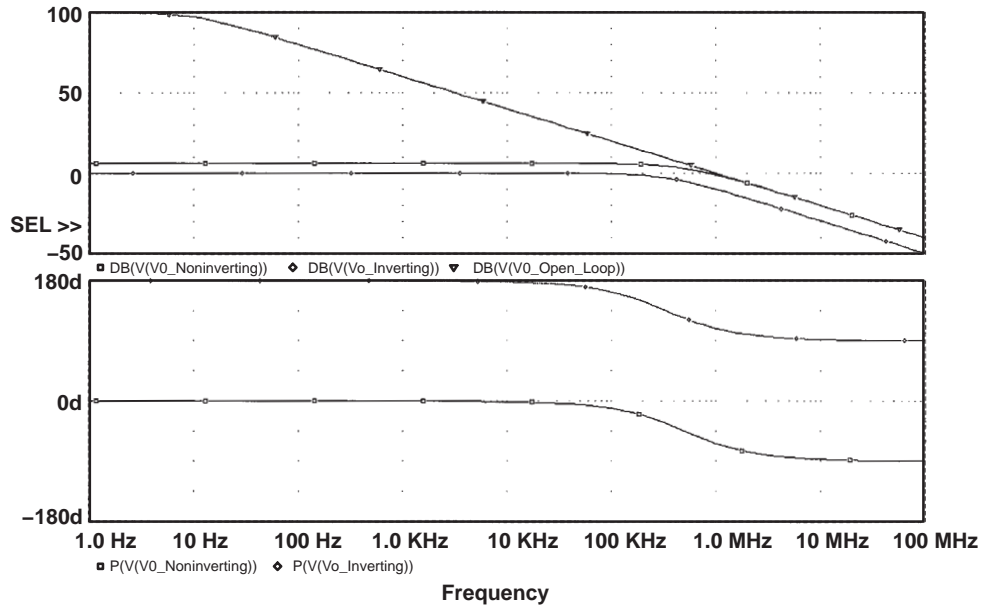
$$c = \frac{Vn}{Vi} = \left[ \frac{\left( \frac{R2}{1 + sR2Cn||C2} \right)}{\left( \frac{R2}{1 + sR2Cn||C2} \right) + \left( \frac{R1}{1 + sR1C1} \right)} \right] = \frac{1}{1 + \left( \frac{R1}{R2} \right) \left( \frac{1 + sR2Cn||C2}{1 + sR1C1} \right)}$$

$$\left(\frac{c}{b}\right) = \frac{1 + \left(\frac{R2}{R1}\right) \left(\frac{1 + sR1Cn||C1}{1 + sR2C2}\right)}{1 + \left(\frac{R1}{R2}\right) \left(\frac{1 + sR2Cn||C2}{1 + sR1C1}\right)}$$

Setting  $C2 = (Cn||C1) \frac{R1}{R2}$  in the numerator, simultaneously with setting  $C1 = (Cn||C2) \frac{R2}{R1}$  in the denominator, results in cancellation. The problem is that this cannot be simultaneously achieved.

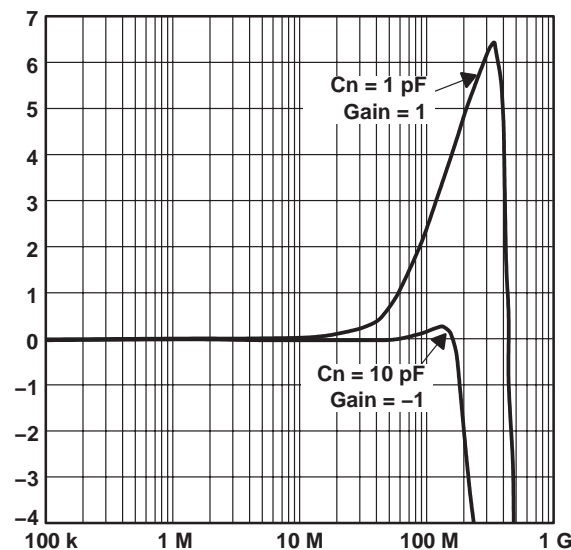
To arrive at a suitable compromise, assume that placing  $C2 = Cn \frac{R1}{R2}$  across  $R2$  cancels the effect of  $Cn$  in the feedback path as described above. Then, isolate the signal path between  $Vi$  and  $Vn$  by assuming  $R2$  is open. With this scenario,  $Cn$  is acting with  $R1$  to create a pole in the input signal path, and placing an equal value capacitor in parallel with  $R1$  will create a zero to cancel its effect.

Figure 9 shows the results of a spice simulation where methods 3 and 4 are used to compensate for  $Cn = 15.9$  nF.  $C2 = 15.9$  nF in the noninverting amplifier and  $C1 = C2 = 15.9$  nF in the inverting amplifier. In both amplifier circuits, resistors  $R1$  and  $R2 = 100$  k $\Omega$ , and  $Rs = 50$  k $\Omega$ . The plots show excellent results.



**Figure 9. Simulation Results With C1 and C2 Added to Compensate for  $C_n$**

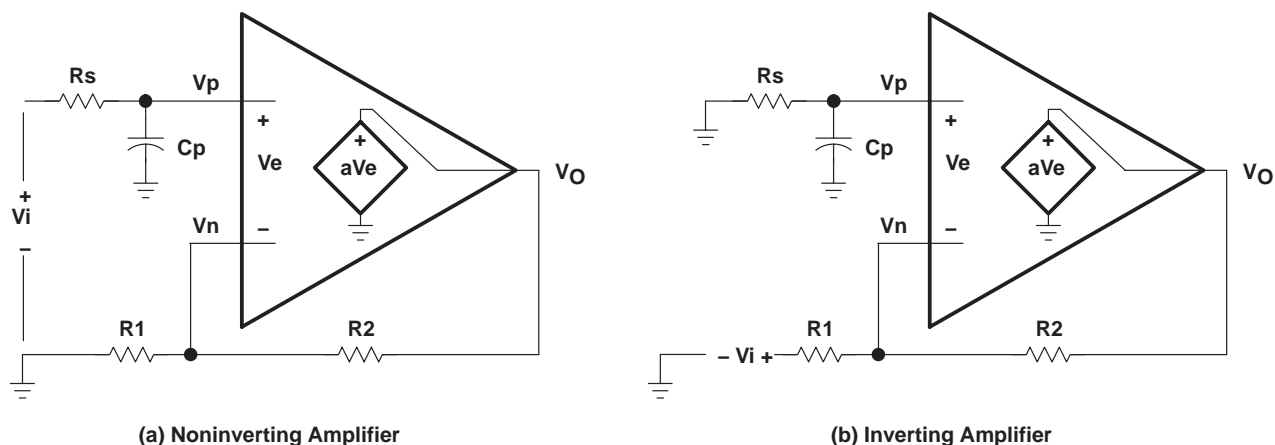
The action of any operational amplifier operated with negative feedback is such that it tries to maintain 0 V across the input terminals. In the inverting amplifier, the operational amplifier works to keep 0 V (and thus 0 charge) across  $C_n$ . Because capacitance is the ratio of charge to potential, the effective capacitance of  $C_n$  is greatly reduced. In the noninverting amplifier  $C_n$  is charged and discharged in response to  $V_i$ . Thus the impact of  $C_n$  depends on topology. Lab results verify that, in inverting amplifier topologies, the effective value of  $C_n$  will be reduced by the action of the operational amplifier, and tends to be less problematic than in noninverting topologies. Figure 10 shows that the effects of adding  $C_n$  to a noninverting amplifier are much worse than adding ten times the same amount to an inverting amplifier with similar circuit components.



**Figure 10. Effect of  $C_n$  in Inverting and Noninverting Amplifier**

## 5 Capacitance at the Noninverting Input

In Figure 11  $C_p$  is added to the amplifier circuits.



**Figure 11. Adding  $C_p$  to Amplifier Circuits**

### 5.1 Gain Analysis With $C_p$

In the case of the noninverting amplifier, the voltage seen at the noninverting input is modified so that  $V_p = V_i \left( \frac{1}{1 + sR_sC_p} \right)$ . Thus there is a pole in the input signal path before the signal reaches the input of the operational amplifier.  $R_s$  and  $C_p$  form a low-pass filter between  $V_i$  and  $V_p$ . If the break frequency is above the frequency at which  $\left| \frac{1}{b} \right|$  intersects  $|a|$ , there is no effect on the operation of the circuit in the normal frequencies of operation.

The gain of the inverting amplifier is not affected by adding  $C_p$  to the circuit.

Figure 14 shows the results of a spice simulation where  $C_p = 15.9$  nF. In both amplifier circuits, resistors  $R_1$  and  $R_2 = 100$  k $\Omega$ , and  $R_s = 50$  k $\Omega$ . The plot shows a pole in the transfer function of the noninverting amplifier, whereas the inverting amplifier is unaffected.

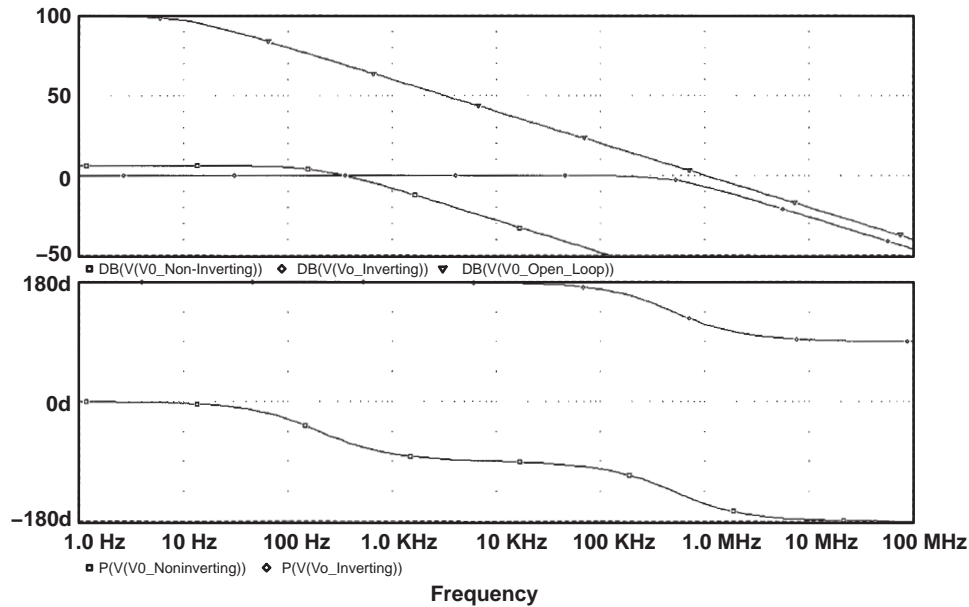


Figure 12. Spice Simulation With  $C_p$  in Noninverting and Inverting Amplifier Circuits

## 5.2 Stability Analysis With $C_p$

There is no change in the loop gain and thus no effect on stability for either amplifier circuit.

## 5.3 Compensating for the Effects of $C_p$

To compensate for the effect of capacitance at the noninverting input:

1. Reduce the value of  $C_p$  by removing ground or power plane around the circuit trace to the noninverting input.
2. Reduce the value of  $R_s$ .
3. Place a capacitor,  $C_s$ , in parallel with  $R_s$  so that  $C_s \gg C_p$ .

Methods 1 and 2 attempt to move the effect of  $C_p$  to a higher frequency where it does not affect transmission of signals in the pass band of the amplifier.

Method 3 tries to cancel the effect of  $C_p$ . The modified transfer function with  $C_s$  in parallel with  $R_s$  is:

$$\frac{V_p}{V_i} = \left( \frac{1 + sR_sC_s}{1 + sR_s(C_p + C_s)} \right) \quad (8)$$

If  $C_s \gg C_p$ , then  $\left( \frac{1 + sR_sC_s}{1 + sR_s(C_p + C_s)} \right) \cong 1$  and  $V_p \cong V_i$ .

Figure 13 shows the results of a spice simulation of the previous noninverting amplifier circuit where a 159-nF and a 1.59- $\mu$ F capacitor is placed in parallel with  $R_s$  to compensate for  $C_p = 15.9$  nF. The plot shows that a 10:1 ratio is good—loss of 1 db in gain at higher frequencies, but with a 100:1 ratio the effects of  $C_p$  are undetectable.

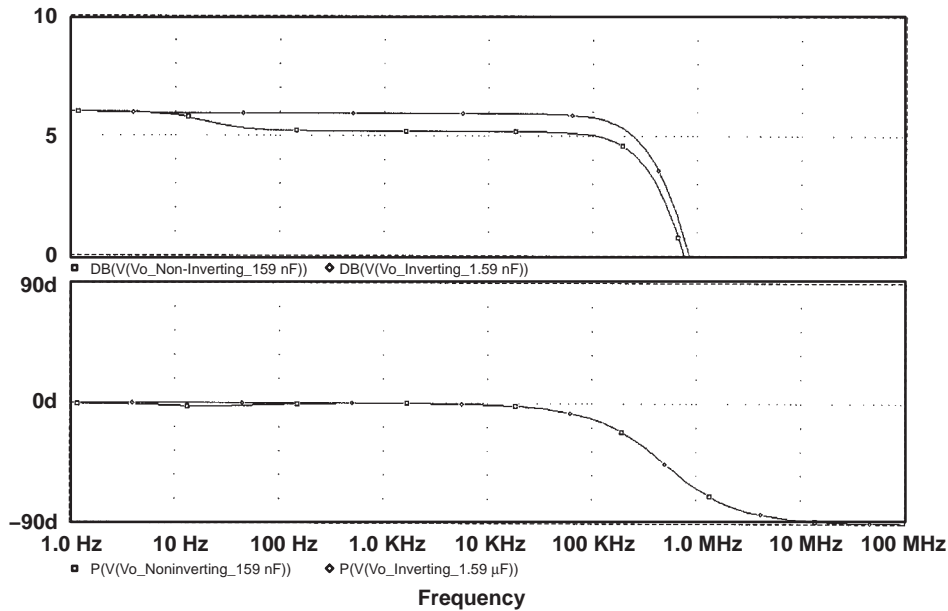


Figure 13. Spice Simulation With  $C_s$  Added to Compensate for  $C_p$  in Noninverting Amplifier

## 6 Output Resistance and Capacitance

Figure 14 shows  $R_o$  and  $C_o$  added to the amplifier circuits.  $R_o$  represent the output resistance of the operational amplifier and  $C_o$  represents the capacitance of the load.

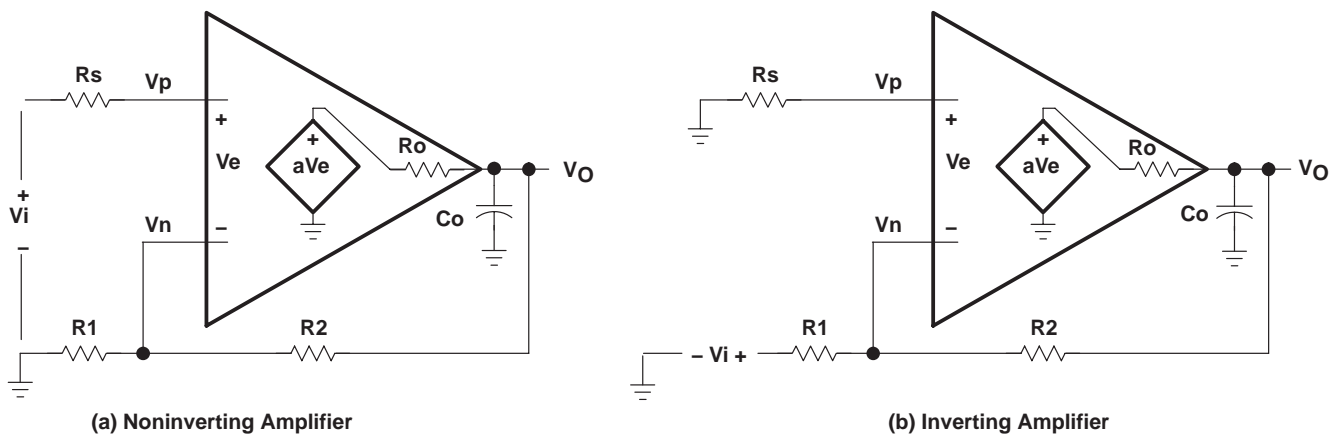


Figure 14.  $R_o$  and  $C_o$  Added to Amplifiers

### 6.1 Gain Analysis With $R_o$ and $C_o$

Assuming that the impedance of  $R_2$  is much higher than the impedance of  $R_o$  and  $C_o$ , the gain block diagrams for the amplifiers are modified to those shown in Figure 15 where:

$$d = \frac{V_o}{aV_e} = \frac{1}{1 + sR_oC_o}$$



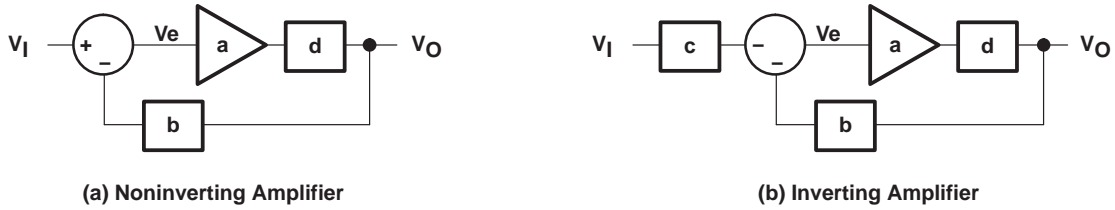


Figure 15. Gain Block Diagrams With  $R_o$  and  $C_o$

Using Figure 15 (a), we calculate the transfer function of the noninverting amplifier:

$$\frac{V_o}{V_i} = \frac{1}{b} \left[ \frac{1}{1 + \frac{1}{abd}} \right] = \left( \frac{R1 + R2}{R1} \right) \left[ \frac{1}{1 + \left( \frac{1 + sRcCc}{gmRc} \right) \left( \frac{R1 + R2}{R1} \right) (1 + sRoCo)} \right] \quad (9)$$

Using Figure 15 (b), we calculate the transfer function of the inverting amplifier:

$$\frac{V_o}{V_i} = -\left( \frac{c}{b} \right) \left[ \frac{1}{1 + \frac{1}{abd}} \right] = -\left( \frac{R2}{R1} \right) \left[ \frac{1}{1 + \left( \frac{1 + sRcCc}{gmRc} \right) \left( \frac{R1 + R2}{R1} \right) (1 + sRoCo)} \right] \quad (10)$$

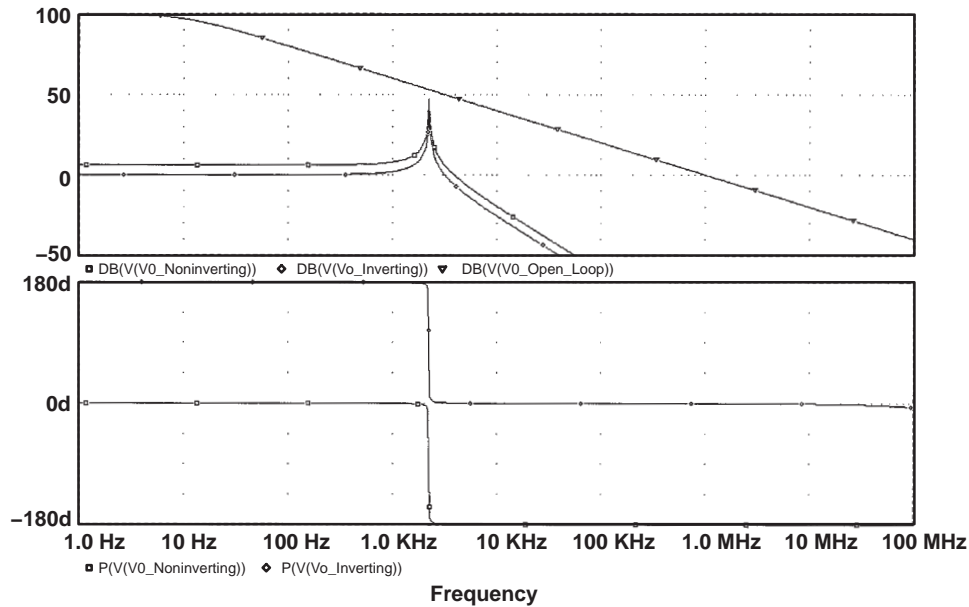
Figure 16 shows the results of a spice simulation with  $R_o = 100 \Omega$  and  $C_o = 159 \mu\text{F}$ . Resistors  $R1$  and  $R2 = 100 \text{ k}\Omega$ , and  $R_s = 50 \text{ k}\Omega$ . Refer to the simulation results while taking a closer look at the second term of equations 9 and 10. Expanding the denominator of the second term with  $R_m = \frac{1}{gm}$  and collecting  $s$  terms:

$$s^2(RmCcRoCo) \left( \frac{R1 + R2}{R1} \right) + s \left( RoCo \left( \frac{Rm}{Rc} \right) + RmCc \right) \left( \frac{R1 + R2}{R1} \right) + 1 + \left( \frac{Rm}{Rc} \right) \left( \frac{R1 + R2}{R1} \right)$$

Solving the characteristic equation for  $s^2$ , the transfer function has a complex-conjugate pole at  $s_{1,2} = -63 + j14,063$ . Taking only the dominant terms in the equation, the double pole can be approximated in the frequency domain to:

$$f_{p1,2} \cong \frac{1}{2\pi \sqrt{RmCcRoCo \left( \frac{R1 + R2}{R1} \right)}} = 2.2 \text{ kHz},$$

with the model values as simulated. At this frequency the second term's denominator tends to zero and the gain theoretically increases to infinity. What we see in the simulation results at 2.2 kHz is significant peaking in the gain, and a rapid 180° phase shift. The circuit is unstable.



**Figure 16. Spice Simulation With  $R_o$  and  $C_o$**

## 6.2 Stability Analysis With $R_o$ and $C_o$

By the gain block diagrams shown in Figure 15 (a) and (b), the loop gain is now =  $abd$  for both circuits. Since gain blocks  $a$  and  $b$  are not changed, to determine the stability of the circuit, the effect of gain block  $d$  is analyzed.

As noted above,  $d = \frac{V_o}{aV_e} = \frac{1}{1 + sR_oC_o}$ . At low frequencies where  $1 \gg 2\pi fR_oC_o$ ,  $\frac{1}{d} \cong 1$  and the plot is flat ( $\angle d = 0^\circ$ ). As frequency increases, eventually  $2\pi fR_oC_o = 1$ . At this frequency  $\left|\frac{1}{d}\right| = (\sqrt{2})$ , and  $\angle d = -45^\circ$ . Above this frequency  $\left|\frac{1}{d}\right|$  increases at 20 dB/dec, and  $\angle d = -90^\circ$ . Depending on the value of  $R_o$  and  $C_o$ , there are two possible scenarios:

1. The break frequency is below the frequency where  $\left|\frac{1}{bd}\right|$  and  $|a|$  intersect. This causes the rate of closure to be 40 dB/dec. This is an unstable situation and will cause oscillations (or peaking) near this frequency. Reference  $\left|\frac{1}{bd1}\right|$  in Figure 17 and the results of the spice simulation shown in Figure 16.
2. The break frequency is above the frequency where  $\left|\frac{1}{bd}\right|$  and  $|a|$  intersect. There is no effect in the pass band of the amplifier. Reference  $\left|\frac{1}{bd2}\right|$  in Figure 17.

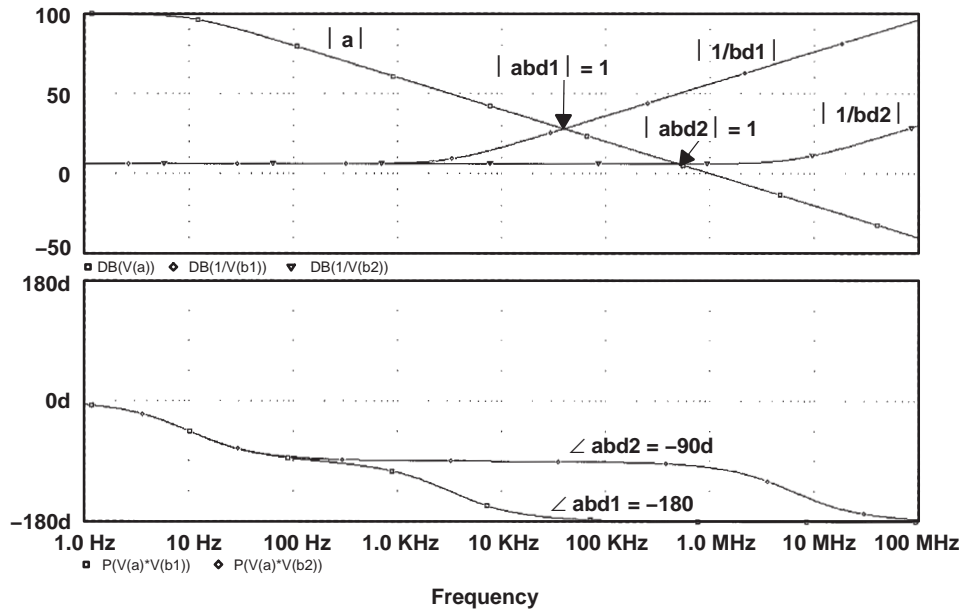


Figure 17. Loop Gain Magnitude and Phase With  $R_o$  and  $C_o$

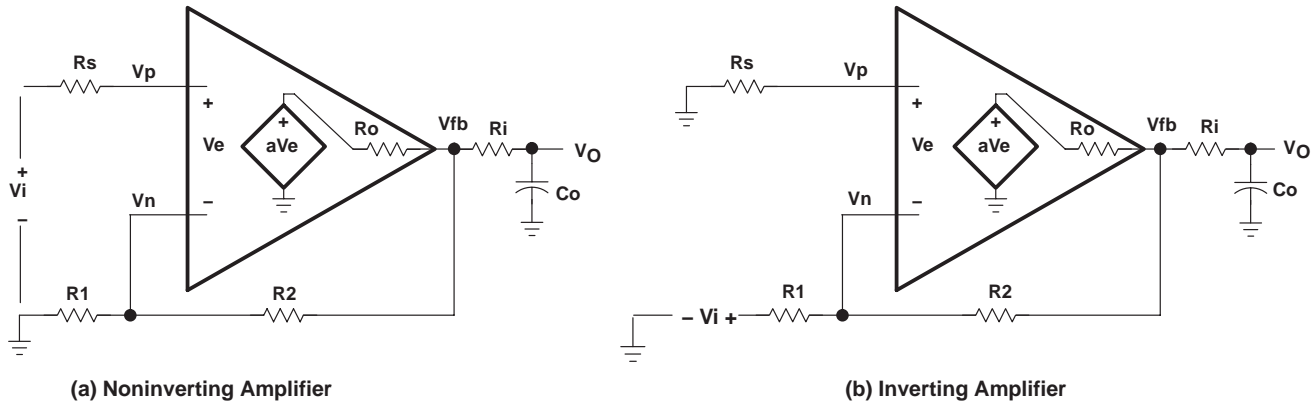
### 6.3 Compensation for $R_o$ and $C_o$

To compensate for the effect of capacitance at the output:

1. Reduce the value of  $C_o$  by removing ground or power plane around the circuit trace to the output.
2. Reduce the value of  $C_o$  by minimizing the length of output cables.
3. Isolate the output pin from  $C_o$  with a series resistor.
4. Isolate the output pin from  $C_o$  with a series resistor, and provide phase lead compensation with a capacitor across  $R_2$ .

Methods 1 and 2 seek to minimize the value of  $C_o$  and thus its effects, but there is a limit to what can be done. In some cases, you will still be left with a capacitance that is too large for the amplifier to drive. Then method 3 or 4 can be used, depending on your requirements.

Method 3 can be used if the resistive load is insignificant, or it is known and constant. Figure 18 shows the circuit modified with  $R_i$  added to isolate  $C_o$ . By observation, adding  $R_i$  increases the phase shift seen at  $V_o$ , but now the feedback is taken from node  $V_{fb}$ .



(a) Noninverting Amplifier

(b) Inverting Amplifier

**Figure 18. Isolation Resistor Added to Isolate the Feedback Loop From Effects of  $R_o$** 

This modifies the gain block  $d$ . Making the assumption that the impedance of  $R_o$ ,  $R_i$ , and  $C_o$  is small compared to  $R_2$ , then:

$$d = \frac{V_{fb}}{aV_e} = \left( \frac{R_i + \frac{1}{sC_o}}{R_o + R_i + \frac{1}{sC_o}} \right) = \frac{1}{\frac{R_o}{R_i} + 1 + \frac{1}{sR_iC_o}} + \frac{1}{1 + sC_o(R_i + R_o)}$$

Letting  $z = \frac{1}{\frac{R_o}{R_i} + 1 + \frac{1}{sR_iC_o}}$  and  $p = \frac{1}{1 + sC_o(R_i + R_o)}$ :  $d = z + p$ .  $z$  is a zero and  $p$  is a

pole. Both have the same corner frequency  $f_{z,p} = \frac{1}{2\pi C_o(R_i + R_o)}$ . When  $f \ll f_{z,p}$ , or when  $f \gg f_{z,p}$  the phase is zero. The ratio of  $R_i:R_o$  determines the maximum phase shift near  $f_{z,p}$ .

Figure 19 shows a plot of the phase shift of  $\frac{V_{fb}}{aV_e}$  versus frequency with various ratios of  $R_i:R_o$ , and Figure 20 plots the maximum phase shift vs the ratio of  $R_i:R_o$ . Depending on how much the phase margin can be eroded, a ratio can be chosen to suit. Note that the amount of phase shift depends only on the resistor ratio, not on the resistor or capacitor values (these set the frequency  $f_{z,p}$ ).

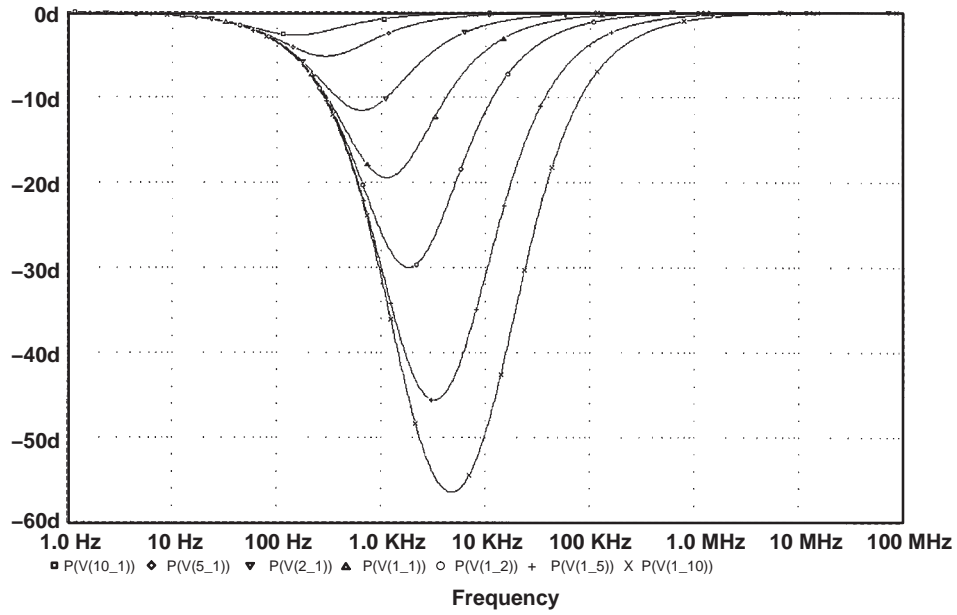


Figure 19. Phase Shift in  $\frac{V_{fb}}{aV_e}$  vs the Ratio  $R_i:R_o$

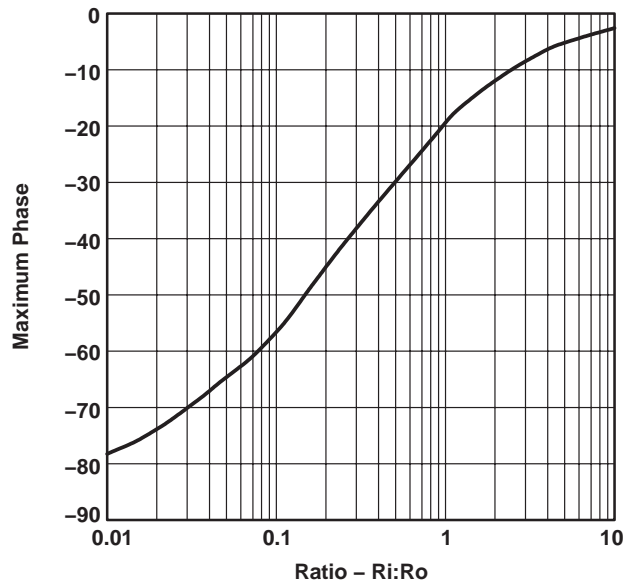
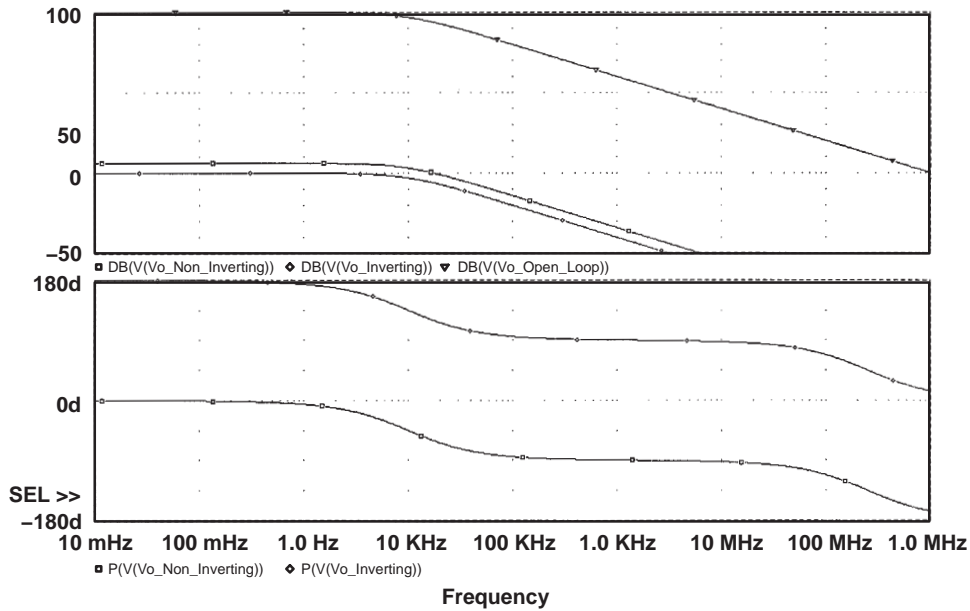


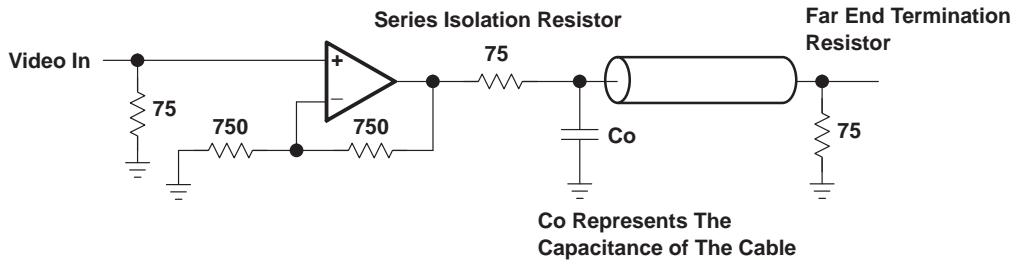
Figure 20. Maximum Phase Shift in  $\frac{V_{fb}}{aV_e}$  vs the Ratio  $R_i:R_o$

Figure 21 shows simulation results with the same circuits used for Figure 16 ( $R_o = 100 \Omega$  and  $C_o = 159 \mu F$ ), but with  $R_i = 100 \Omega$  added to the circuit. The circuits are stable.



**Figure 21. Spice Simulation Results With  $R_i$  Added to Compensate for  $R_o$  and  $C_o$**

A common use of an isolation resistor is shown in Figure 22, where a video buffer circuit is drawn. To avoid line reflections, the signal is delivered to the transmission line through a 75- $\Omega$  resistor, and the transmission line is terminated at the far end with a 75- $\Omega$  resistor. The gain of the operational amplifier is 2 to compensate for the voltage divider.



**Figure 22. Video Buffer Application**

If the load is unknown or dynamic in nature, method 3 is not satisfactory. Then method 4, the configuration shown in Figure 23, is used with better results. At low frequencies, the impedance of  $C_c$  is high in comparison with  $R_2$ , and the feedback path is primarily from  $V_o$ , restoring the dc and low frequency response. At higher frequencies the impedance of  $C_c$  is low compared with  $R_2$ , and the feedback path is primarily from  $V_{fb}$ , where the phase shift due to  $C_o$  is buffered by  $R_i$ .

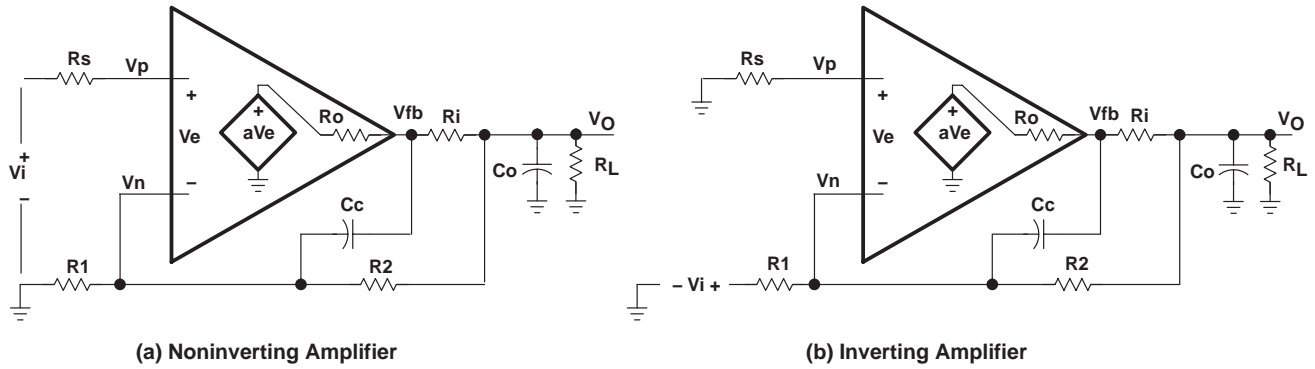


Figure 23.  $R_i$  and  $C_c$  Added to Compensate for Effects of  $R_o$  and  $C_o$

To solve these circuits analytically is quite cumbersome. By making some simplifications, the basic operation is more easily seen. The transfer function of interest is  $\frac{V_n}{aVe}$ .

Assume that the impedance of  $R_1$  and  $R_2$  is much higher than the impedance of  $R_i$ ,  $R_o$ , and  $C_o$ , and that  $C_c \ll C_o$ . At low frequencies,  $C_c$  looks like an open path and the circuit can be represented as shown in Figure 24 (a). At higher frequencies,  $C_c$  becomes active,  $C_o$  is essentially a short, and the circuit can be represented as shown in Figure 24 (b).

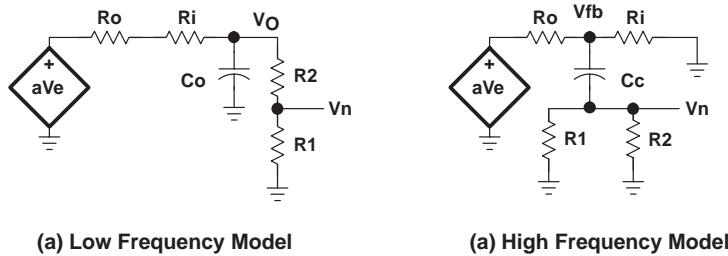


Figure 24. Simplified Feedback Models

This breaks the feedback into low and high-frequency circuits:

$$\text{At low frequency: } \frac{V_n}{aVe}(f_{low}) = \left( \frac{R_1}{R_1 + R_2} \right) \left( \frac{1}{1 + sC_o(R_o + R_i)} \right).$$

$$\text{At high frequency: } \frac{V_n}{aVe}(f_{high}) = \left( \frac{R_i}{R_i + R_o} \right) \left[ \frac{1}{1 + \frac{1}{sC_c(R_1 \parallel R_2)}} \right].$$

The overall feedback factor is a combination of the two so that:

$$\frac{V_n}{aVe} = \left( \frac{R_1}{R_1 + R_2} \right) \left( \frac{1}{1 + sC_o(R_o + R_i)} \right) + \left( \frac{R_i}{R_i + R_o} \right) \left[ \frac{1}{1 + \frac{1}{sC_c(R_1 \parallel R_2)}} \right]$$

This formula contains a pole and a zero. Choosing the value of the components so that the pole and zero are at the same frequency by setting  $C_c = C_o \frac{R_o + R_i}{R_1 || R_2}$  results in the feedback path switching from  $V_o$  to  $V_{fb}$  as the phase shift due to  $C_o(R_i + R_o)$  transitions to  $-90^\circ$ .

Figure 25 shows the simulation results of adding  $C_c = 636$  nF with isolation resistor,  $R_i = 100 \Omega$ , to the feedback path (as indicated in Figure 23). The circuit is no longer unstable and the low-frequency load independence of the output is restored. Simulation of the circuit shows similar results as those depicted in Figure 21, and is not shown.

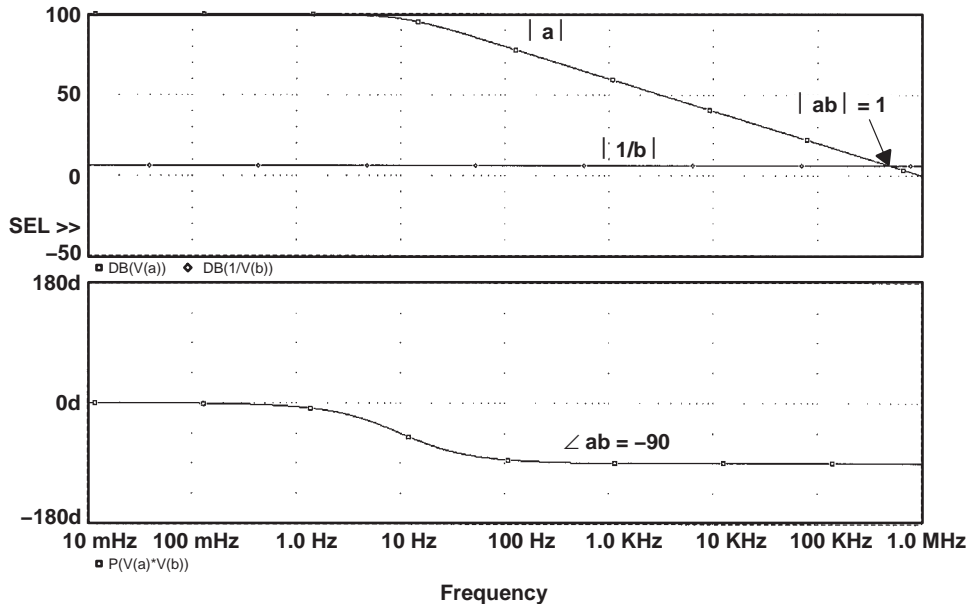


Figure 25. Simulation of Feedback Using  $R_i$  and  $C_c$  to Compensate for  $R_o$  and  $C_o$

## 7 Summary

The techniques described herein show means for analyzing and compensating for known component values. The value of parasitic components is not always known in circuit applications. Thus, the ubiquitous rule of thumb comes into play:

1. Always connect a small, 20-pF to 100-pF, capacitor between the output and the negative input.
2. If the operational amplifier has to drive a significant capacitance, isolate the output with a small, 20- $\Omega$  to 100- $\Omega$ , resistor.

Table 1. Noninverting Amplifier: Capacitor Location, Effect, and Compensation Summary

TOPOLOGY: NONINVERTING AMPLIFIER		
CAPACITOR LOCATION	EFFECT	COMPENSATION
All places	Various	Reduce capacitance and/or associated resistance.
Negative input, $C_n$	Gain peaking or oscillation	Compensate with $C_2 = C_n \frac{R_1}{R_2}$ across $R_2$ .



Positive input, $C_p$	Reduced bandwidth	Compensate with $C1 \gg Cn$ across $R1$ .
Output, $C_o$	Gain peaking or oscillation	<ol style="list-style-type: none"> <li>If load is known, isolate with resistor, <math>R_i = R_o</math>. This causes load dependence.</li> <li>If load is unknown, isolate with resistor, <math>R_i = R_o</math> and provide ac feedback from isolated point with <math>C_c = C_o \frac{R_o + R_i}{R1    R2}</math>.</li> </ol> <p>Provide dc feedback from <math>V_o</math>.</p>

**Table 2. Inverting Amplifier: Capacitor Location, Effect, and Compensation Summary**

TOPOLOGY: NONINVERTING AMPLIFIER		
CAPACITOR LOCATION	EFFECT	COMPENSATION
All places	Various	Reduce capacitance and/or associated resistance.
Negative input, $C_n$	Gain peaking or oscillation	Compensate with $C2 = Cn \frac{R1}{R2}$ across $R2$ , and $C1 = Cn$ across $R1$ .
Positive input, $C_p$	None	None
Output, $C_o$	Gain peaking or oscillation	<ol style="list-style-type: none"> <li>If load is known, isolate with resistor, <math>R_i = R_o</math>. This causes load dependence.</li> <li>If load is unknown, isolate with resistor, <math>R_i = R_o</math> and provide ac feedback from isolated point with <math>C_c = C_o \frac{R_o + R_i}{R1    R2}</math>.</li> </ol> <p>Provide dc feedback from <math>V_o</math>.</p>

## 8 References

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