

Simple Methods for Detecting Zero Crossing

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Abstract— *Affects of noise, harmonics, and multi-frequency signal make frequency and period measurements difficult for synchronizing control events. Various methods are presented to minimize errors in period and phase measurements. Both frequency and amplitude domain approaches are analyzed. Post detection processing allows greater accuracy. Static and dynamic hysteresis as well as interpolation methods of zero-crossing detection are investigated.*

Index Terms— *filtering, frequency, hysteresis, interpolation, period measurement, phase measurement, voltage comparator, phase locked loops, zero crossing detection.*

I. INTRODUCTION

Zero crossing detection is the most common method for measuring the frequency or the period of a periodic signal. When measuring the frequency of a signal, usually the number of cycles of a reference signal is measured over one or more time periods of the signal being measured. Measuring multiple periods helps to reduce errors caused by phase noise by making the perturbations in zero crossings small relative to the total period of the measurement. The net result is an accurate measurement at the expense of slow measurement rates.

Zero crossing is the point of choice for measuring phase and frequency. The reference is usually easy to establish and the signal's amplitude rate of change is maximum at signal zero. Phase synchronized triggering requires placing additional constraints on zero crossing detection. Weidenburg et. al. reviewed several method for synchronizing for firing thyristor based power converters and proposed adaptive online waveform reconstruction.^[1] Vainio et. al. describes a predictive digital filter for noise reduction.^{[2][3][4]} Depending upon the frequency for a particular application and the degree of signal processing, these methods can require high-speed processing components that are too expensive for low cost applications.

Fairchild Semiconductor has developed special purpose integrated circuits for silicon controlled rectifier (SCR) and triac control for low power applications. Such optical-isolated devices offer an additional advantage of electrical isolation between instrumentation and gate firing circuits.^[4] However, the design has no provision for mitigating multiple zero crossing nor does it compensate for diode forward voltage

drop.

II. ZERO CROSSING MEASUREMENT TECHNIQUES

Whether measuring period, frequency, or phase, the sources of errors are the same. When measuring a signal for the purposes of synchronization, fast and accurate frequency measurements are required.^{[5][6]} This requirement also translates into low phase distortion that can be introduced by frequency filtering and by measurement delays. The purpose of the instrumentation circuits and techniques discussed below are to reduce frequency errors due to multiple zero crossings (more than two per period) and reduce phase errors by advanced or delayed zero crossing.

Methods that require extensive processing have significant time delays from when changes of input frequency occur to when the change is reflected on the output. For this reason, methods described in this paper exclude highly computational methods including DFT and Wavelet type algorithms. The discussion methods is limited here to hardware and combined hardware and software techniques with low process delay. Although these methods can be applied to any frequency, the discussion here focuses on electric power system applications.

A. Pre-Detection Low Pass filtering

Low pass filtering or band pass filtering helps to restrict the bandwidth to the frequencies close to the frequency of the signal being measured. This technique is well suited for signals that are expected to have small deviations about a nominal fixed frequency. It is also well suited for signals corrupted by harmonics or other periodic signals that are sufficiently distinguishable from the signal of interest.

A simple first order filter that can be constructed with a resistor and capacitor is effective in reducing noise as shown in Fig. 1. The magnitude and phase response for a first-order low pass filter is shown in Fig. 2. The cutoff frequency for this filter is set for 600 Hz. Although the filter has little effect on the amplitude, there is significant phase shift at 60 Hz as shown in Fig. 1 which is predictable from the phase at 60 Hz on the filter's Bode plot shown in Fig. 2.

Higher order filters can appear to have zero phase shift but in reality, such filters merely have phase shifts of integer multiples of 360 degrees. This is true for both analog and digital filters. For digital filters, the phase delay is compounded by process delays.

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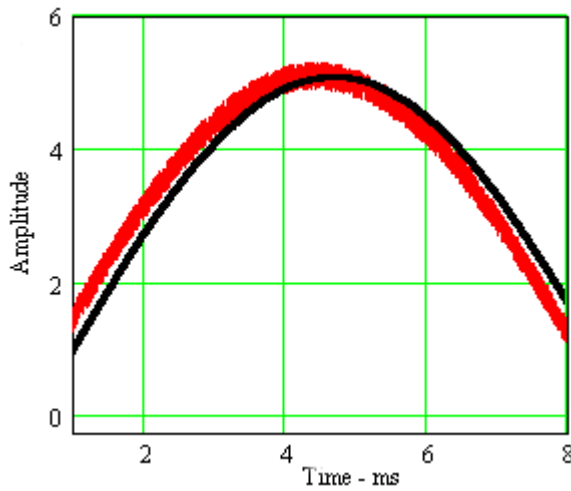


Fig. 1. Filtering signal to eliminate noise

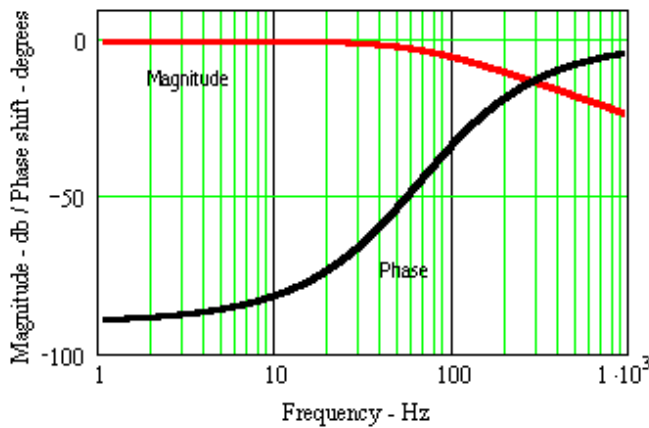


Fig. 2. Frequency and phase response of a 1st order Butterworth filter with cutoff at 600 Hz.

Filter phase delay can be compensated for mathematically if the filters characteristics are predictable. Unfortunately, filters constructed from physical resistors and capacitors have low accuracy, repeatability, and temperature stability. For the filter design used in this example, the phase shift is highly dependent on the frequency. This dependency further complicates phase compensation techniques. As the cutoff frequency is increased, the phase shift from filtering is less dependent on a specific frequency but the filters effectiveness for noise reduction is likewise reduced.

B. Post Processing Signal Conditioning

Multiple outputs for a single zero crossing must be expected in designs requiring accuracy and precision. Digital processing of the output signal does present significant advantages. There are two approaches: rule based and digital filtering. Rule based design eliminates events that don't meet expected timing requirements. This approach inhibits zero crossing detection for a specified period after an earlier detection event. This approach relies on the statistical probability that the next zero crossing will be close to the next half period. The inhibit period must be constrained to allow natural variations in the input signal.

Digital filtering has the ability to discriminate events based upon frequency of occurrence just as passive filtering but overcomes their disadvantages by having high accuracy and predictability. Such a method is the software implementation of a phase locked loop (PLL) with feed-forward control described by Wall and Hess.[5] The phase locked loop does compensate for advanced or delayed zero crossing detection due to noise and even, to a degree, that which is caused by harmonic or alien signal corruption. There is a compromise between the degree of rejection and the speed of adapting to new steady state conditions. There is no phase error because of the nature of the phased locked loop. Capture and lock dynamics can be dynamically changed if the PLL is implemented in software. Implementing a feed-forward algorithm increases the filter's response to changes in input frequency.

The software implementation of the PLL is a second order digital filter and requires minimal processor capability. The Microchip PIC16C73B, a microcontroller with 4K word program memory and 192 byte RAM, is sufficient to execute the PLL algorithm. Thus it remains a low cost implementation.

A significant improvement in performance can be realized by using both post processing techniques that allows event discrimination based on time and frequency. The time discrimination reduces the probability of erroneous zero crossing detection and the phased locked loop attempts to average the effect over a long period of time.

C. Simple Optical Isolated Semiconductor Devices.

One of the more simple approaches is to use an optical isolator with a Schmitt triggered logical output such as the TLP2200 in a circuit represented by top half of Fig. 3.[7] The data sheet for the TLP2200 specify that the LED forward voltage drop is 1.55 to 1.7vdc with a negative 0.2 mv/°C temperature coefficient. This voltage drop constitutes a phase shift that is device dependent, input signal level, and temperature dependent. Let the input signal be characterized by (1). The approximate slope of the input signal at the zero crossing is described by (2). Equation (3) provides the expression that represents the first order approximation of the phase shift as a function of volts around the zero crossing. Thus, for a 12 vac input signal, α equals 3.38 degrees/volt.

$$x(t) = Am \cdot \sin(\omega t) \quad (1)$$

$$s = \frac{d(x(t))}{dt} = \omega Am \cdot \cos(\omega t) \Big|_{t=0} \text{ volts / s} \quad (2)$$

$$\alpha = \frac{\omega \text{ rad / sec}}{\omega \cdot Am \text{ volts / sec}} = \frac{1}{Am} \text{ rad / volt or} \quad (3)$$

$$\alpha = \frac{180}{\pi Am} \text{ }^\circ \text{ angular per volt}$$

For the TLP2200 optical isolator, this expected zero crossing detection is 5.233 to 5.739 degrees leading or lagging

the actual zero crossing with a 0.6752 angular degree per °C temperature coefficient. As (3) reveals, α is inversely proportional to signal amplitude. Hence for a 120 vac input signal, the phases computed above will be only one tenth as great.

D. Zero-Crossing Detection by Interpolation

The implementation used in this design identifies two points on the sine wave: the first just before the positive going zero crossing and the second just after the same zero crossing. This implementation uses two optoisolators as shown in Fig. 3 to compensate for variations in level sensitivity and switching time delays. Optoisolators with Schmitt triggered outputs are used to provide additional hysteresis.

Input signals with constant frequency render delays due to optoisolator output switching indistinguishable from delays due to threshold levels. The interpolation method requires additional processor resources to accurately determine when two events occur. This usually requires that the processor have interrupt capability and capture and compare resources. The processor is programmed to capture the time of the times when *Out-* optoisolator output goes high and the *Out+* optoisolator output goes low. The true zero crossing is computed by linear interpolation between these two times. Fig. 4 shows that this method results in an improved degree of accuracy. The *Est. Zero* shown in Fig. 4 is computed from the phase-locked loop algorithm that estimates the next zero crossing time.[5]

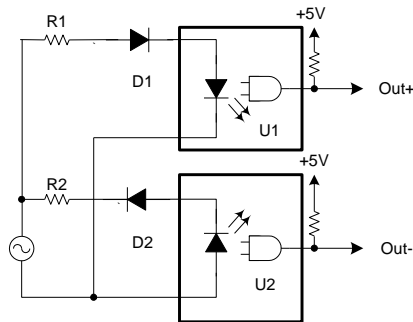


Fig. 3. Circuit for dual point interpolation method for detecting a zero crossing

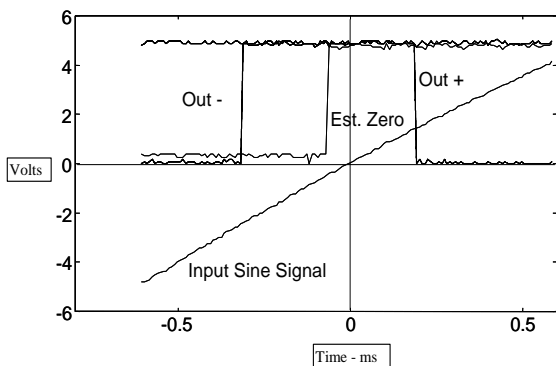


Fig.

4. Oscilloscope capture of the sine wave signal, optoisolator outputs and computed zero crossing.

The voltage drop of the external diodes D1 and D2 combined with the optoisolators internal LEDs cause the optoisolator outputs to switch state before and after that actual zero crossing. Processor algorithms inhibit recognizing more than one *Out-* or *Out+* outputs in succession. This is discussed in further detail in Section F. As Fig. 4 demonstrates, this method is not immune from phase error due to unequal turn on and turn off voltage levels.

E. Comparator Circuits with Fixed Hysteresis

It is common to use a circuit similar to that shown in Fig. 5 to translate voltage levels and provide noise immunity using fixed hysteresis. Note that this circuit used a single voltage supply. Manufacturers of electronic comparator integrated circuits specify that the maximum negative voltage on either positive or negative input is 0.3 volts.^[8] Schotky diodes, D1, and D2, clip the input voltage to limit the comparator input below recommended positive and negative levels.

This method works well provided that the signal being measured is free of distortion from harmonics that can potentially generate multiple zero-crossings per fundamental cycle. The Schotky diodes do not provide any appreciable noise rejection nor do they prevent multiple zero crossings per period due to distortion. Signal distortion from harmonic or other periodic signals can be reduced using classical frequency filtering techniques as described above. Signals can be filtered before passing through the zero crossing detector provided that they meet the constraints previously described.

Noise, on the other hand, is generally broad band and frequency filtering alone is insufficient to reduce detecting multiple zero crossings per half period. Although the resistive feedback hysteresis circuit shown in Fig. 5 provides a degree of immunity to noise, the circuit cannot prevent an advanced or delayed zero crossing. Hysteresis is used to prevent noise from generating multiple zero crossings during the time that the measured signal is very close to zero. The comparator's hysteresis voltage appears at its positive input and is labeled V_c in Fig. 5. Since the hysteresis snap action occurs when V_1 is nearly zero, the amount of hysteresis is computed by (5). If $R_0 + R_1$ is much greater than R_2 , then V_2 nearly equals 5 volts when V_c is positive.

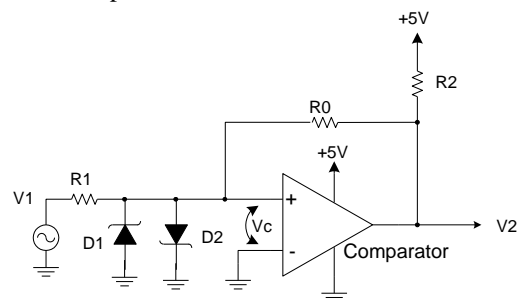


Fig. 5. Resistive feedback hysteresis circuit

$$V_c = V_2 \cdot \frac{R_1}{R_0 + R_1} \begin{cases} V_2 = 0 & \text{for } V_c < 0 \\ V_2 = \frac{5 \cdot (R_0 + R_1)}{R_0 + R_1 + R_2} & \text{for } V_c > 0 \end{cases} \quad (4)$$

Inherently, the signal to noise ratio is the lowest at a zero crossing thus requiring large hysteresis voltages when high noise levels are expected. The resistive hysteresis circuit also creates a time delay in the comparator transition from positive five volts to zero when the input sine passes through zero with a negative slope. Although a greater hysteresis voltage is desirable for better noise immunity, the period distortion is also greater. This has no adverse affects if period is being measured only when the input has a positive slope zero crossing. However, faster response measurements are possible if periods are measured twice each cycle. This is usually not done with fixed hysteresis since the two half periods are not symmetrical.

F. Comparator Output Frequency Filtering

The comparator output is frequently connected to some other electronic device that is capable of recording high-frequency binary outputs at V_2 shown in Fig. 3 and 4. Regardless of the input frequency filtering and the amount of voltage hysteresis, the probability of multiple comparator outputs for a single zero crossing remains. One is tempted to eliminate these high frequency events by using a simple passive or even active low pass filter between the comparator's output and the input to the next measuring circuit. This is not recommended because of the additional unpredictable delay from the temperature dependent low accuracy passive components. Phase locked loops are the exception to this caution as the principle is to maintain the phase relationship. Phase locked loops are discussed further in the next section.

G. Comparator Circuits with Dynamic Hysteresis

It is therefore desirable to have no voltage offset immediately before the input signals zero crossing and very high hysteresis immediately after the first zero crossing. The capacitive feedback comparator circuit shown in Fig. 6 has these characteristics. As before, it is reasonable to assume that R_1 is much greater than R_2 , $V_2(s)$ switched between zero and five volts.

The transfer function defined by $V_c(s)/V_2(s)$ from (5) is a high pass filter which allows the high frequencies from the V_2 step function to pass to the comparator positive input at V_c . This results in a step increase of V_c when the comparator first goes positive providing a large hysteresis and then decays to zero over time.

$$V_c(s) = V_2(s) \cdot \frac{G \cdot s}{s + \alpha} \quad \text{where } G = \left(\frac{2/T}{\tau + 2/T} \right), \quad (5)$$

$$\alpha = \frac{\tau - (2/T)}{\tau + (2/T)}, \quad \tau = (1/C \cdot R_1), \quad \text{and } T \text{ is the sample period.} \quad (6)$$

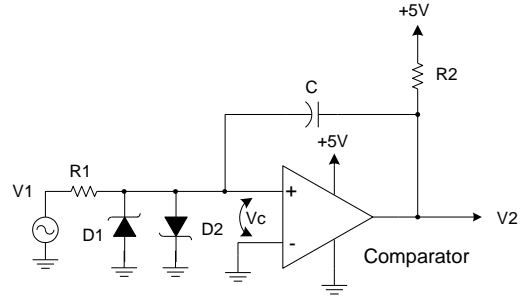


Fig. 6. Dynamic hysteresis comparator circuit

III. RESULTS OF DYNAMIC COMPARATOR HYSTERESIS

Fig. 6 and 7 demonstrate the simulated response for input sine wave, V_1 , with a 34 db signal to noise ratio. These plots readily show that the difference voltage between V_c and the input sine wave, V_1 goes to zero well before the next zero crossing but provides a large hysteresis until the wave form has reached almost half of its peak value. For this simulation, R_2 is 47K ohms, C is 10 nF, and R_1 is 4.7K ohms. Diodes, D_1 and D_2 were omitted because, as observed previously, they cannot prevent erroneous zero crossings. The input signal level for this simulation is 5 volts peak.

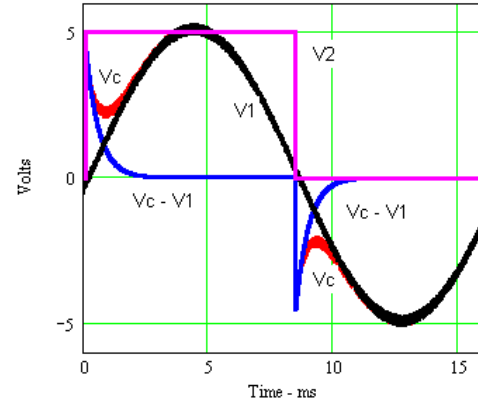


Fig. 7. The response of the dynamic zero crossing detector

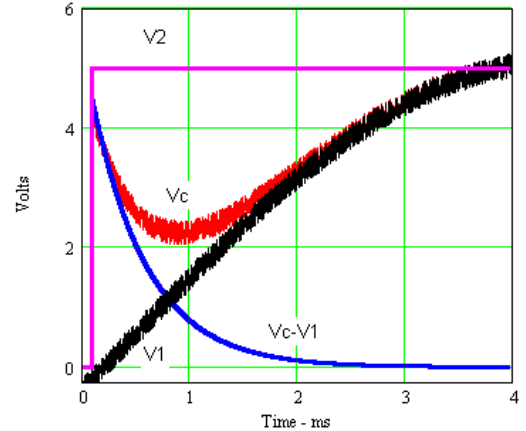


Fig. 8. Expanded plot of the dynamic zero crossing detector for positive output step

It is apparent that, although this approach results in reduced multiple zero crossing, it cannot eliminate advanced or delayed zero crossing detection. The dynamic hysteresis does eliminate distortion of period measurements made on two successive half periods.

IV. CONCLUSION

The accuracy of measuring zero crossing for synchronizing power system control and instrumentation requires a diverse approach to minimize phase detection errors from signals corrupted with noise and extraneous signals. Using optical isolated gates to detect a zero crossing can result in phase distortion due to the diode's non-zero forward voltage. This phase shift can be reduced using the interpolation method.

The dynamic hysteresis circuit provides high signal to noise ratio without period distortion due to DC level shifts on the measured AC signal. Although proper signal conditioning can improve the reliability of period measurements, phase errors cannot be totally eliminated. Using pre-filtering and post processing can improve zero crossing detection when combined with dynamic hysteresis or the interpolation method.

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