Practical Analog Design

Texas Instruments

INTRODUCTION

Texas Instruments is pleased to present the Practical Analog Design Seminar to our analog customers. This material represents some practical knowledge, as well as straight forward explanations of fundamental analog principles and design techniques.

Section 1 introduces the materials and describes the objectives for this seminar. Section 2 explores the basics of voltage feedback and current feedback amplifiers using feedback theory. The VFA/CFA discussion starts with a feedback review because that is where the difference between the circuits lies, continues through the simplified circuit diagrams, develops the circuit equations, compares stability, and ends with a detailed comparison of the parameters. Section 3 moves on to a discussion of signal routing and noise suppression. Section 3 is a design tools discussion. This section differentiates between selection tools, downloadable design tools, and a downloadable analysis tool. Then he does a live demonstration of three design tools and analysis tool. Operation of several of these tools are discussed in detail along with circuit examples.

This seminar was written by Ron Mancini. Ron has spent 47 years in electronics, where he authored/edited *Op Amps for Everyone*, wrote hundreds of papers, patented or co-patented 12 circuits, and gave hundreds of seminars. Ron has a talent for simplifying complicated subjects, and he is applying that talent to a discussion of voltage versus current feedback amplifiers, the age-old problem of routing signals/suppressing noise, and the new topic of PC based circuit design tools.

Charles Wray

Technical Training Manager

Texas Instruments

Practical Analog Design

Table of Contents

Practical Analog Design

Section—1

Introduction

What Will We Learn?

- VFA/CFA—Feedback review, equation development, and circuit comparison
- Signal integrity—The tricks and traps involved in laying out a working circuit board
- Design tools—The new goodies that decrease design time, increase performance, and are free from Texas Instruments

Section—2

Voltage and Current Feedback Amplifiers

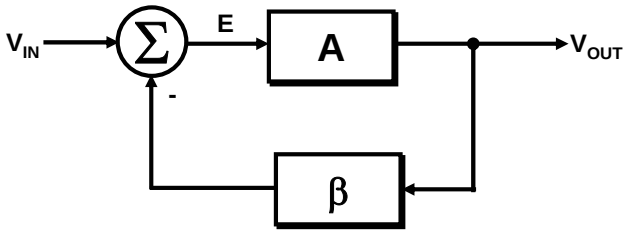
The key word here is feedback because neither of these amplifiers can be controlled without feedback. The general idea is to use excessive gain called Loop Gain to create a circuit that is solely dependent on the external passive resistors rather than on the amplifiers. This leads to a situation where the circuit performance is dictated by accurate and relatively drift free resistors.

Feedback Analysis Tools

Feedback Equation
Bode Plots
Stability
Second Order Equation

We investigate the fundamental feedback principles prior to looking at the individual amplifiers because knowledge of feedback is required to understand amplifiers.

The Feedback Equation (Circuit Theory)



$$V_{OUT} = EA$$

$$E = V_{IN} - \beta V_{OUT}$$

$$E = \frac{V_{OUT}}{A}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{(1 + A\beta)}$$

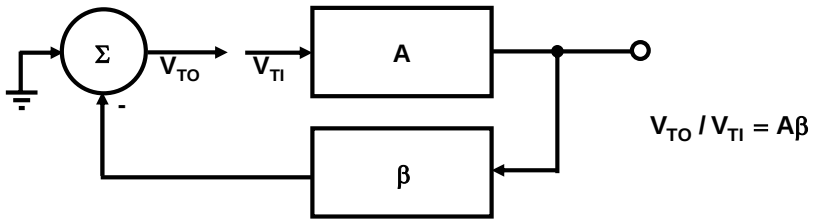
$$\frac{E}{V_{IN}} = \frac{1}{(1 + A\beta)}$$

All feedback circuits, regardless of complexity, can be reduced to this simple loop. Summers can be added along with noise inputs, and more feedback loops can be added, but the resultant circuit can always be reduced to this simple loop. Notice that the error is inversely proportional to the loop gain $A\beta$. Notice that when $A \Rightarrow \infty$ the closed loop gain, $V_{OUT}/V_{IN} \Rightarrow 1/\beta$.

Determining Stability

$$1 + A\beta = 0$$

$$A\beta = -1 = \left| 1 \right| @ -180^\circ$$



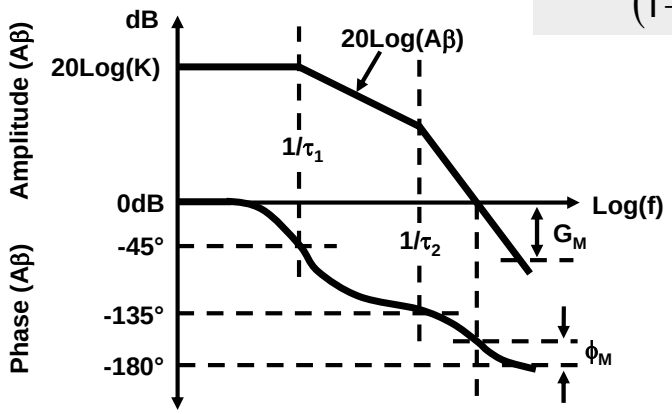
Block Diagram For Computing The Loop Gain

When the denominator becomes zero the transfer function becomes 1/0 = ∞. This is the absolute critical point for stability because the circuit oscillates at this point. The circuit overshoots and rings before it oscillates, and this behavior is shown later. The critical point is when the loop gain, Aβ, equals a magnitude of one at a phase shift of -180°. The loop gain is calculated by setting voltage inputs to zero breaking the loop, and calculating the gain. Because the inputs are zero when the loop gain is calculated they have no effect on stability.

Typical Second Order Bode Plot

where K=DC gain.

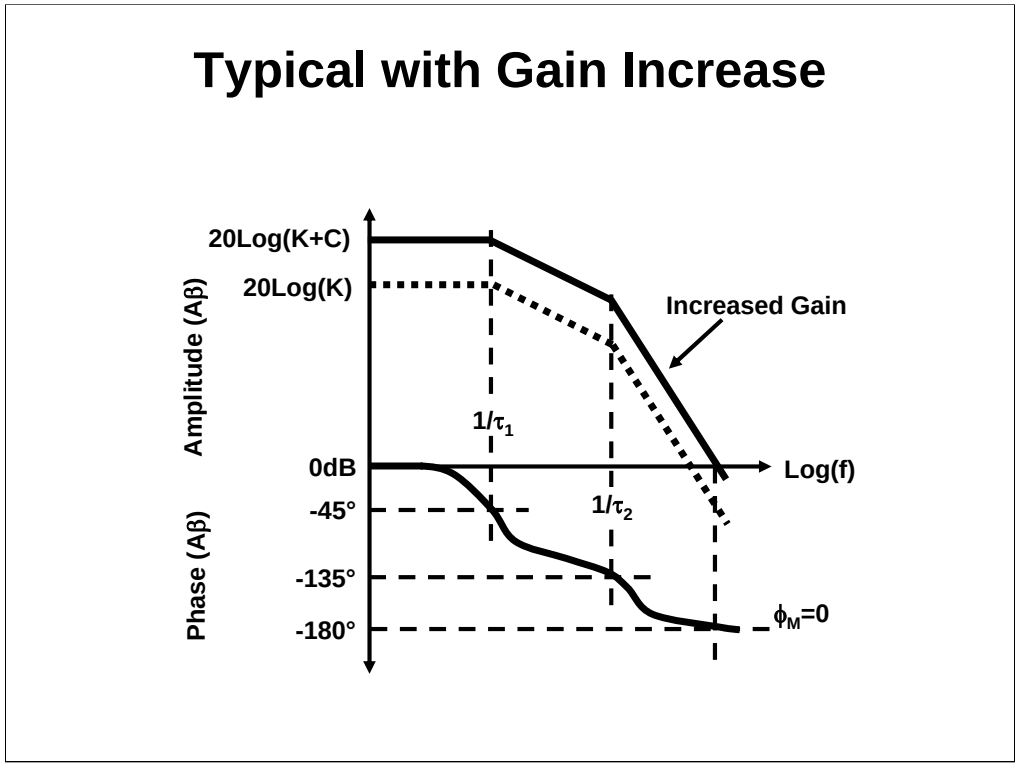
$$A\beta = \frac{K}{(1+\tau_1 s)(1+\tau_2 s)}$$



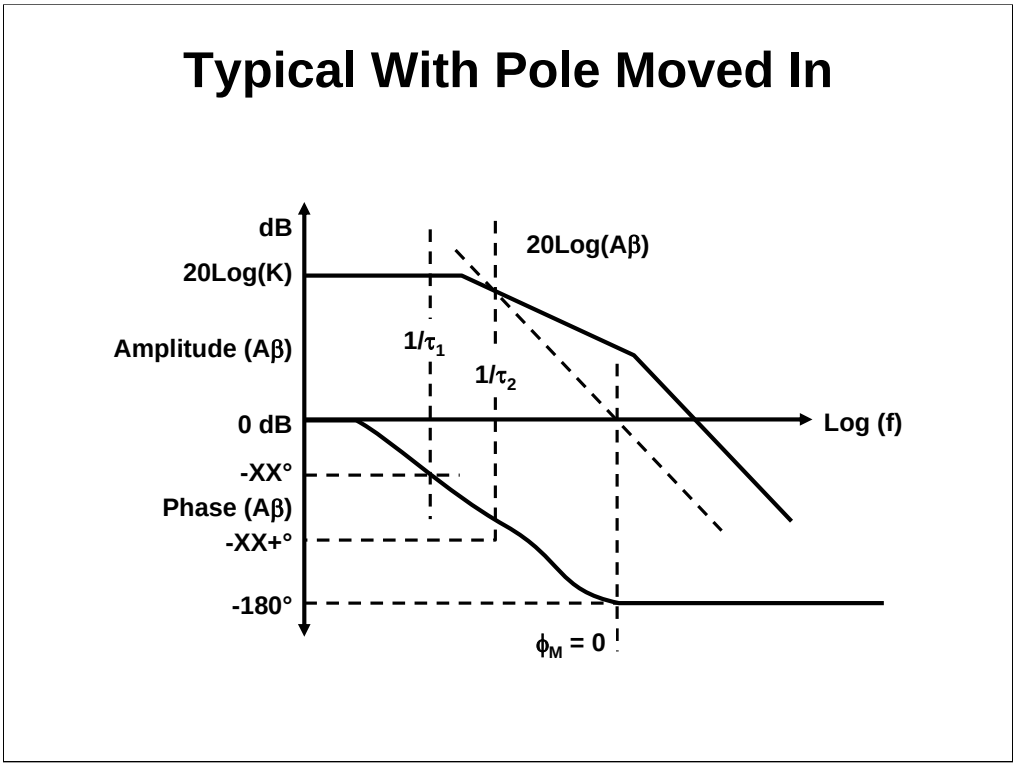
This is a plot of the loop gain of a second order system. Usually the amplifier has a dominant pole, a dc gain of K, and the second pole comes from the amplifier or the external circuits. The gain plot starts at 20 log K, and breaks down at a slope of -20 dB per decade at $\omega = 1/\tau_1$ ($s = j\omega$). The second breakpoint occurs at $\omega = 1/\tau_2$, and the gains falls off at a rate of -40 dB per octave.

The phase is a tangent function so it is not a linear function of frequency; rather it is zero at a decade earlier than the breakpoint, -45^o at the breakpoint, and -90^o at a decade past the breakpoint. Because the phase shift is 45^o at the first breakpoint we know that no phase shift from the second breakpoint has added to it, thus there must be at least a decade in frequency separating the breakpoints.

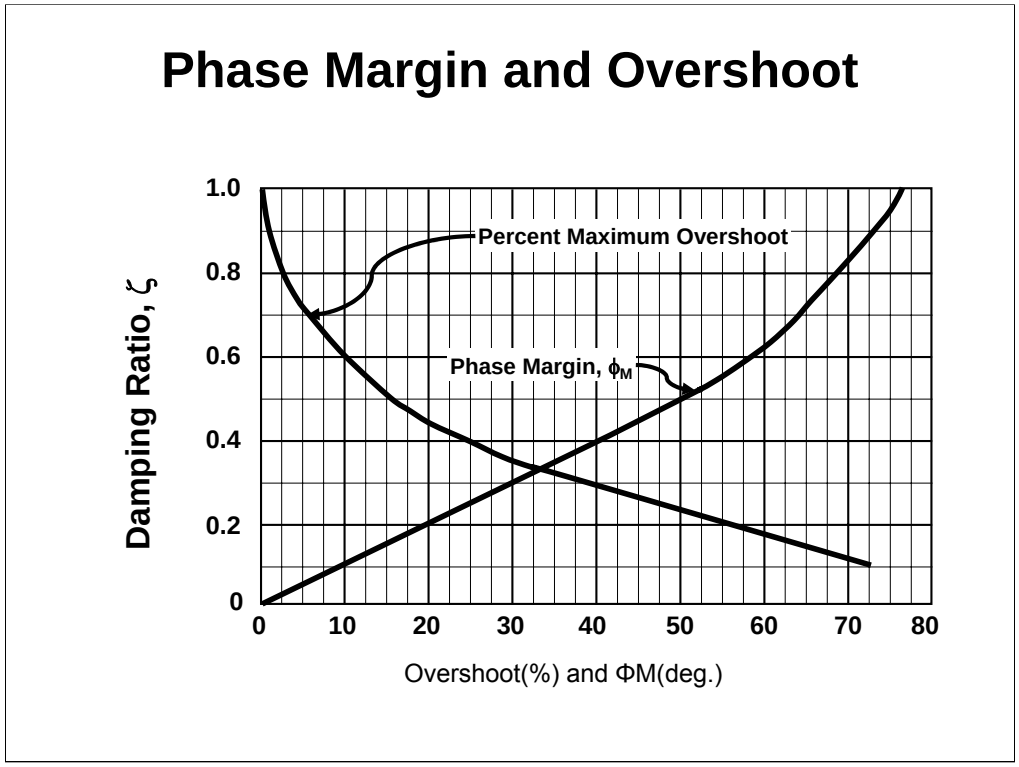
When the gain passes through 0 dB one criteria for non-oscillation is met, hence the phase shift at this point is critical. The phase shift difference between -180^o and the actual phase shift at the o dB crossover is so important that it is given a special name, the phase margin, ϕ_M.



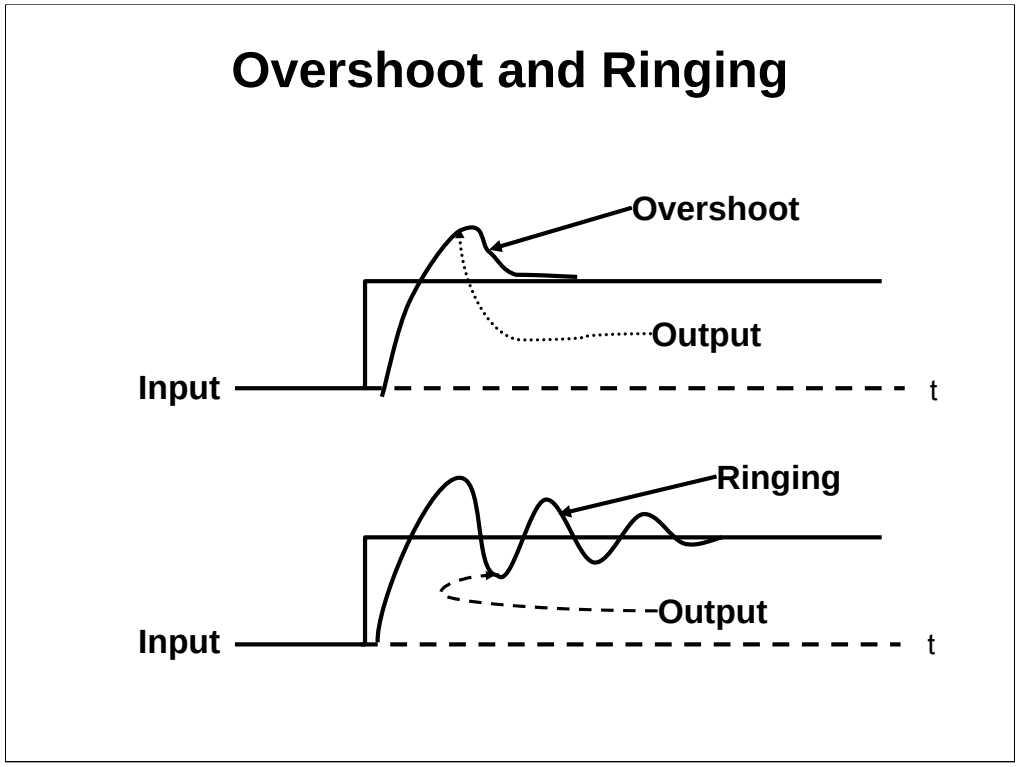
When the loop gain is increased from K to K+C it moves up the amplitude axis and the 0 dB crossover point moves out to a higher frequency. Remember that the error is inversely proportional to the loop gain, so these two parameters play against each other; improve error and stability suffers, and vice versa.



Pole location is critical to its effect on stability. When the two poles are moved nearly on top of each other the rate of phase shift accumulation accelerates rapidly. When the pole is at very low frequencies it rolls the gain off before the second pole comes into play. If the second pole is at a very high frequency the gain is very low so it has little effect on stability. Keep poles widely separated for stability purposes, and if you can't separate poles cover the second pole with a zero.



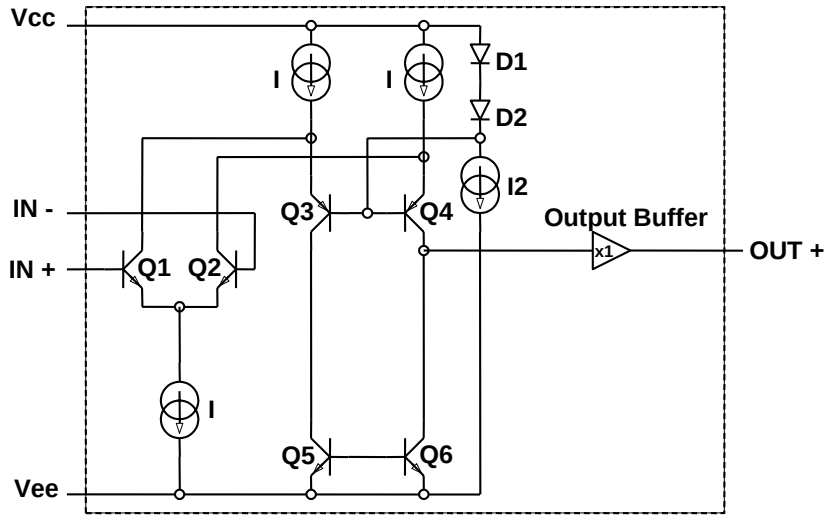
Phase margin is a critical parameter for gauging stability. Unless you are designing oscillators, the phase shift is kept to less than -180°, but how determining much less is the problem. As the phase shift of a two pole system approaches -90° the system gets very slow because it approximates a single pole system. The tradeoff for phase margin is overshoot, and the plot connects the two parameters through a dummy variable, ζ. The math for this plot can be obtained from Del Toro and Parker; a 1960's controls textbook. Enter the graph at 2.5% overshoot and go up until you intersect the percent maximum overshoot line, then go across at a steady damping ratio of 0.8 until you intersect the phase margin line, and drop down to the phase margin of 69°. Conversely, you can enter the graph at 45° phase margin, rise up to the 0.45 damping ratio line, cross over to the percent maximum overshoot line, and drop down to read 18% overshoot.



Overshoot is less pronounced ringing, and they result from pole placement. If you imagine a two pole plot, when the poles are located on the resistance axis the response time is similar to a single pole circuit that has 90^{o} phase shift. As the poles moves from the resistive axis to the imaginary axis the response time gets faster but the overshoot increases. At some point the overshoot exceeds one cycle and is termed ringing. The ringing increases with the pole movement towards the imaginary axis until they reach the imaginary axis where oscillation starts.

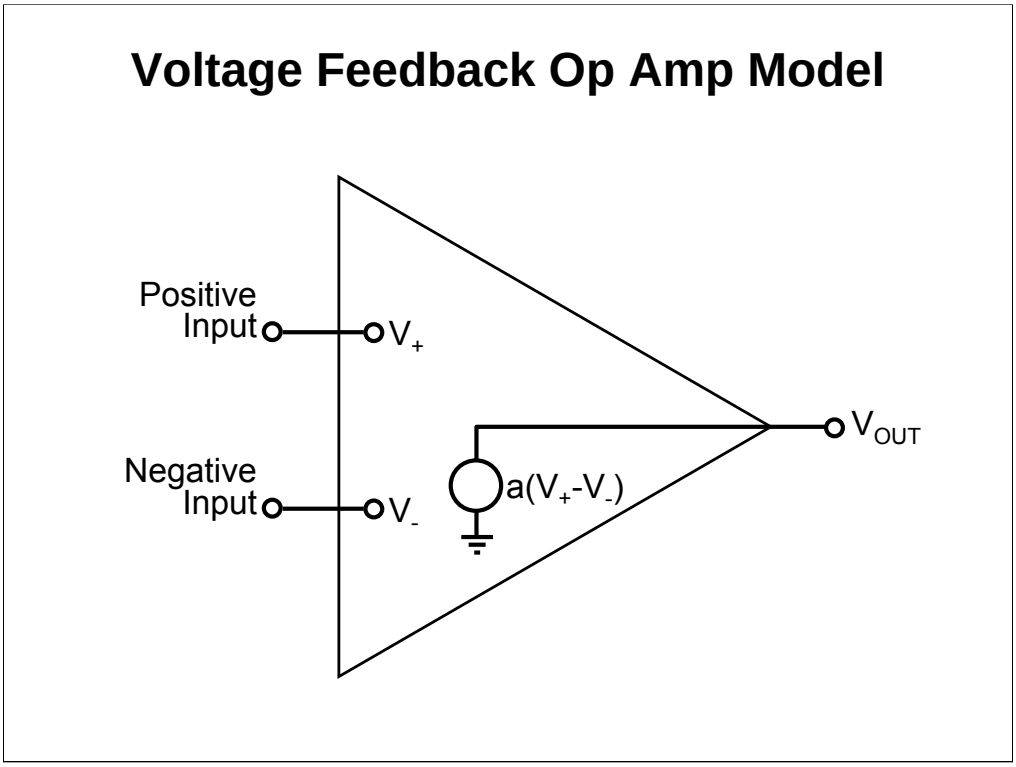
Voltage Feedback Op Amp Analysis

Standard Voltage Feedback Operational Amplifier



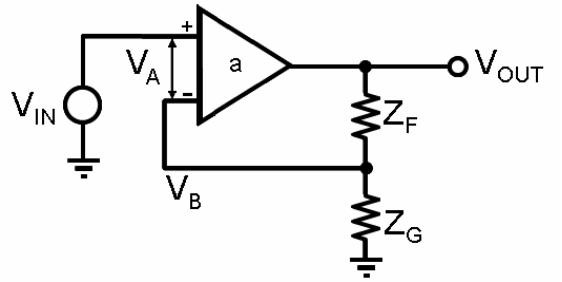
The VFA input circuit is a long tailed differential transistor pair. If both transistors are matched their currents are equal, and this being the case increasing both base voltages an equal amount does no cause a differential signal. The transistor matching give the circuit its inherent precision, and circuit designers have become very adept at the matching. When they can't match with the required precision they laser trim, blow links or use some other method to obtain the precision desired.

The collector current of Q_4 is limited by its emitter current source, I, thus regardless of the input signal amplitude the collector capacitor of Q_4 and the current, I, limit the slew rate according to this equation dV/dT = I/C. Two conclusions can be drawn here: the VFA is a precision device, and its slew rate is limited by its internal design.



For our purposes, no input current flows, no power supply rail limitations exist, and the gain is infinite.

Non-Inverting Op Amp



$$V_{OUT} = a(V_{IN} - V_B)$$

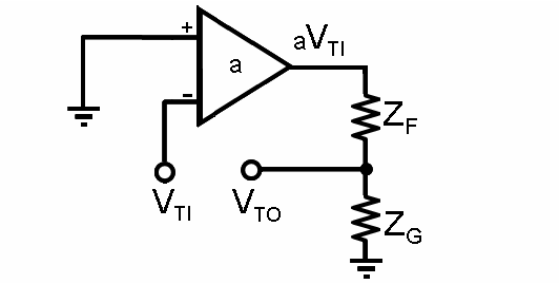
$$V_B = \frac{V_{OUT} Z_G}{Z_F + Z_G}$$

$$V_{OUT} = aV_{IN} - \frac{aZ_G V_{OUT}}{Z_G + Z_F}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}}$$

The output equation is written from inspection. V_B is obtained by the voltage divider rule because $I_{IN} = 0$. Combining those equations yields the closed loop equation which has the same form as the basic feedback equation. Thus, we can pick out $A\beta = aZ_G/(Z_F+Z_G)$. The loop gain is independent of the inputs, so this loop gain is valid for the inverting op amp circuit.

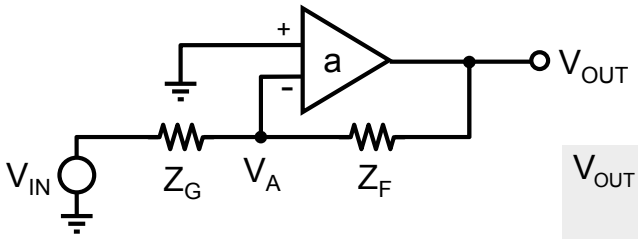
Op Amp-Loop Gain Calculation



$$\frac{V_{TO}}{V_{TI}} = \frac{aZ_G}{Z_G + Z_F} = A\beta$$

We can obtain the loop gain by grounding the input signal, breaking the loop, and calculating the transfer function. Notice, it doesn't matter what method you use to calculate the loop gain.

Inverting Op Amp



$$V_{OUT} = -aV_A$$

$$V_A = \frac{V_{IN}Z_F}{Z_G + Z_F} + \frac{V_{OUT}Z_G}{Z_G + Z_F}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{-aZ_F}{Z_G + Z_F}}{1 + \frac{aZ_G}{Z_G + Z_F}}$$

The dummy variable, V_A, is calculated with the aid of superposition. Notice that the loop gain is still the same.

Inverting and Non-Inverting VFA Comparisons

- Non-Inverting

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1+\frac{aZ_G}{Z_G+Z_F}} = \frac{Z_F+Z_G}{Z_G}$$

- Inverting

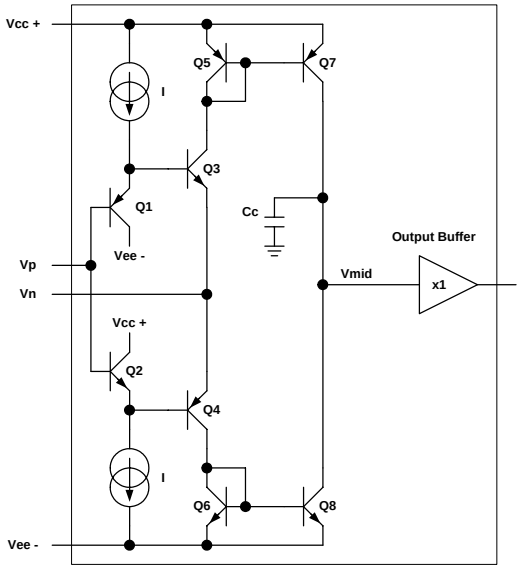
$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{-aZ_F}{Z_G+Z_F}}{1+\frac{aZ_G}{Z_G+Z_F}} = -\frac{Z_F}{Z_G}$$

(Simplified equation is for a>>1)

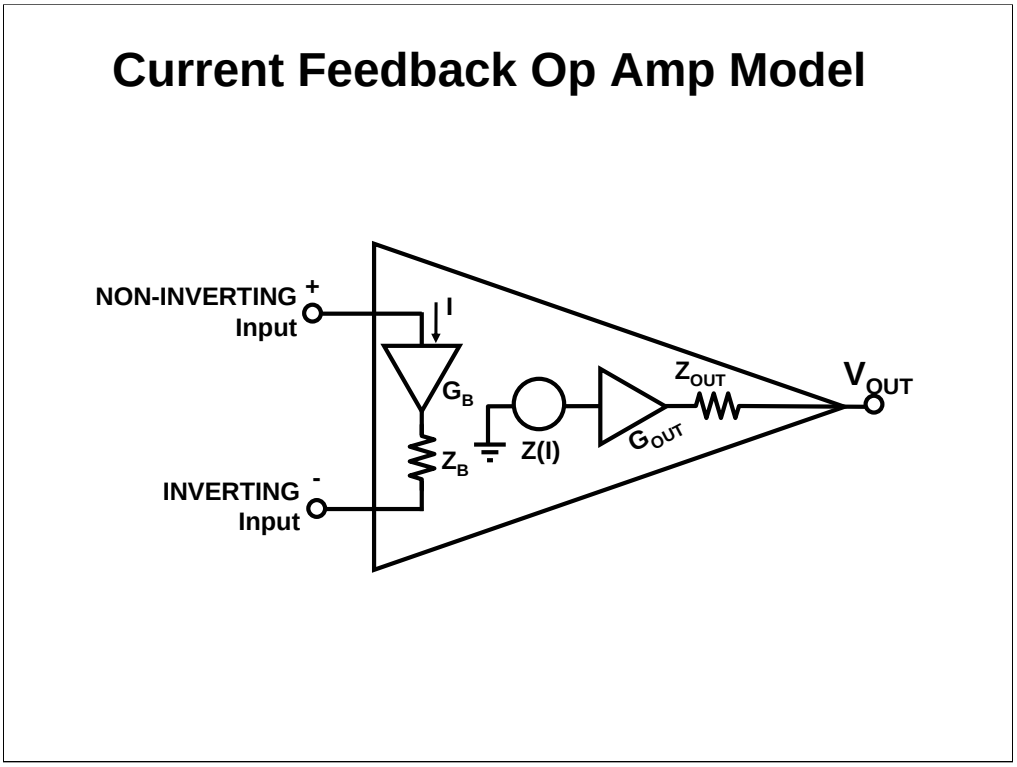
A comparison of the transfer equations shows that the loop gain stays constant.

Current Feedback Op Amp Analysis

Simplified CFB Op Amp Schematic

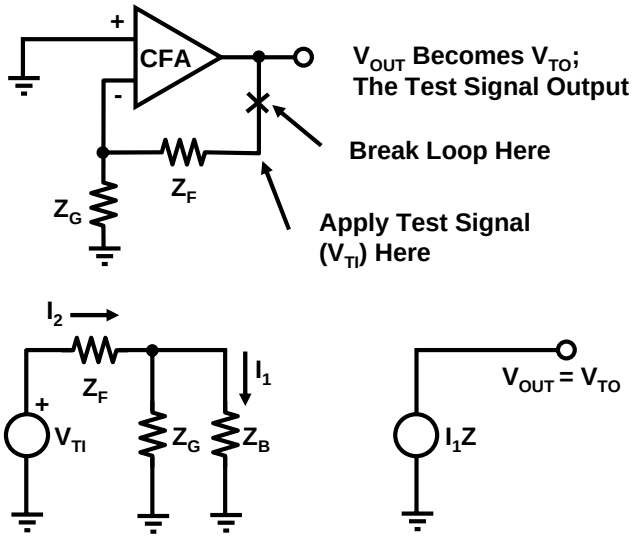


The non-inverting input is connected to a buffer input, and the inverting input is connected to a buffer output, so the inputs can't be matched very well. This means that the CFA never achieves the high precision available from the VFA. The input buffer output impedance is very low, from 25 to 100 ohms, so it does not limit the input current very much. The input current equation is $V_{IN+}/ (Z_B+R_{EXT})$, and this current could be several hundred mA. The input current contributes to the slewing current, thus the CFA is not internally slew rate limited. Z_B is a secondary term, but it can't be neglected, while Z_{OUT} is always neglected.



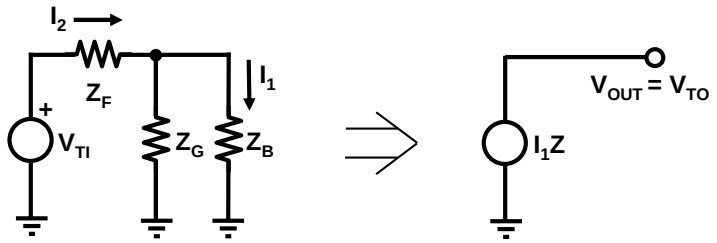
The input current is instantaneous and mirrored to the output stage. The input buffer's output impedance does have a secondary effect on the CFA's performance, so it is included in the calculations. The output buffer's out put impedance gets divided by the transimpedance, so it is neglected. Both buffers are assumed to have a gain of one. .

Stability Analysis Circuit



The stability analysis is performed by breaking the loop and calculating the loop gain. Notice, when the non-inverting input Z_B is grounded through the input buffer. This completes the model for the stability analysis.

Stability Analysis



$$V_{TO} = I_1 Z$$

$$V_{TI} = I_2(Z_F + Z_G \,||\, Z_B)$$

$$I_2(Z_G \,||\, Z_B) = I_1 Z_B; \text{ For } G_B = 1$$

$$V_{TI} = I_1(Z_F + Z_G \,||\, Z_B)\left(1 + \frac{Z_B}{Z_G}\right) = I_1 Z_F\left(1 + \frac{Z_B}{Z_F \,||\, Z_G}\right)$$

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{Z_F\left(1 + \frac{Z_B}{Z_F \,||\, Z_G}\right)}$$

The equations for the stability analysis are written here. The loop gain is determined by the transimpedance divided by the feedback resistor with a secondary term caused by the presence of Z_B. If $Z_B = 0$ then $A\beta = Z/Z_F$, and the stability is controlled by R_F. The loop gain is completely separated from the closed loop gain under this assumption. Normally Z_B is approximately 50Ω, $R_F||R_G$ is approximately 500Ω, so Z_B causes a 10% error.

VTO = I1Z

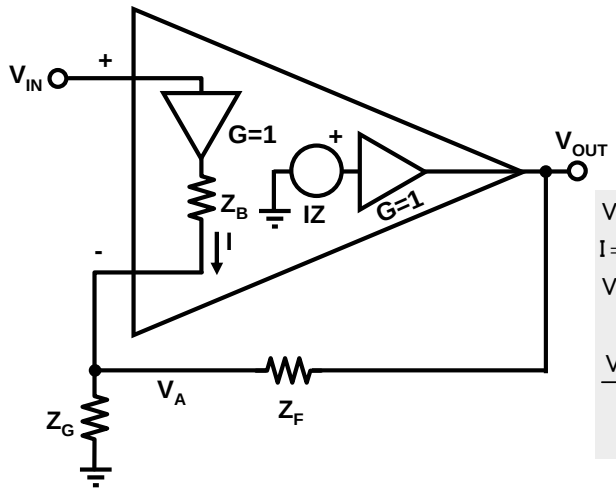
VTI = I2(ZF+ZG||ZB)

I2(ZG||ZB) = I1ZB; For GB = 1

VTI = I1(ZF+ZG||ZB)(1+ZB/ZG)=I1ZF (1+ZB/ZF||ZG)

Aβ = VTO/VTI = Z/(ZF(1+ZB/ZF||ZG))

Non-Inverting Op Amp

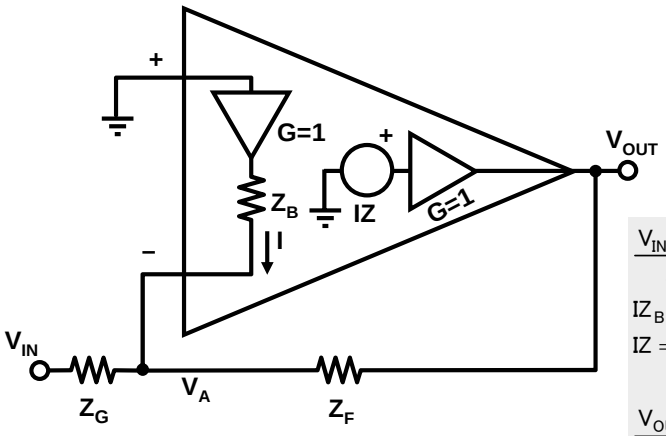


$$V_{OUT} = IZ$$
$$I = (V_A/Z_G) - (V_{OUT} - V_A)/Z_F$$
$$V_A = V_{IN} = IZ_B$$
$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z(1 + Z_F/Z_G)}{Z_F(1 + Z_B/Z_F \| Z_G)}}{1 + \frac{Z}{Z_F(1 + Z_B/Z_F \| Z_G)}}$$

Calculating the transfer equation for the non-inverting circuit starts with the output equation. Then the current equation for the V_A node is written. Finally, an equation is written for the dummy variable, V_A. Again, the loop gain can be picked out of the closed loop gain when it is written in standard format, and the loop gain equals that obtained with the open loop procedure.

Z_F is critical for stability.

Inverting Op Amp



$$\frac{V_{IN} - V_A}{Z_G} + I = \frac{V_A - V_{OUT}}{Z_F}$$

$$IZ_B = -V_A$$

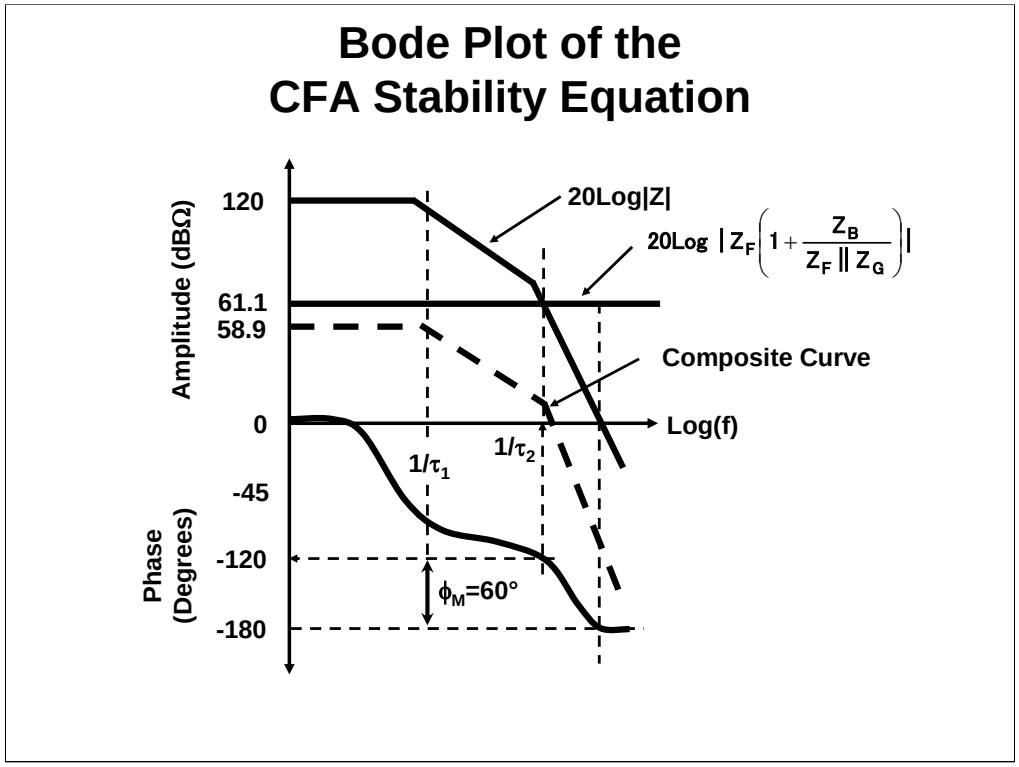
$$IZ = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\frac{Z}{Z_G\left(1 + Z_B/Z_F \| Z_G\right)}}{1 + \frac{Z}{Z_F\left(1 + Z_B/Z_F \| Z_G\right)}}$$

Used only when driving a very low impedance

The equation development for the inverting circuit is left to the reader.

Z_F is critical for stability.



The log loop gain plot consists of drawing the transimpedance line and the modified feedback resistance line. Graphically subtract the feedback resistance from the transimpedance to get the composite curve. The poles are independent of the transimpedance (or gain), so when the feedback resistance is increased the composite curve moves down, and the 0 dBΩ crossover point moves to the left yielding increased stability at a sacrifice in bandwidth. When the feedback resistance decreases the composite curve moves up, bandwidth goes up, and stability is decreased.

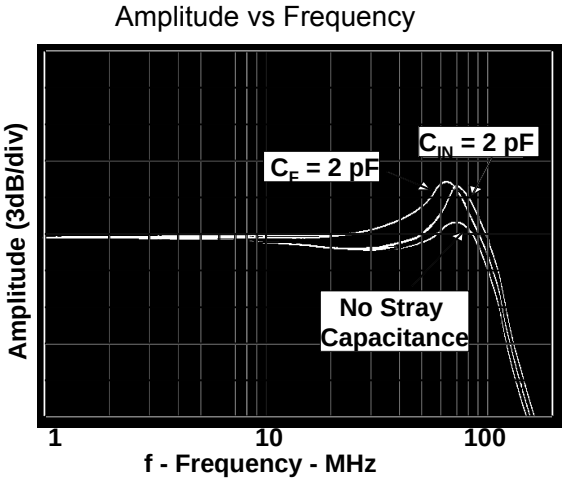
Input Buffer Output Impedance

- h_{ib} = 50Ω, R_B / (β_0 +1) = 25Ω, Z_B = 75Ω
- Z_B approaches h_{ib} + R_B / β_0
- β_{PNP} is not equal to β_{NPN}

$$Z_B = h_{ib} + \frac{R_B}{\beta_0 + 1}\left(\frac{1 + S\beta_0/\omega_T}{1 + S\beta_0/(\beta_0 + 1)\omega_T}\right)$$

The input buffer output impedance is completely dependent on semiconductor parameters. So it varies with process and temperature, and is not a dependable value.

Stray Capacitance in CFAs



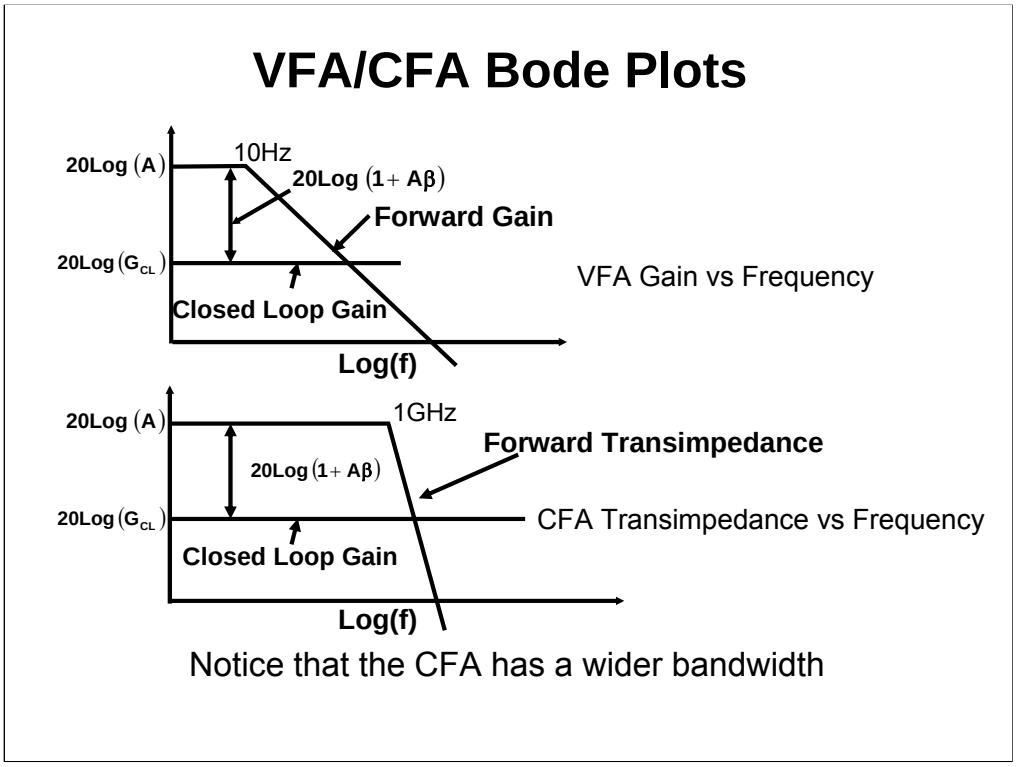
Because of its extremely high bandwidth and sensitivity to feedback resistance, the CFA is extremely sensitive to stray capacitance. Just 2pF of input or feedback capacitance causes 3dB peaking in the output.

CFB versus VFB

VFA and CFA Comparison

	VFA	CFA
Precision	Highest	
Speed		Highest
Slew Rate		Highest
Sensitivity to stray capacitance	Less	More
Input Impedance	Balanced	Unbalanced
Limitations	Constant GBW	
Stability Control	RF+RG	RF

The VFA input stage is a differential amplifier constructed from a long-tailed pair consisting of emitter connected input transistors fed by a common current source. This construction is symmetrical thus it inherently lends itself to precision performance by virtue of matching. The CFA inputs connected to a buffer input and output, thus it is impossible for the CFA to take advantage of matching. The CFA inputs are at dramatically different impedance levels because they are connected to the input and output of a buffer, and this situation precludes operation as a differential amplifier.



The scales for the two amplifiers are dramatically different, thus while it looks like the CFA is rolling off at a faster rate it still rolls off at -20 dB/decade. Designers work on the slope of the VFA curve because the flat potion is so small (10Hz for a 1MHz GBW device). This puts the designer in the uncomfortable position of introducing a small non-linear error into the system because the forward gain changes with frequency in the sloped portion of the curve. The CFA is used in the flat portion of the forward gain curve so it has slightly less distortion. The GBW of a CFA is often much greater than needed, and this excess gain amplifies noise or contributes to instability, thus experienced engineers sometimes increase the feedback resistance to lower the GBW to slightly more than required.

Stability

VFA Stability equation: $$A\beta = \frac{aZ_G}{Z_F + Z_G}$$

VFA stability is dependent on R_F and R_G.

CFA stability equation: $$A\beta = \frac{Z}{Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)}$$

CFA stability is dependent on R_F.

Both stability equations are the circuit loop gain equations, $A\beta$, but the value of $A\beta$ is different for each circuit because the VFA and CFA internal circuitry is different. The VFA stability equation contains R_F and R_G, both of which determine the closed loop gain. Thus, there is no way to change the VFA closed loop gain without impacting the stability.

The CFA stability equation only contains R_F (when R_B is neglected), so R_F is the only external component that determines stability. This gives the CFA another degree of freedom because R_F can be adjusted for stability without affecting the closed loop gain. Also, there is always a value of R_F that stabilizes the circuit. Any capacitance in parallel with R_F destabilizes the circuit because the capacitive impedance decreases to an unstable value at high frequencies. This is why a feedback capacitor should not be used with a CFA.

VFA and CFA Gain Equations

Circuit Configuration	Current Feedback Amplifier (CFA)	Voltage Feedback Amplifier (VFA)
Closed Loop Gain NONINVERTING	$1+\frac{Z_F}{Z_G}$	$1+\frac{Z_F}{Z_G}$
Ideal Loop Gain	$\frac{Z}{Z_F}\left(1+\frac{Z_B}{Z_F \parallel Z_G}\right)$	$\frac{aZ_G}{(Z_G+Z_F)}$
Closed Loop Gain INVERTING	$-\frac{Z_F}{Z_G}$	$-\frac{Z_F}{Z_G}$

The ideal closed loop gain equations for the CFA and VFA are identical. The VFA assumes that the op amp gain, a, is very large to arrive at the ideal closed loop gain equation. The CFA arrives at the ideal closed loop gain equation by assuming that the transimpedance, Z, is very large and the input buffer output impedance, R_B, is very small.

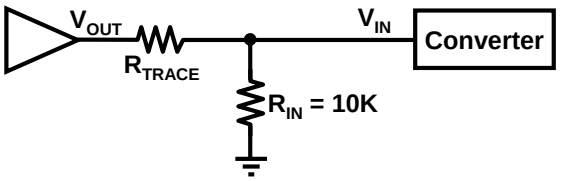
Practical Analog Design

Section—3

Signal Integrity

This section presents the time honored motherhood and apple pie information about grounding and power distribution, but this information is backed up by the supporting detail. Rather than just tell you what to do, we show you how to do it.

PCB Trace Resistance



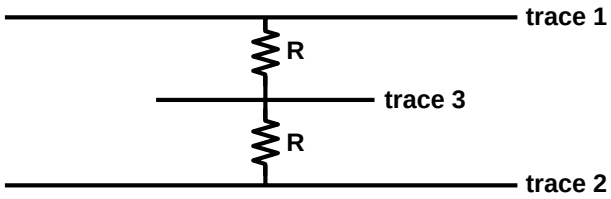
- R_{TRACE} is approximately 0.1Ω when the trace is 2.5 inches long

$$V_{IN} = \frac{R_{IN}}{R_{TRACE} + R_{IN}} = 0.99999$$

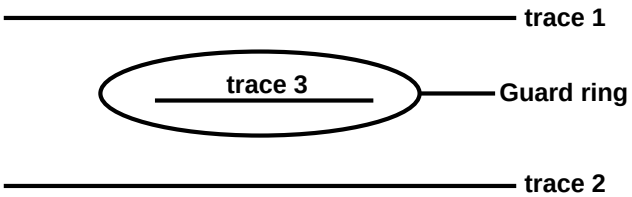
  Error = 1-0.999 = 0.00099%
- Can't achieve 18 bits accuracy
- *KEEP TRACES SHORT*

Pay attention to detail! A small trace resistance can preclude 18-bit accuracy. The trace resistance can be adjusted out, but because of dissimilar materials a temperature drift occurs that can accumulate to 18-bits over the temperature range. Long input traces are always susceptible to problems, so they should be avoided whenever possible.

Beware of Leakage Currents



- Surface currents flow from both adjacent traces to trace 3



- Guard rings minimize leakage currents

Trace 3 carries a high impedance signal, and R is the board leakage resistance between traces 1 or 2 and trace 3. Although steps can be taken to minimize the leakage resistance, it can never be eliminated. One trick is to guard trace 3 with a guard ring trace. Now if the guard ring is connected to the proper potential the leakage current flows into the guard ring rather than trace 3. Where should the guard ring be connected? Connect the guard ring to the lowest potential to start, and if that doesn't solve the problem, try connecting the guard ring to other potentials. The guard ring must intercept the leakage path, and the physical dimensions and voltage determine the leakage path, so it is virtually impossible to know where to connect the guard ring without knowing the leakage path. Guard rings require multiple layer boards and are hard to implement, so they are used sparingly.

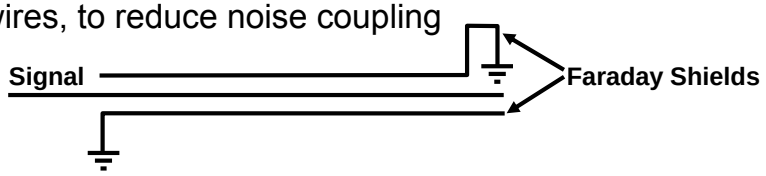
Stray Capacitance

- Trace-to-trace or trace-to-ground plane
- Couples noise onto signal lines
- Reduces bandwidth or causes oscillation
- Remove ground plane under critical nodes
- Short narrow traces
- No parallel traces (IC wire bonds)

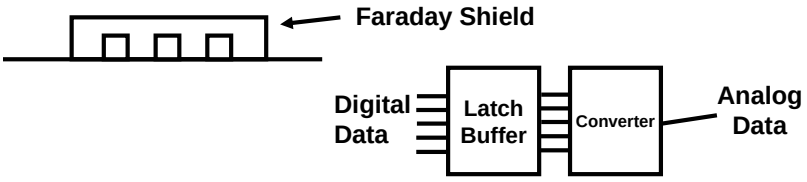
Stray capacitance is any capacitor made without intention. Since any two plates separated by a dielectric material constitutes a capacitor, stray capacitance is found everywhere. Two parallel traces on a circuit board form a capacitor, and noise can jump from one trace to an adjacent trace. This is another good reason to keep traces short. Feedback capacitors formed by ground plane under a feedback resistor kill the circuit's high frequency response. Inverting input node capacitance introduces another pole into Bode plot thus making the circuit ring or become unstable. Removing or decreasing the size of one plates decreases the stray capacitor's value.

Faraday Shields

- Run wires with one end grounded, parallel to signal wires, to reduce noise coupling



- Metal shield protects critical circuits from radiation and latch buffer acts as a Faraday shield for radiated signals



Sometimes it is impossible to prevent signal interference by any other means than shielding. A Faraday shield traps all incoming noise and routes it to the shield potential. If you must run an analog signal trace along a course parallel to traces carrying digital signals, Faraday traces should be run next to the signal traces. Connecting the Faraday trace to the proper point eliminates noise coupling. The Faraday traces can be connected to ground, the supply, at the near end, at the far end, or at different ends, and the physics of the situation determines where you should connect them to get the best results. Metal covers act as Faraday shields against radiated noise. Bond wires have about 0.2pF wire to wire. If the digital bus is not isolated the DAC's digital input noise will couple from across the bond wires to the output.

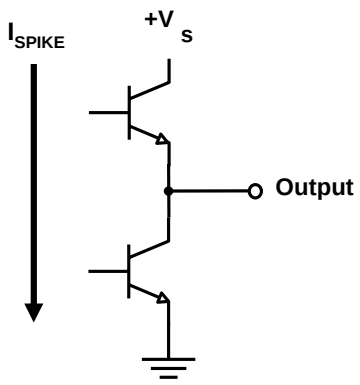
Decoupling Capacitors

- Noise is generated by logic circuits
- Decoupling capacitors prevent noise from propagating into the power supply
- Use a good grade of capacitor
- Capacitors must have short leads
- Surface mount capacitors are best
- One on each IC; two if it is a big digital IC

Decoupling capacitors circulate noise at the source. If the logic circuits are not decoupled the ground trace on a scope picture will have so much noise on it that it will look like a fuzzy line. Be generous with decoupling capacitors.

Saturated Logic Generates Noise

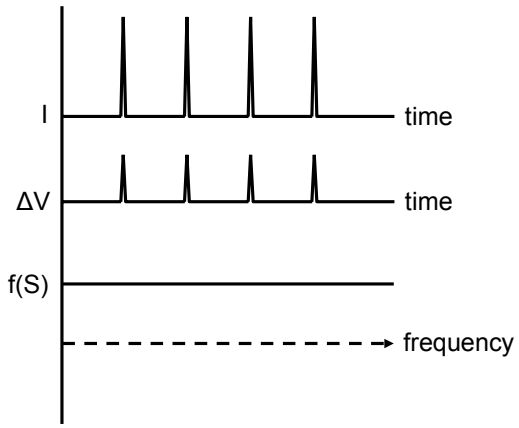
- Transistors on simultaneously causes current spike
- All Logic does this
- Up to 70mA spike
- Current spikes are fast (nS) approaching an impulse



The totem pole output of saturated logic circuits, including CMOS, generates a current spike every time it is switched. This is required because current must be maintained in the load to prevent line reflections. The current spike finds its way from ground back to the 5V supply by the path of least resistance, and that path surly will be common to an amplifier thus causing noise injection. When many loads are switched simultaneously, like in a display or bus driver, the current spikes accumulates into one big spike. When TTL is switched asynchronously the multitude of current spikes spread out and make the ground reference look fuzzy on an oscilloscope.

Current Spikes are Broadband

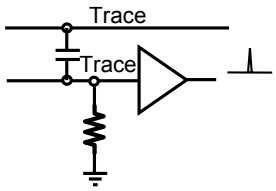
- Switching multiple gates multiplies the current spike
- A current spike plots flat in frequency spectrum
- Current spikes cause voltage drops across distributed power impedance

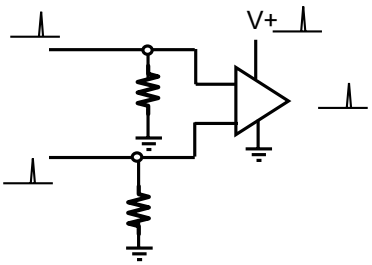


Current or voltage spikes approximate an impulse function in the time domain, thus they plot as a flat line in the frequency domain. This means that these spikes will interfere with any receiver they find, and PC traces make excellent receivers. The current spikes drop voltage across the distributed impedance of the power system, so they show up on all parts of the power system as voltage spikes unless they are constrained to a very short path at the source.

Noise Propagates in Power Distribution

- Spikes slip through stray capacitance
- PSR of op amps cannot reject voltage spikes efficiently
- CMR of op amps cannot reject voltage spikes efficiently

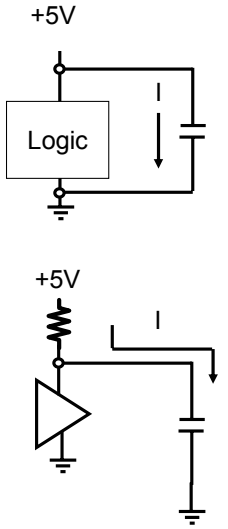




The voltage spikes are coupled to the signal system from ground or 5V by stray capacitance. Two methods of reducing this effect is to reduce the noise or to reduce the stray capacitance. The amplifier power supply rejection (PSR) capability helps reduce the noise coupled from the supplies, but the noise contains high frequency components and PSR falls off at high frequencies. When the noise is on ground it becomes common mode noise, and the amplifier rejects it through its common mode rejection (CMR) capability, but again the high frequency component of the noise is not rejected as well because CMR decreases with increasing frequency.

Noise Suppression

- Decoupling capacitor at logic IC leads circulates the current spike at the IC keeping it out of ground
- Decoupling capacitor at op amp improves PSR-RC filter is better



Adding a decoupling capacitor adds a local path for the totem pole transistor current spike to circulate close to the source. The decoupling capacitor keeps the noise localized to the IC that generates the noise. The size of the decoupling capacitor is determined by the equation I=C(dV/dT) where I is the magnitude of the current spike, dV is the maximum allowable voltage spike amplitude, and dT is the width of the spike (about 2 nS). This usually works out to one 0.1μF for a 16 pin IC and two capacitors for bigger ICs.

The spikes are on the power lines, and PSR doesn't do a really good job of rejecting them, so adding a decoupling capacitor to the amplifier helps reduce the effects of noise. The decoupling capacitor works against the supply impedance to act as a low pass filter, and if the filter action is not great enough, increase the decoupling capacitor or add a small resistor (10 to 51Ω) in series with the supply.

Choose Decoupling Capacitor Dielectric Carefully

- Sized by I = C(dV/dT)
- All capacitors have self resonance
- Impedance increases after the self resonant point
- Apparent capacitance decreases 10% at this frequency

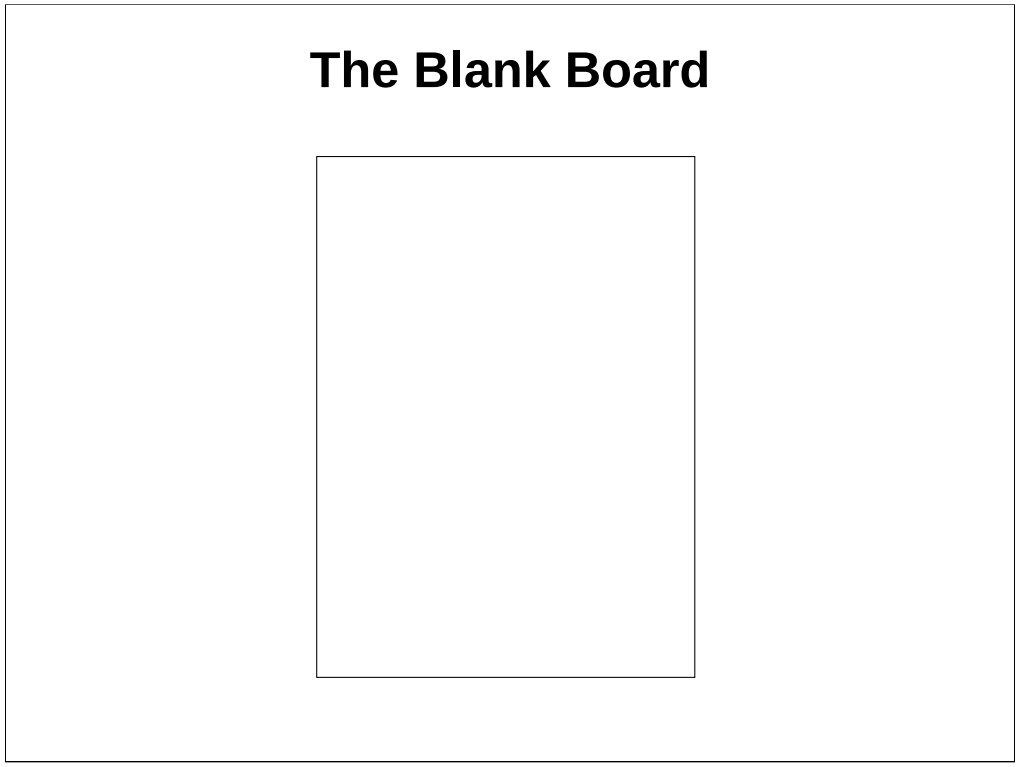
Dielectric	MHz
Alu-Ele	N/A
Tantalum	0.002
Titanates	1
Ceramic	10
Glass	100
Mica	100
NPO	100

The dielectric determines a capacitors effectiveness or equivalent capacitance at high frequencies. Notice that an aluminum-electrolytic capacitor is worthless at high frequencies, and that ceramic disc capacitors are only good to 10MHz.

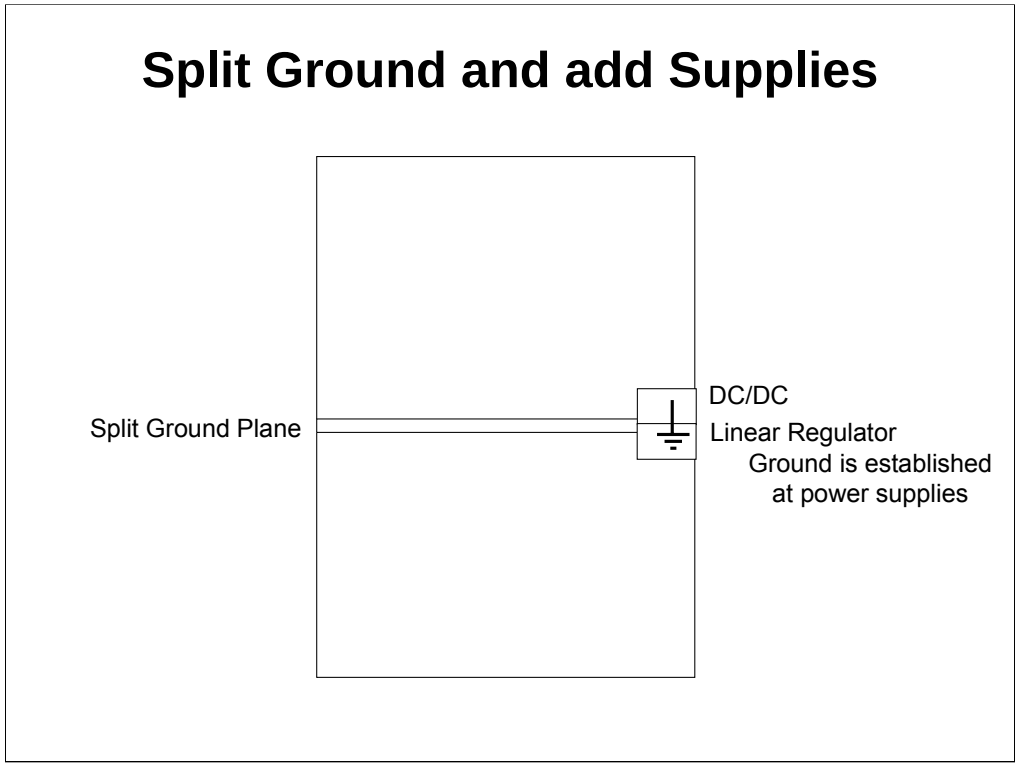
Route Signals Wisely

- Keep signal and return together to prevent single ended noise
- Prevent loops which can become transformers
- Route analog and digital signals separately
- Beware of cables
  - Mutual inductance, capacitive load, and crosstalk

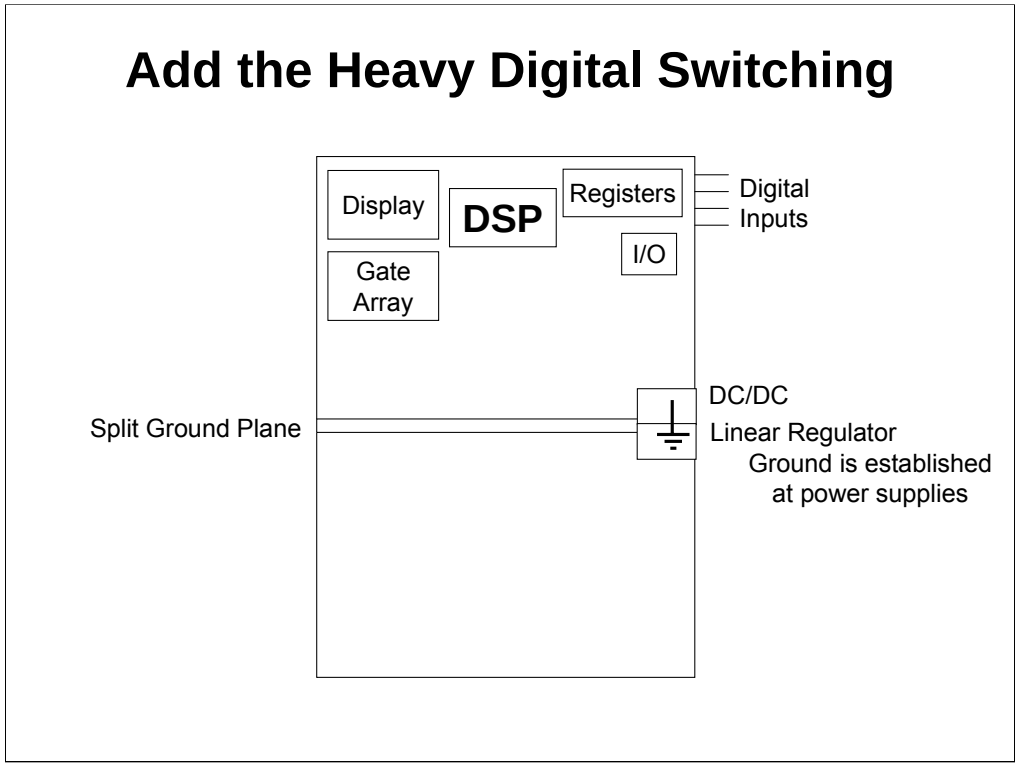
Successful signal routing doesn't just happen; it is planned from the beginning of the design. Although there are some basic principles that help gain success, they are best explained with a sample circuit.



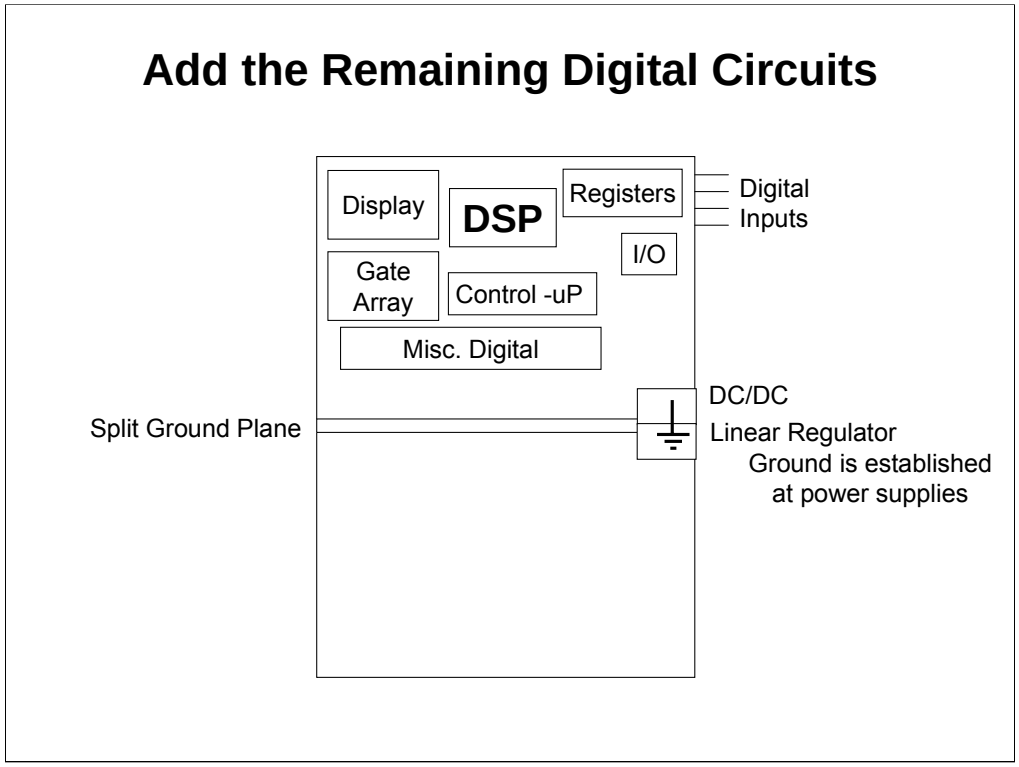
This is the blank board that is going to be used for the design. Normally, board orientation is determined by human factors and the connectors, so the circuit designer has to accept the board outline and orientation. The first decision concerns the number of layers because costs increases with the number of layers, while noise and layout problems decrease with the number of layers. Should the ground plane be split into analog and digital sections (notice, a plane is assumed), or should the grounds be kept common?



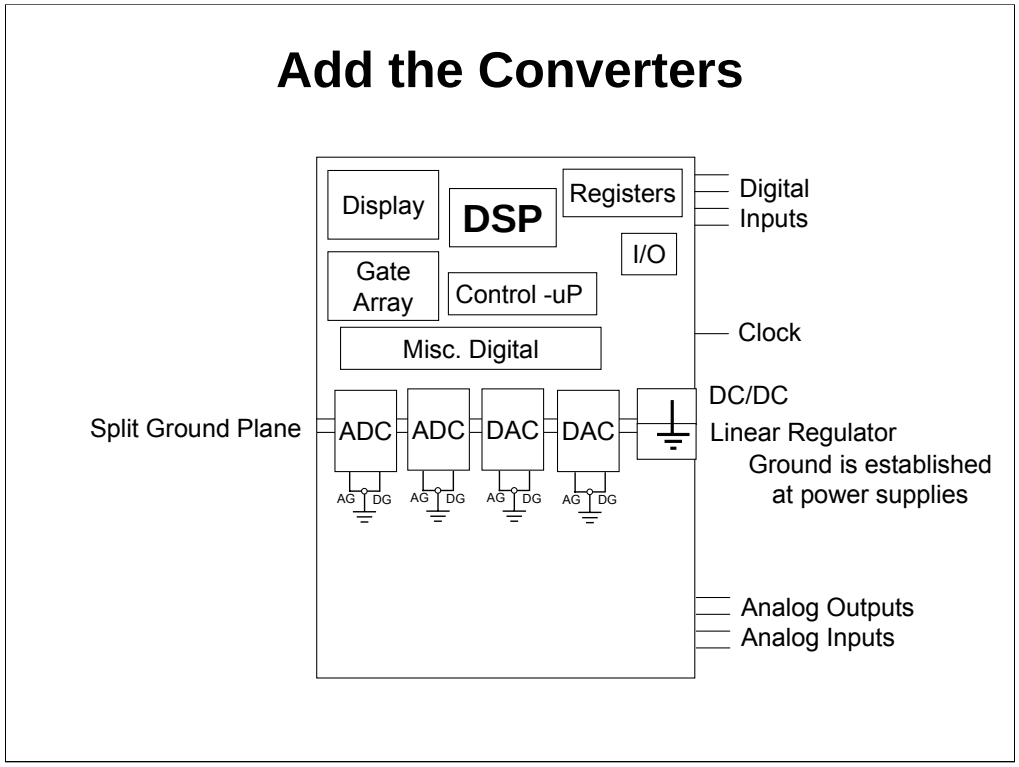
Splitting the ground plane minimizes the digital noise propagation into the delicate analog signals. A split ground plane design can always be turned into a whole ground plane design, but the reverse is almost impossible without starting over. The split propagates from the power supplies across board. The dc/dc converter is located in the digital half of the ground plane because it is noisy, and the linear regulator is located in the analog half of the ground plane because it is less noisy. The ground plane that is left in the power supply area is the connection between the digital and analog grounds and is sometimes called main system ground. This crucial part of the ground plane is marked with a ground sign.



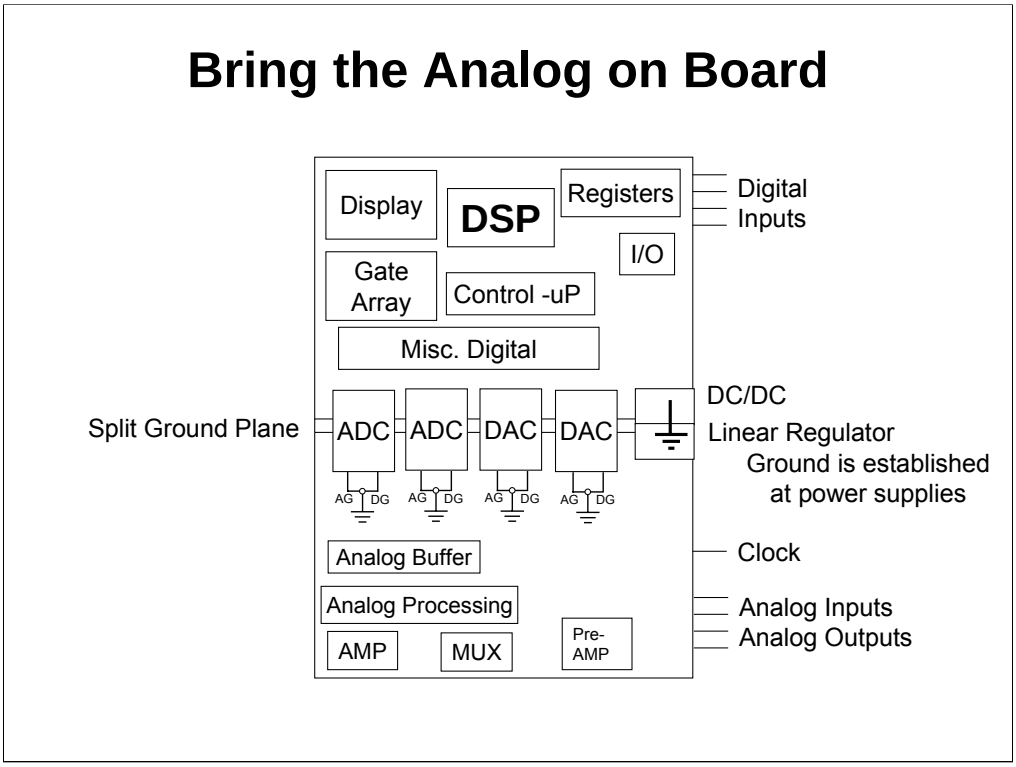
High current, high speed, high repetition rate, and fast switching ICs are placed at the farthest point from the delicate analog signals because distance is the enemy of noise. The digital inputs for these circuits are kept near the circuits and away from the analog circuits.



The remaining digital circuits are added to the board. When the circuits are added signal flow is kept in mind. The digital inputs should flow naturally to the circuits they control, and the digital I/O for the converters should flow to the center of the board. Now provisions must be made for digital outputs from the digital circuits and the D/A.



The converters are added somewhere in the middle of the board between the analog and digital circuits. The converters may or may not straddle the split in the ground plane. Each converter has an analog ground lead and a digital ground lead, and these leads must be connected together at the converter IC to establish a good ground for the converter. There are two different ground leads on converters because the IC can't make a low enough internal resistance connection to function correctly. The converter analog ground and digital ground leads should be connected to analog ground. This does cause some digital current to flow in the analog ground, but you can control this current and decouple the converter heavily. This causes the converter to lose a few mV of digital noise immunity, but the digital circuits can spare it because they have several hundred mV of noise immunity. Connecting the converter digital ground to the analog ground keeps the analog ground plane intact and separate from the digital ground plane.

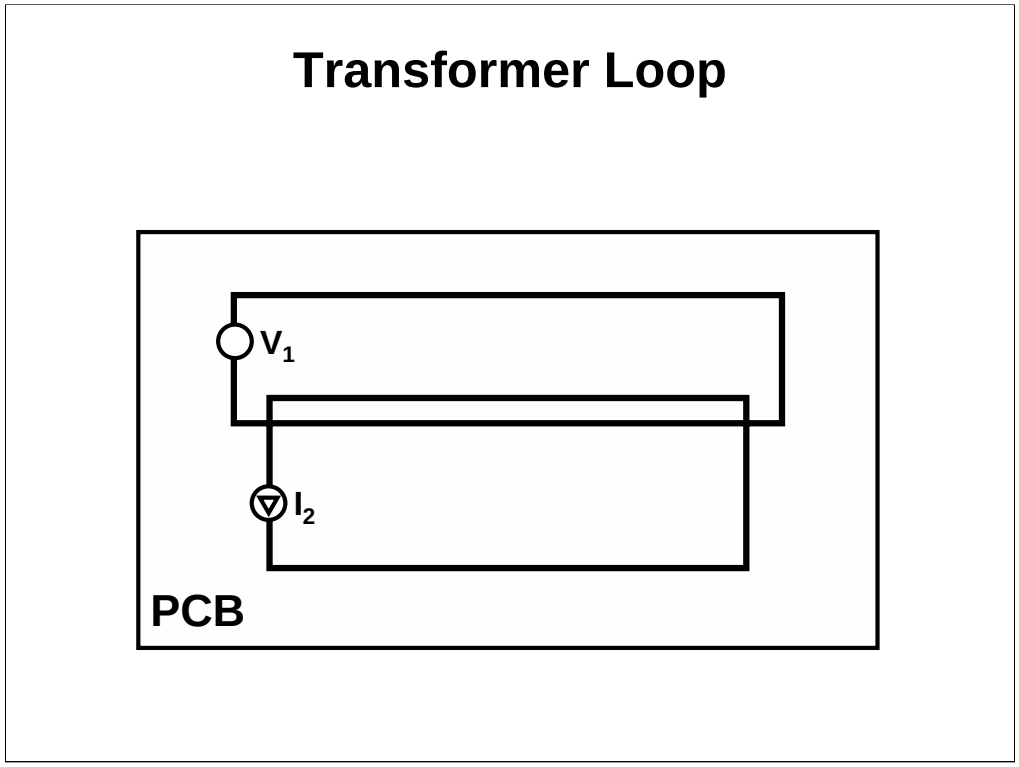


The analog circuits are added next. Keep the analog inputs as far from the digital signals as possible. Use the analog outputs or grounded pins to buffer the analog inputs from noise. As the analog signal is gained up it is routed to the converters where it is needed. The clock is a digital signal, but clock jitter is so critical in high frequency systems that the clock is often considered as an analog signal. No, I don't like a digital signal, even if it is a clock, in the analog side of the board, but I don't always get what I want. Some form of this layout will work for you.

Final Board Considerations

- Analog and digital ground tie together at one point in the power supply
- Signal flow must separate analog and digital signals
- Low level analog signals are protected from digital noise
- Converter grounds connect to analog ground

Each of these points were considered in the previous layout, but they are universal, so they have to be considered when ever a board is laid out.



Loops make transformers; bad transformers, but only micro volts have to be transformed to cause 18-bit errors. Transformer noise is single ended noise, so the amplifier can't reject it. Avoid loops whenever possible, and when you are forced into making a loop be aware of possible noise injection.

Ground

- Use a plane for ground, and if possible, a plane for power
- Ground return paths have inductance and resistance
- Keep return path impedance low
- Keep high currents out of signal ground
- Separate analog and digital grounds; tie together at one point

Ground planes provide the smallest possible impedance. The return currents run under the outgoing currents in a ground plane system, and this situation takes advantage of Lenz's law for field cancellation. High currents in the ground system can cause heating that propagates a thermal cycle or noise, so high currents should be run with separate wires. It is almost impossible to separate digital and analog return currents in a common ground plane design, thus splitting the ground plane automatically solves most of the return current problem. There will always be some digital current flowing in an analog ground, and this is OK if you control the digital current and route it wisely.

Beware of Inductance

- Open wire has approximately 1nH per foot
- PC traces have approximately 10nH per inch
- Cables are inductive
- Wire bonds are inductive
- Inductance causes peaking

Inductors want to keep current flowing or they provide a large voltage spike. Inductance should be minimized when ever possible to avoid spiking or peaking.

Resistors

- Resistors have parallel capacitance and series inductance
- Power resistors will couple heat to circuits
- High value resistors are less stable
- High value resistors change value when voltage is applied
- Wirewound resistors are highly inductive
- All resistors have noise

Simple components like resistors have parameters that can cause a circuit to malfunction. Parallel capacitance can increase or decrease frequency response depending on how the resistor is used. Power resistors dissipate heat, and the radiated heat can cause on-board components or adjacent components to drift or malfunction. High value film resistors (above 4.7MΩ) drift more than low value resistors. Resistor noise in the preamp stage may cause poor overall noise performance.

Printed Wiring Board - PWB

- The Printed Wiring Board is the pattern of interconnect - typically multiple layers of interconnect
- By deciding the properties that are important it is easier to make informed decisions regarding the materials used

Be careful in the selection of the circuit board material because it performs many functions.

Summary of Board Material Factors

- Mechanical
  - Flexural Strength
  - Glass transition temperature
  - Punching properties
- Electrical
  - Dielectric strength
  - Dielectric Breakdown
  - Dielectric Constant - Permittivity
  - Characteristic impedance
  - Propagation delay
- Flammability
  - UL evaluation system

Summary

- Pay attention to details
- If you don’t know; ask
- There must be a reason for every part’s existence
- Look for what you lost
- Test for performance and customer inflicted damage
- Calculate, then test, then test again

The circuit design process does not end when the schematic and parts list is committed to paper. The circuit layout is critical to function, cost, and performance, so you must take the layout design as seriously as you take the circuit design. When you don’t know why you are doing something ask a peer for advice, not for the solution. You aren’t obligated to take the advice, but you should strongly consider the advice. After a time you will determine who gives good advice. Every new breakthrough you make comes at something else’s expense; are you willing to pay the price? Testing is like living life; you can make the experience informative and consequently pleasurable, or you can make it a long series of repeated mistakes.

Section—4
Design Tools

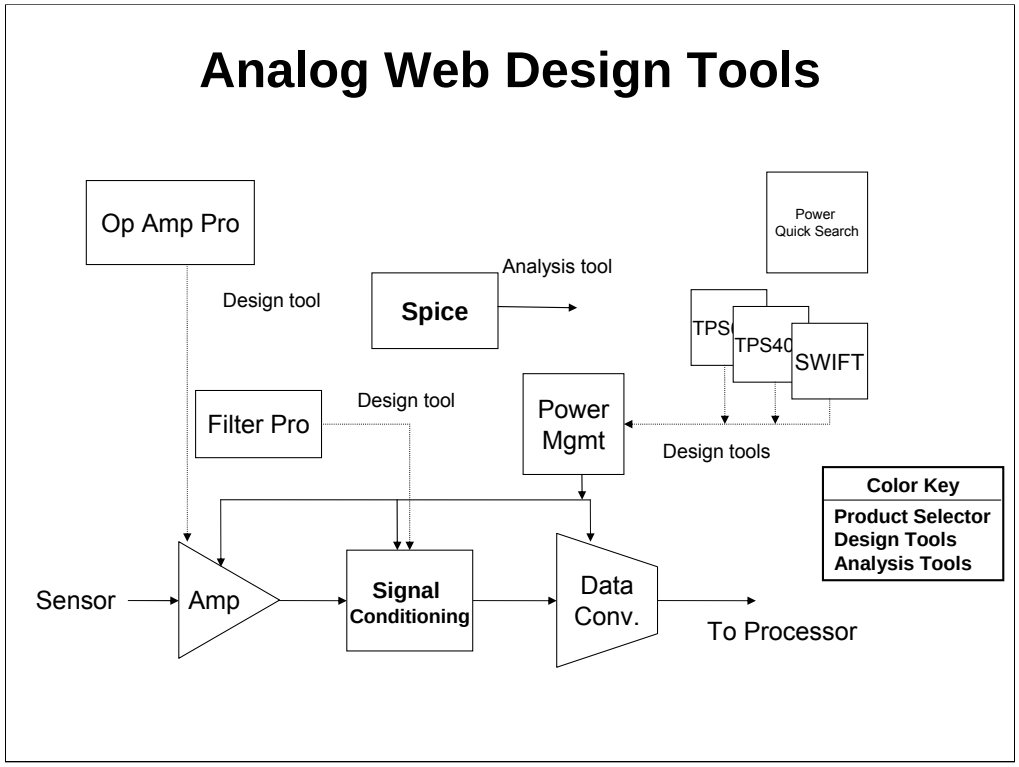
These Tools are Available from the
Texas Instruments Web Site

Design tools for an engineer compare to a shovel, backhoe, and diesel shovel for a ditch digger. There are many different design tools an engineer can use, and some are better than others, but even the lowly calculator, like the shovel, has everyday uses. The design tools given in this section of the seminar are in the backhoe to diesel shovel range.

Types of Tools Available From TI

- Product Selector
  - Select the optimum IC
- Design Tools
  - User provides the data (defines the circuit)
  - Program calculates component values, optimizes IC selection, performs error analysis.
  - Program prevents design and entry errors
- Analysis Tools
  - User provides the circuit schematic
  - Program performs circuit analysis on command
  - SPICE

Three types of tools are available from TI. Product selectors help the engineer who knows the type of product desired and just needs to quickly select the optimum part. Product selectors reside on TI's web site and are not downloadable because they are continually refreshed. Design tools can be used by engineers having little or no analog design experience. The design tool user must know what they expect from their application, like input, output and supply voltages, and the tool selects the circuit and completes the design. Analysis tools require the user to have at least a medium degree of analog knowledge because these sophisticated tools require the user to bring a circuit containing the problem solution to the party. Analysis tools are used to do an in depth circuit analysis of a customer designed circuit, and they can be used to extend the analysis performed by a design tool.



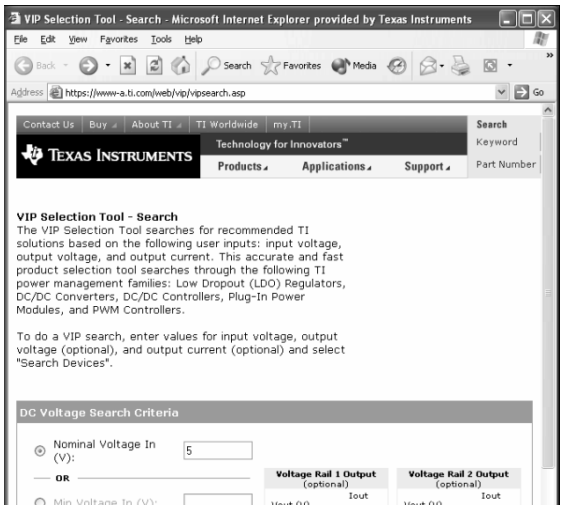
All tools shown here are available now from Texas Instruments for no charge. The bottom blocks comprise a standard signal chain, the green blocks represent the available design tools, the yellow box represents the search tool (Product Selector), and the red box represents the analysis tool.

Product Selector Allows Two Types of Searches

- Search by IC function
  - "Quick search"
- Search by parameter
  - Most data sheet parameters including:
  - Supply voltage
  - Offset voltage
  - Bias current
- Web Based Searches
  - Latest information
  - Large database

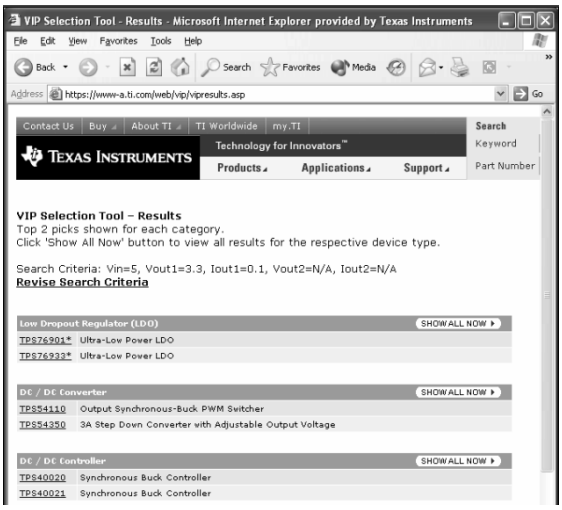
Product selectors are not down loadable because they must be constantly updated to insure that they contain the freshest information. There are two types of design tools. Quick Search tools enable the designer to search by circuit function; i. e., dc/dc converter, linear regulator, ADC, DAC, etc. Parameter Search tools enable the designer to search by parameter; i. e., voltage current, resolution, gain, etc. Using the tools in tandem results in a speedy identification of the desired product.

Product Selector
VIP - Power Quick Search



Parameter search keys in on a selected product and enables the selection of the exact product by parameter.

Product Selector
VIP - Power Quick Search Results



Quick search tools search by circuit type. The two most popular or newest circuits are identified and highlighted in blue. The complete product offering is shown when the show all now box is clicked.

OpAmpPro – Design Tool

- Requires input/output data and PS value
- Performs these functions
  - Selects circuit configuration
  - Calculates resistor values, enables scaling
  - Worst case resistor analysis
  - Calculates optimum adjustment resistor value
  - Selects op amp and does error calculations
  - Bode and transient plots

WWW.ti.com/opamppro

OpAmpPro is a design tool that designs an analog interface between a low output impedance source and a high input impedance load. This program takes the input data and calculates the transform equation. Based on this equation it selects the circuit configuration that implements the transform equation, and it uses seed resistor values to calculates and displays the actual resistor values. This versatile program enables the designer to scale the resistor values, and it can calculate the worst case transform equations based on entered tolerances. The final resistor calculation is to find the optimum values required to adjust out the tolerances.

The program continues on to select the optimum op amp based on an error analysis that uses designer entered error budgets. The op amp selection accounts for package, number of amplifiers per package, quiescent current, error analysis, and price. A Bode plot and transient response plot is available after an op amp is selected.

FilterPro – Design Tool

- Number of poles
- Type filter
  - Butterworth
  - Chebychev
  - Bessel and more
- Sallen Key or MFB implementation
- High pass or low pass
- Filter cutoff frequency, and much more

WWW.ti.com/filterpro

FilterPro designs 8 types of filters. These filter designs are available in MFB or Sallen-Key circuit implementations and in high pass or low pass configurations. Further controllable variables are filter cutoff frequency, number of poles, seed resistor values, resistor tolerance selection, capacitor tolerance selection, and a fully differential mode. The filter performance data may be observed through the placement of a cursor in a graph, and designer selected component values may be entered to observe their response effect.

DC to DC Converter Design Tools

- Complete design
  - Schematic, analysis, efficiency graph
  - Stress analysis, loop response graph
  - Waveforms, bill of material
- Three choices
  - SWIFT Designer—3.3V @ 6V, 5V @ 3A
  - TPS40K—1.8V @ 10A
  - LoPwrDC—1.8V @ 200mA

WWW.ti.com/swift

Each dc/dc converter design tool works with a specific family of ICs. These programs design dc/dc converters for a range of load voltages and load currents. They complete all aspects of the design including a schematic, node analysis, stress analysis, Bode plot, efficiency plot, and bill-of-materials. The designer can change the load requirement, key component values, or performance parameters at will and rerun the design to determine the effect of the changes.

Tina-TI Analysis Tool

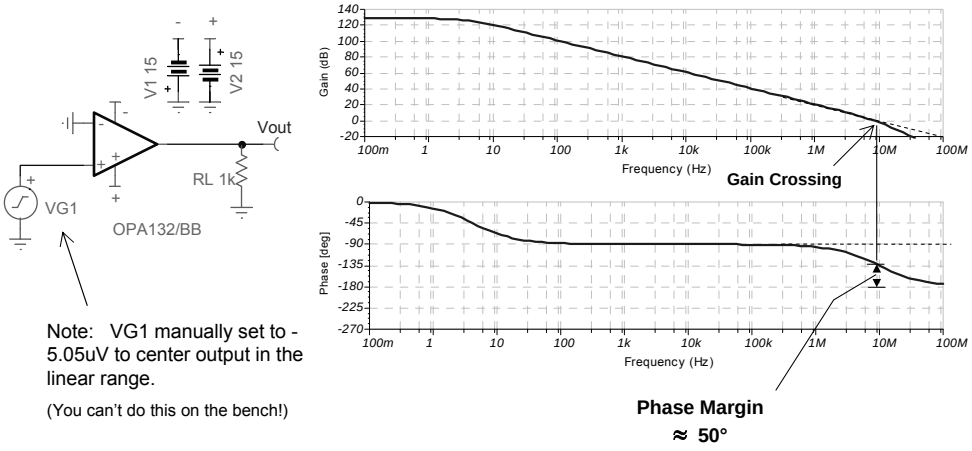
- Free Spice analysis program
- Three op amps and 100 nodes
- TI model compatibility
  - Functionality only
- Common platform with TI applications engineers
- Transfer from future app notes, Analog Applications Journal, or data sheet to circuit folder in Tina-TI

www.ti.com/tina-ti

Tina-TI is a Spice based program that is compatible with TI generated models. This insures that the TI model works with Tina-TI or we will fix the model. Another advantage of Tina-TI is that you can cut and paste or email schematics, data and plots to your design review committee. If you question the model, or circuit's performance in Tina-TI you can email your information to TI applications to obtain their comments. New analog application notes, analog Journal articles, and data sheets contain a Tina-TI bug; clicking on the bug brings up the previously installed Tina-TI, and it comes up at the file for the circuit that contained the bug. Fast transfer from an application note to the same circuit in Spice is possible with this technique.

Open-Loop Response

Simulation shows data-sheet-type gain/phase plot to check spice model.

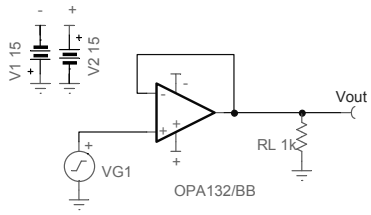


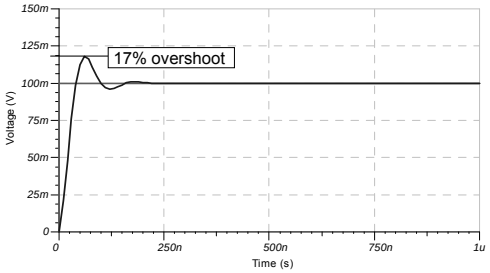
Note: VG1 manually set to -5.05uV to center output in the linear range.

(You can't do this on the bench!)

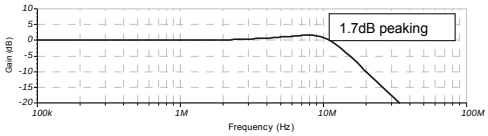
The output voltage range is the power supply voltage minus the op amp overhead voltage 15x2-2xVOH = 32-3 = 29V. The gain is approximately 130dB or 3,163, 000. Dividing the voltage range by the gain yields the maximum input voltage swing of 9.1μV; notice that the designer chose an input voltage of approximately 5μV. Now, run the open loop gain transfer function on Spice and plot as shown. The OPA132 data sheet open loop gain matches the Spice plot, so now we know that the data sheet correlates the model.

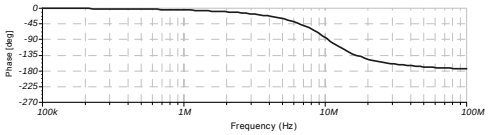
G=1, (no C load)





Phase Margin	Overshoot
90°	0
80°	2%
70°	5%
60°	10%
50°	16%
40°	25%
30°	37%
20°	53%
10°	73%





See notes for instructions.

Tina Schematic

The proof-of-the-pudding is when you can match the model to the data sheet and verify this performance in the lab. Notice that the model shows 50o phase margin, and that the table relates this to approximately 17% overshoot. The circuit use to test for the transient response is a buffer, thus the transient response is a function of the op amp and not external components. The model performance is easily verified in the lab, so the model is connected to the data sheet through Spice, and the model is connected to the data sheet through the lab.

Design Tools – Coming Attractions

- SensorPro
  - Design sensor to ADC interface circuit
- Cookbook Circuit File
  - File of applications circuits
  - Circuit description
  - Tina-TI folder with analysis data

TI is constantly improving and generating new design tools. Watch TI's web site to follow the new developments.

Section 6

Additional Information on Products, Tools and Support

From

Texas Instruments

For more information on Data Converters please look at the Texas Instruments data converter home page:

www.dataconverter.com

This page provides access to:

DATA CONVERTER PRODUCTS

- Alphabetical Product Listing
- Device Locator
- New Products
- Parametric Search
- Part Number and Keyword Search

DESIGN RESOURCES

- Application Notes
- Datasheets
- Development Tools (EVMs)
- Packaging Information

HOW TO PURCHASE

- Distributors
- Pricing and Availability
- Samples

SUPPORT

- Ask an Expert
- Industry Forums
- News and Publications
- Standards Bodies
- Training

For more information on Amplifiers please look at the Texas Instruments amplifier home page:

www.amplifier.ti.com

This page provides access to:

AMPLIFIER PRODUCTS

- Alphabetical Product Listing
- Analog Cross Refefence Search
- Device Locator
- Parametric Search
- Part Number and Keyword Search

DESIGN RESOURCES

- Application Notes
- Datasheets
- Development Tools
- Engineering Design Utilities
- Packaging Information
- Macro Models

HOW TO PURCHASE

- Distributors
- Pricing and Availability
- Samples

SUPPORT

- Ask an Expert
- Knowledge base
- Industry Forums
- News and Publications
- Standards Bodies
- Training

For more information on Power please look at the Texas Instruments power home page:

www.power.ti.com

This page provides access to:

POWER PRODUCTS

- Alphabetical Product Listing
- Analog Cross Refefence Search
- Device Locator
- Parametric Search
- Part Number and Keyword Search

DESIGN RESOURCES

- Application Notes
- Datasheets
- Development Tools
- Engineering Design Utilities
- Packaging Information
- Macro Models

HOW TO PURCHASE

- Distributors
- Pricing and Availability
- Samples

SUPPORT

- Ask an Expert
- Knowledge base
- Industry Forums
- News and Publications
- Standards Bodies
- Training

For more information on Interface please look at the Texas Instruments interface home page:

www.ti.com/sc/datatran

This page provides access to:

INTERFACE PRODUCTS

- Alphabetical Product Listing
- Analog Cross Refefence Search
- Device Locator
- Parametric Search
- Part Number and Keyword Search

DESIGN RESOURCES

- Application Notes
- Datasheets
- Development Tools
- Engineering Design Utilities
- Packaging Information
- Macro Models

HOW TO PURCHASE

- Distributors
- Pricing and Availability
- Samples

SUPPORT

- Ask an Expert
- Knowledge base
- Industry Forums
- News and Publications
- Standards Bodies
- Training

TI Home Page

www.ti.com

Analog Home Page

http://focus.ti.com/docs/analog/analoghomepage.jhtml

Applications Home Page

http://focus.ti.com/docs/apps/appshomepage.jhtml

Signal Conditioning basics:

Op Amps For Everyone—Please contact your local TI Sales office or Distributor office.

For information on training including: on-line training, webcasts, seminars and workshops.

http://focus.ti.com/docs/training/traininghomepage.jhtml