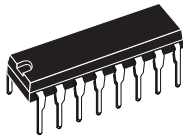
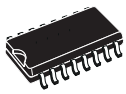
HCF4046B

MICROPOWER PHASE-LOCKED LOOP

- QUIESCENT CURRENT SPECIFIED UP TO 20V
- VERY LOW POWER CONSUMPTION : 70µW (TYP.) AT VCO f_o = 10kHz, V_{DD} = 5V
- OPERATING FREQUENCY RANGE : UP TO 1.4MHz (TYP.) AT V_{DD} = 10V
- LOW FREQUENCY DRIFT : 0.04%/°C (typ.) AT V_{DD} = 10V
- CHOICE OF TWO PHASE COMPARATORS : 1) EXCLUSIVE - OR NETWORK 2) EDGE-CONTROLLED MEMORY NETWORK WITH PHASE-PULSE OUTPUT FOR LOCK INDICATION
- HIGH VCO LINEARITY: <1% (TYP.)
- VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION
- SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (demod. output)
- ZENER DIODE TO ASSIST SUPPLY REGULATION
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP



SOP

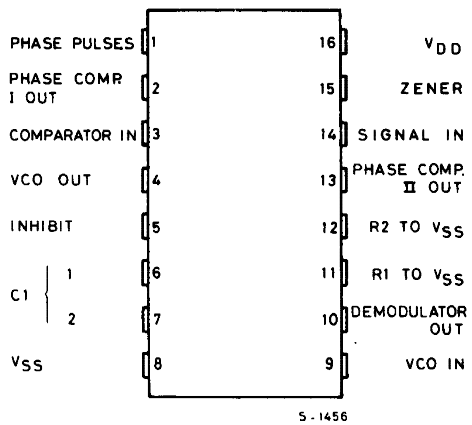
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4046BEY	
SOP	HCF4046BM1	HCF4046M013TR

DESCRIPTION

The HCF4046B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor Technology, available in 16-lead dual in-line plastic or ceramic package. The HCF4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

PIN CONNECTION



VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifiers the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 KΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the HCF4024B, HCF4018B, HCF4020B, HCF4022B, HCF4029B and HBF4059A. One or more HCF4018B (Presettable Divide-by-N Counter) or HCF4029B (Presettable Up/Down Counter), or HBF4059A (Programmable Divide-by-"N" Counter), together with the HCF4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" $\leq$ 30% of (V_{DD}-V_{SS}), logic "1" $\geq$ 70% of (V_{DD}-V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal-and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (fo). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range (2 f_C). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range (2 f_L). The capture range is $\leq$ the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig.1 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of fo is shown in fig.2. Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the

p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig.3 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

Figure 1 : Phase-Comparator I Characteristics at Low-Pass Filter Output.

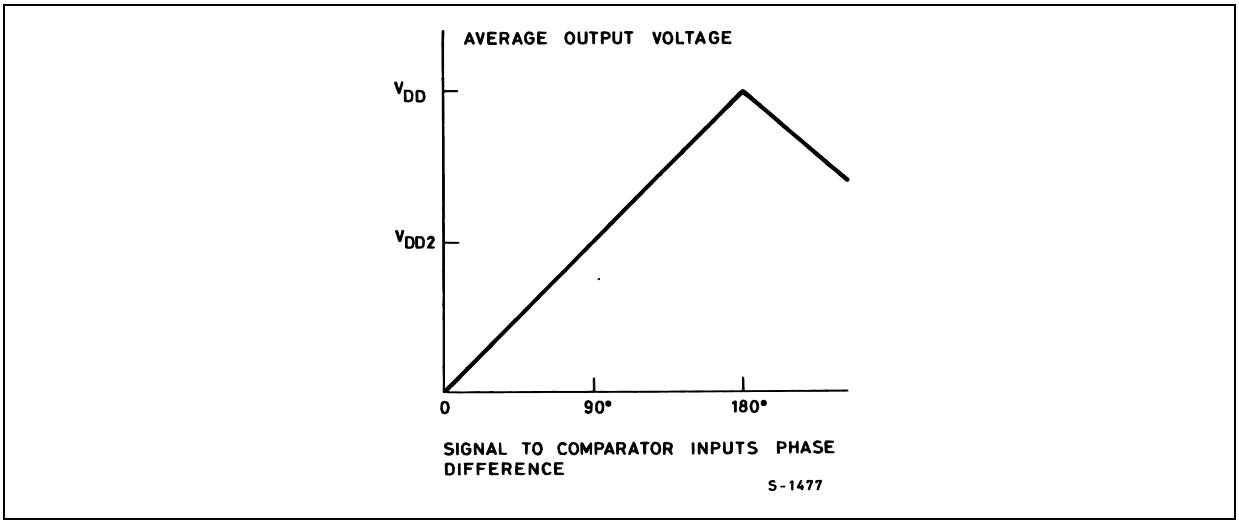


Figure 2 : Typical Waveforms for CMOS Phase Locked-Loop Employing Phase Comparator I in Locked Condition of f_o

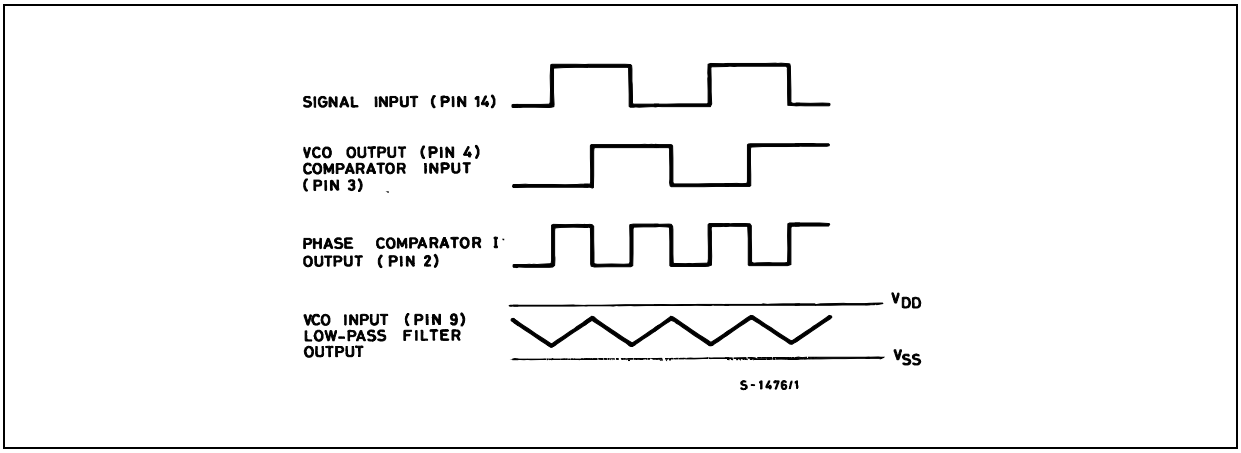
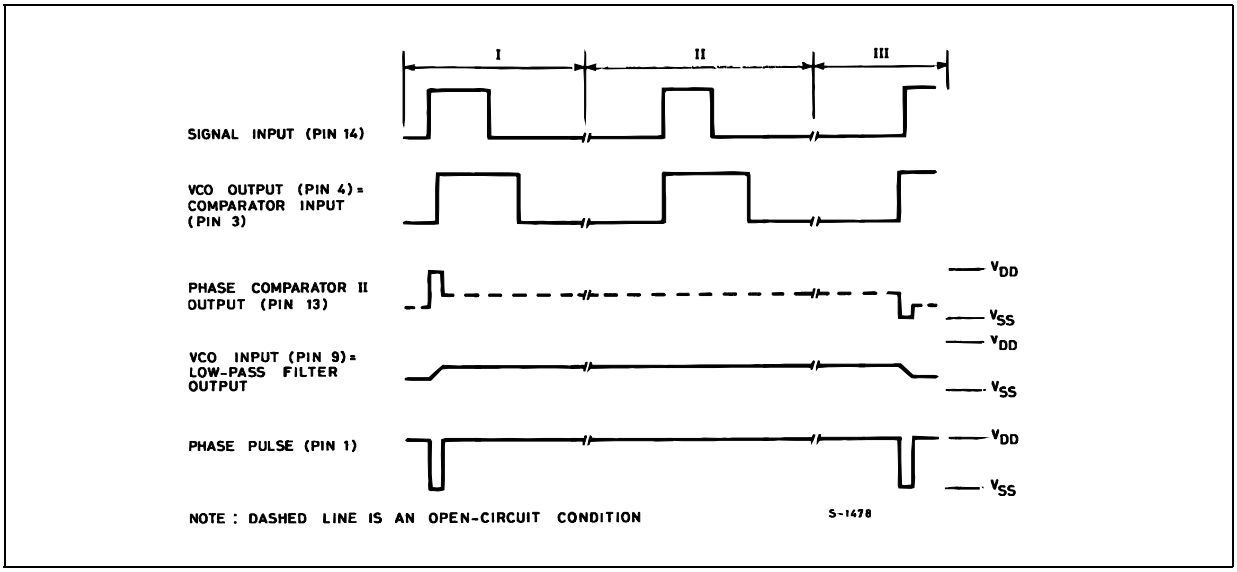
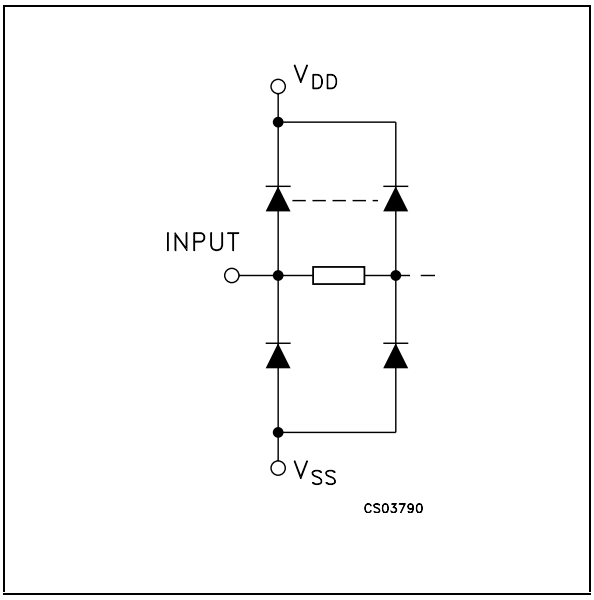


Figure 3 : Typical Waveforms for CMOS Phase-locked Loop Employing Phase Comparator II In Locked Condition



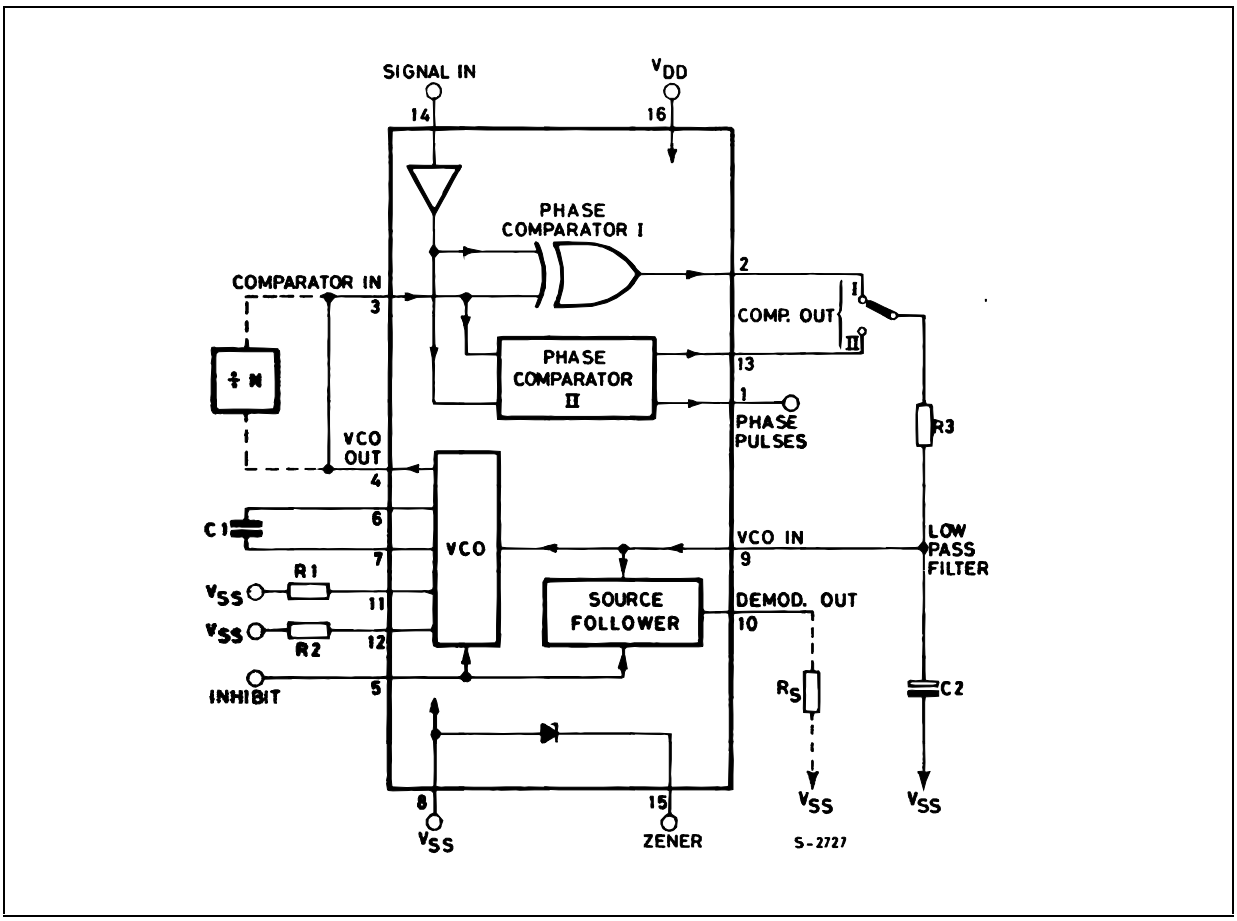
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	PHASE PULSES	Phase Comparator Pulse Output
2	PHASE COMP I OUT	Phase Comparator 1 Output
3	COMPARATOR IN	Comparator Input
4	VCO OUT	VCO Output
5	INHIBIT	Inhibit Input
6, 7	C1	Capacitors
9	VCO IN	VCO Input
10	DEMODULATOR OUT	Demodulator Output
11	R_1 TO V_{SS}	Resistor R1 Connection
12	R_2 TO V_{SS}	Resistor R2Connection
13	PHASE COMP II OUT	Phase Comparator 2 Output
14	SIGNAL IN	Signal Input
15	ZENER	Diode Zener
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
VCO SECTION													
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
PHASE COMPARATOR SECTION													
I_{DD}	Total Device Current Pin 14= Open Pin 5= V_{DD}	0/5			5		0.05	0.1		0.1		0.1	mA
		0/10			10		0.25	0.5		0.5		0.5	
		0/15			15		0.75	1.5		1.5		1.5	
		0/20			20		2	4		4		4	
	Total Device Current Pin 14= V_{SS} or V_{DD} Pin 5= V_{DD}	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000			
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
I_{OUT}	High Impedance Leakage Current	0/18	Any Input		18		$\pm 10^{-4}$	±0.4		±12		±12	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

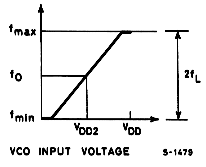
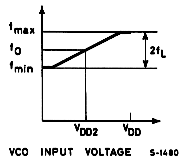
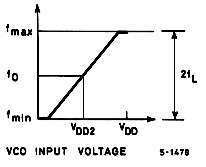
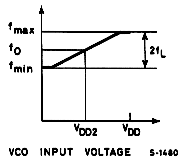
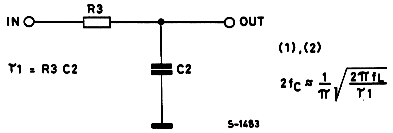
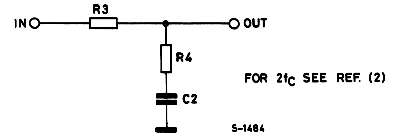
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Test Condition			Value (*)			Unit
		V_{DD} (V)			Min.	Typ.	Max.	
VCO SECTION								
P_D	Operating Power Dissipation	5	f_O = 10KHz	R1 = 10MΩ		70	140	µW
		10	R2 = ∞	$V_{COIN} = V_{DD}/2$		800	1600	
		15				3000	6000	
f_{MAX}	Maximum frequency	5	R_1 = 10KΩ	C1 = 50pF	0.3	0.6		ns
		10	R2 = ∞	$V_{COIN} = V_{DD}$	0.6	1.2		
		15			0.8	1.6		
		5	R_1 = 5KΩ	C1 = 50pF	0.5	0.8		ns
		10	R2 = ∞	$V_{COIN} = V_{DD}$	1	1.4		
		15			1.4	2.4		
	Center Frequency (f_O) and frequency Range f_{max} - f_{min}	Programable with external components R_1, R_2, and C_1 See Design Information						
	Linearity	5	V_{COIN} =2.5V$^{\pm 0.3}$	R_1 = 10KΩ		1.7		%
		10	V_{COIN} =5V$^{\pm 1}$	R_1 = 100KΩ		0.5		
		10	V_{COIN} =5V$^{\pm 2.5}$	R_1 = 400KΩ		4		
		15	V_{COIN} =7.5V$^{\pm 1.5}$	R_1 = 100KΩ		0.5		
		15	V_{COIN} =7.5V$^{\pm 5}$	R_1 = 1MΩ		7		
	Temperature Frequency Stability (no frequency offset) f_{min} = 0	5				±0.12		%/°C
		10				±0.04		
		15				±0.015		
	Temperature Frequency Stability (frequency offset) f_{min} = 0	5				±0.09		
		10				±0.07		
		15				±0.03		
VCO	Output Duty Cycle	5, 10, 15				50		%
t_{TLH} t_{THL}	VCO Output Transition Time	5				100	200	ns
		10				50	100	
		15				40	80	
	Source Follower Output (Demodulated Output): Offset Voltage V_{COIN}-V_{DEM}	5, 10, 15	R_S > 10KΩ			1.8	2.5	V
	Source Follower Output (Demodulated Output): Linearity	5	R_S = 100KΩ	V_{COIN} =2.5V$^{\pm 0.3}$		0.3		%
		10	R_S = 300KΩ	V_{COIN} =5V$^{\pm 2.5}$		0.7		
		15	R_S = 500KΩ	V_{COIN} =7.5V$^{\pm 5}$		0.9		
V_Z	Zener Diode Voltage		I_Z = 50 µA		4.45	5.5	7.5	V
R_Z	Zener Dynamic Resistance		I_Z = 1 mA			40		Ω

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
PHASE COMPARATOR SECTION							
R14	Pin 14 (signal in) Input Resistance	5		1	2		MΩ
		10		0.2	0.4		
		15		0.1	0.2		
	AC Coupled Signal Input Sensivity (*) (peak to peak)	5	f_{IN} = 100KHz sine wave		180	360	mV
		10			330	660	
		15			900	1800	
t_{PLH}	Propagation Delay Time High to Low Level Pins 14 to 1	5			225	450	ns
		10			100	200	
		15			65	130	
t_{PLH}	Propagation Delay Time Low to High Level	5			350	700	ns
		10			150	300	
		15			100	200	
t_{PHZ}	Disable Time High Level to High Impedance Pins 14 to 13	5			225	450	ns
		10			100	200	
		15			65	130	
t_{PLZ}	Disable Time Low Level to High Impedance	5			285	570	ns
		10			130	260	
		15			95	190	
t_r t_f	Input Rise or Fall Time Comparator Pin 3	5				50	µs
		10				1	
		15				0.3	
	Signal Pin 14	5				500	µs
		10				20	
		15				2.5	
t_{TLH} t_{THL}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	

(*) For sine Wave the frequency must be greater than 10KHz for Phase Comparator II

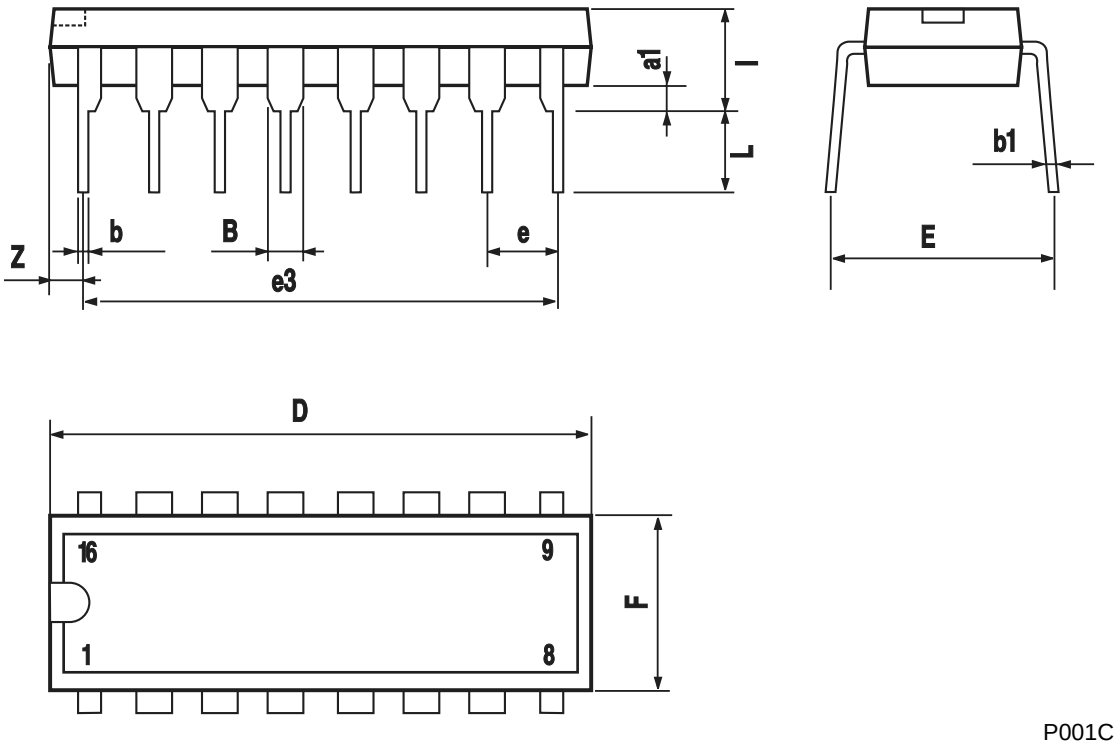
DESIGN INFORMATION This information is a guide for approximating the value of external components in a Phase-Locked-Loop system. The selected external components must be within the following ranges:
$5K\Omega \leq R_1, R_2, R_S \leq 1M\Omega$ $C_1 \geq 100pF$ at $V_{DD} \geq 5V$ $C_1 \geq 50pF$ at $V_{DD} \geq 10V$

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET R2=∞	VCO WITH OFFSET	VCO WITHOUT OFFSET R2=∞	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL System will Adjust to Centre Frequency f_o		VCO in PLL System will Adjust to Lowest Operating Frequency f_o	
Frequency Lock Range, $2f_L$	$2f_L$ = Full VCO Frequency Range $2fL = f_{max} - f_{min}$			
Frequency Lock Range, $2f_C$			$f_C = f_L$	
Loop filter Component Section				
Phase Angle Between SIgnal and Comparator	90° at Centre frequency (f_O), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Centre Frequency	Yes		No	
Signal Input Nose Rejection	High		Low	

For further information, see
(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
(2) G.S. Mosckytz "miniaturized RC filters using phase Lockedloop" BSTJ May 1965

Plastic DIP-16 (0.25) MECHANICAL DATA

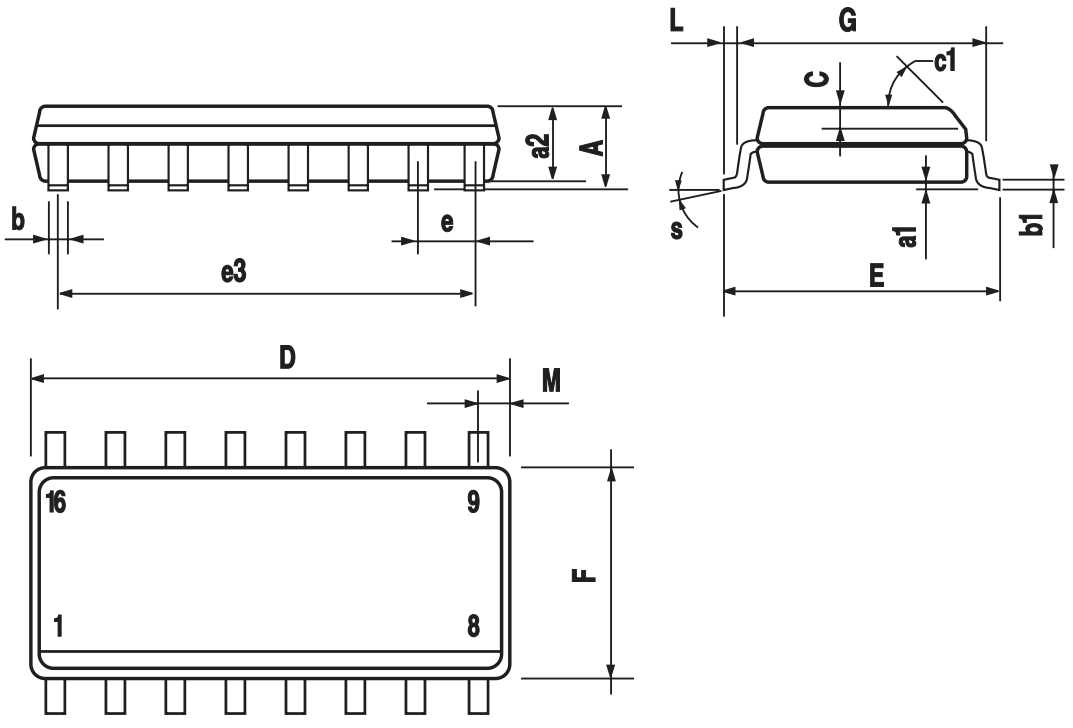
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

SN74LV4046A High-Speed CMOS Logic Phase-Locked Loop With VCO

1 Features

- Choice of Three Phase Comparators
  - Exclusive OR
  - Edge-Triggered J-K Flip-Flop
  - Edge-Triggered RS Flip-Flop
- Excellent VCO Frequency Linearity
- VCO-Inhibit Control for ON/OFF Keying and for Low Standby Power Consumption
- Optimized Power-Supply Voltage Range From 3 V to 5.5 V
- Wide Operating Temperature Range . . . –40°C to 125°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Telecommunications
- Signal Generators
- Digital Phase-Locked Loop

3 Description

The SN74LV4046A is a high-speed silicon-gate CMOS device that is pin compatible with the CD4046B and the CD74HC4046. The device is specified in compliance with JEDEC Std 7.

The SN74LV4046A is a phase-locked loop (PLL) circuit that contains a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2, and PC3). A signal input and a comparator input are common to each comparator.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the SN74LV4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear operational amplifier techniques. Various applications include telecommunications, digital phase-locked loop and signal generators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV4046A	SOP (16)	7.70mm x 10.20mm
	SOIC (16)	6.00mm x 9.90mm
	TSSOP (16)	6.40mm x 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SN74LV4046A Functional Block Diagram

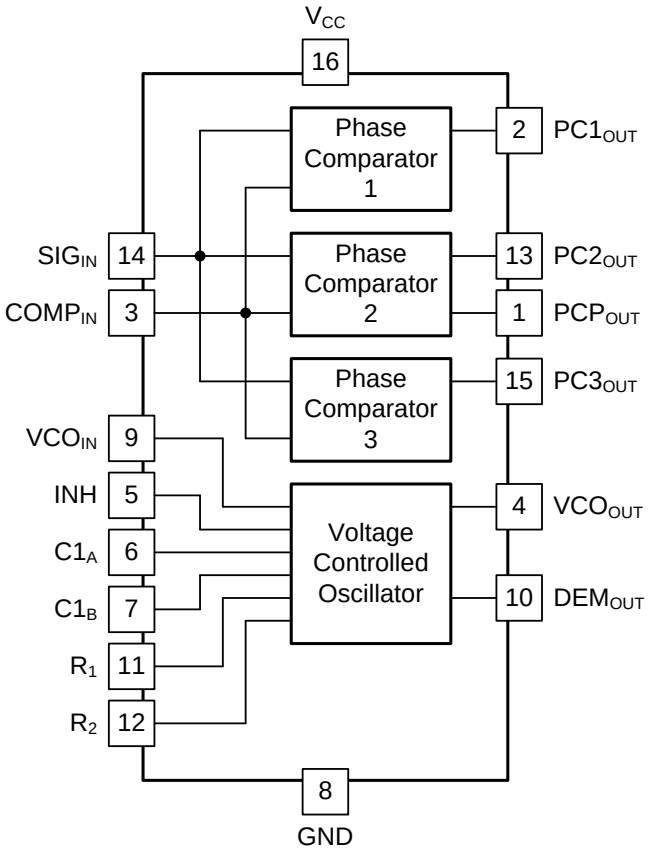


Table of Contents

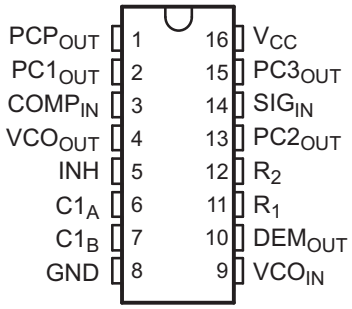
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2007) to Revision D	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

D, DGV, NS, or PW Package
16-Pin SOIC, SOP, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PCP_{OUT}	1	O	Phase comparator pulse output
$PC1_{OUT}$	2	O	Phase comparator 1 output
$COMP_{IN}$	3	I	Comparator input
VCO_{OUT}	4	O	VCO output
INH	5	I	Inhibit input
$C1_A$	6	—	Capacitor C1 connection A
$C1_B$	7	—	Capacitor C1 connection B
GND	8	—	Ground (0 V)
VCO_{IN}	9	I	VCO input
DEM_{OUT}	10	O	Demodulator output
R_1	11	—	Resistor R1 connection
R_2	12	—	Resistor R2 connection
$PC2_{OUT}$	13	O	Phase comparator 2 output
SIG_{IN}	14	I	Signal input
$PC3_{OUT}$	15	O	Phase comparator 3 output
V_{CC}	16	—	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	DC supply voltage		–0.5	7	V
V_I	Input voltage		–0.5	V_{CC} + 0.5	V
V_O	Output voltage		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output curent	V_O = 0 to V_{CC}		±35	mA
I_{CC}	DC V_{CC} or ground current			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	125	°C
V_{CC}	Supply voltage	3	5.5	V
V_I, V_O	DC input or output voltage	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		D	DGV	NS	PW	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	120	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS		V_{CC} (V)	MIN	TYP	MAX	UNIT
				V_I (V)	I_O (mA)					
VCO										
V_{IH}	High-level input voltage	INH				3 to 3.6	V_{CC} × 0.7			V
						4.5 to 5.5	V_{CC} × 0.7			
V_{IL}	Low-level input voltage	INH				3 to 5.5			V_{CC} × 0.3	V
						4.5 to 5.5			V_{CC} × 0.3	
V_{OH}	High-level output voltage	VCO_{OUT}	CMOS	V_{IL} or V_{IH}	–0.05	3 to 3.6	V_{CC} – 0.1			V
						4.5 to 5.5	V_{CC} – 0.1			
			TTL		–12	4.5 to 5.5	3.8			
V_{OL}	Low-level output voltage	VCO_{OUT}	CMOS	V_{IL} or V_{IH}	0.05	3 to 3.6			0.1	V
						4.5 to 5.5			0.1	
			TTL		12	4.5 to 5.5			0.55	
		C1A, C1B (test purposes only)			12	4.5 to 5.5			0.65	
I_I	Input leakage current	INH, VCO_{IN}		V_{CC} or GND		5.5			±1	µA
	R1 range[1]					3 to 5.5	3		50	kΩ
	R2 range[1]					3 to 5.5	3		50	kΩ
	C1 capacitance range					3 to 3.6	40		No Limit	pF
						4.5 to 5.5	40		No Limit	
	Operating voltage range	VCO_{IN}		Over the range specified for R1 for linearity[2]		3 to 3.6	1.1		1.9	V
						4.5 to 5.5	1.1		3.2	
PHASE COMPARATOR										
V_{IH}	DC-coupled high-level input voltage		SIG_{IN}, $COMP_{IN}$			3 to 3.6	V_{CC} × 0.7			
						4.5 to 5.5	V_{CC} × 0.7			
V_{IL}	DC-coupled low-level input voltage		SIG_{IN}, $COMP_{IN}$			3 to 3.6			V_{CC} × 0.3	V
						4.5 to 5.5			V_{CC} × 0.3	
V_{OH}	High-level output voltage	PCP_{OUT}, PCN_{OUT}	CMOS	V_{IL} or V_{IH}	–0.05	3 to 5.5	V_{CC} – 0.1			V
					–6	3 to 3.6	2.48			
			TTL		–12	4.5 to 5.5	3.8			
V_{OL}	Low-level output voltage	PCP_{OUT}, PCN_{OUT}	CMOS	V_{IL} or V_{IH}	0.02	3 to 3.6			0.1	V
						4.5 to 5.5			0.1	
			TTL		4	4.5 to 5.5			0.4	
I_I	Input leakage current		SIG_{IN}, $COMP_{IN}$	V_{CC} or GND		3 to 3.6			±11	µA
						4.5 to 5.5			±29	
I_{OZ}	3-state off-state current		$PC2_{OUT}$	V_{IL} or V_{IH}		3 to 5.5			±5	µA
R_I	Input resistance		SIG_{IN}, $COMP_{IN}$	V_I at self-bias operating point, V_I = 0.5 V		3		800		kΩ
						4.5		250		
DEMODULATOR										
R_S	Resistor range			R_S > 300 kΩ, Leakage current can influence V_{DEMOUT}		3 to 3.6	50		300	kΩ
						4.5 to 5.5	50		300	
V_{OFF}	Offset voltage VCO_{IN} to V_{DEM}			V_I = V_{VCOIN} = $V_{CC/2}$, Values taken over R_S range		3 to 3.6		±30		mV
						4.5 to 5.5		±20		
I_{CC}	Quiescent device current			Pins 3, 5, and 14 at V_{CC}, Pin 9 at GND, I_I at pins 3 and 14 to be excluded		5.5			50	µA

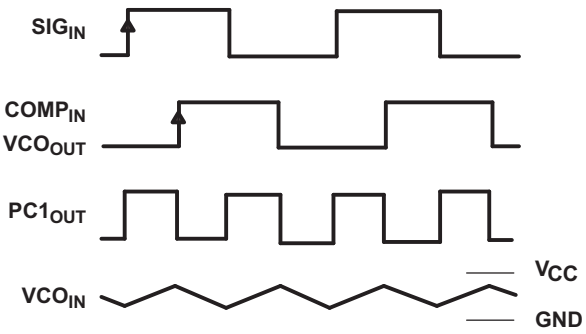
(1) The value for R1 and R2 in parallel should exceed 2.7 kΩ.
(2) The maximum operating voltage can be as high as V_{CC} – 0.9 V; however, this may result in an increased offset voltage.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) C_L = 50 pF, Input t_r, t_f = 6 ns

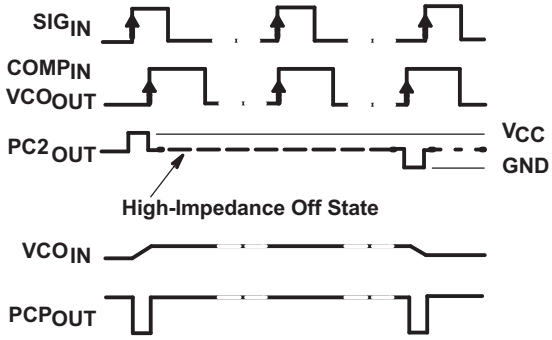
PARAMETER			TEST CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNIT
PHASE COMPARATOR								
t_{PLH}, t_{PHL}	Propagation delay	SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		3 to 3.6			135	ns
				4.5 to 5.5			50	
t_{PLH}, t_{PHL}	Propagation delay	SIGIN, $COMP_{IN}$ to PCP_{OUT}		3 to 3.6			300	ns
				4.5 to 5.5			60	
t_{PLH}, t_{PHL}	Propagation delay	SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		3 to 3.6			200	ns
				4.5 to 5.5			50	
t_{THL}, t_{TLH}	Output transition time			3 to 3.6			75	ns
				4.5 to 5.5			15	
t_{PZH}, t_{PZL}	3-state output enable time	SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		3 to 3.6			270	ns
				4.5 to 5.5			54	
t_{PHZ}, t_{PLZ}	3-state output disable time	SIG_{IN}, $COMP_{IN}$ to PC2OUT		3 to 3.6			320	ns
				4.5 to 5.5			65	
	AC-coupled input sensitivity	(P-P) at SIG_{IN} or $COMP_{IN}$	$V_{I(P-P)}$	3 to 3.6		11		mV
				4.5 to 5.5		15		
VCO								
Δf/ΔT	Frequency stability with temperature change		V_I = VCO_{IN} = 1/2 V_{CC}, R_1 = 100 kΩ, R_2 = ∞, C_1 = 100 pF	3 to 3.6		0.11		%/°C
				4.5 to 5.5		0.11		
f_{MAX}	Maximum frequency		C_1 = 50 pF, R_1 = 3.5 kΩ, R_2 = ∞	3 to 3.6		24		MHz
				4.5 to 5.5		24		
			C_1 = 0 pF, R_1 = 9.1 kΩ, R2 = ∞	3 to 3.6		38		
				4.5 to 5.5		38		
	Center frequency (duty 50%)		C_1 = 40 pF, R_1 = 3 kΩ, R_2 = ∞, VCO_{IN} = V_{CC}/2	3 to 3.6	7	10		MHz
				4.5 to 5.5	12	17		
				4.5 (1)	15 (1)		17.5 (1)	
ΔfVCO	Frequency linearity		C_1 = 100 pF, R_1 = 100 kΩ, R_2 = ∞	3 to 3.6		0.4%		
				4.5 to 5.5		0.4%		
	Offset frequency		C_1 = 1 nF, R_2 = 220 kΩ	3 to 3.6		400		kHz
				4.5 to 5.5		400		
DEMODULATOR								
V_{OUT} vs f_{IN}			C_1 = 100 pF, C_2 = 100 pF, R_1 = 100 kΩ, R_2 = ∞, R_3 = 100 kΩ	3		8		mV/kHz
				4.5		330		

(1) Data is specified at 25°C



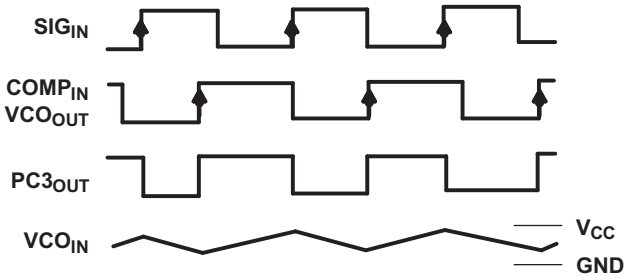
Loop Locked at f_o

Figure 1. Typical Waveforms for PLL Using Phase Comparator 1



Loop Locked at f_o

Figure 2. Typical Waveforms for PLL Using Phase Comparator 2



Loop Locked at f_o

Figure 3. Typical Waveforms for PLL Using Phase Comparator 3

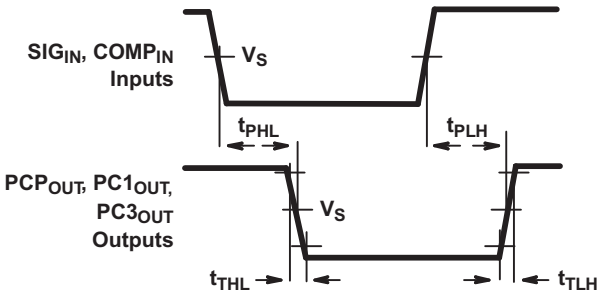


Figure 4. Input-to-Output Propagation Delays and Output Transition Times

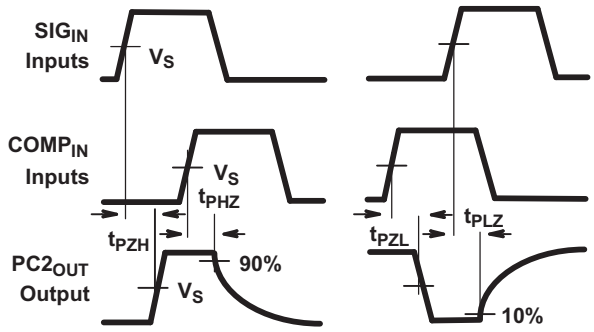
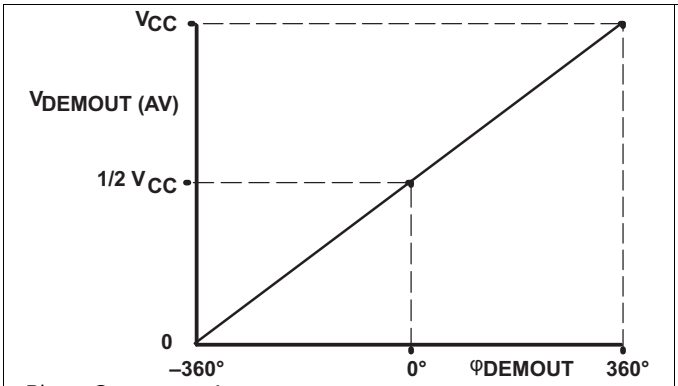


Figure 5. 3-State Enable and Disable Times for $PC2_{OUT}$

6.7 Typical Characteristics

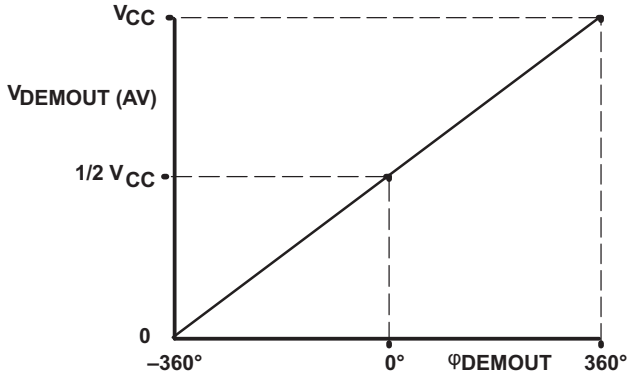


Phase Comparator 1:

$V_{DEMOUT} = V_{PC1OUT} = (V_{CC}/\pi)\ (SIG_{IN} – COMP_{IN})$;

$DEMOUT = (SIG_{IN} – COMP_{IN})$

Figure 6. Average Output Voltage vs Input Phase Difference

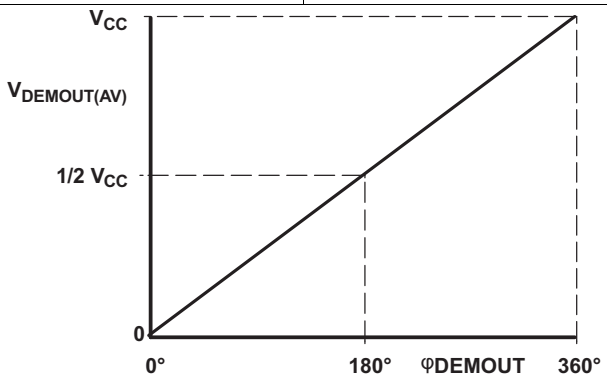


Phase Comparator 2:

$V_{DEMOUT} = V_{PC2OUT} = (V_{CC}/4)\ (SIG_{IN} – COMP_{IN})$;

$DEMOUT = (SIG_{IN} – COMP_{IN})$

Figure 7. Average Output Voltage vs Input Phase Difference



Phase Comparator 3:

$V_{DEMOUT} = V_{PC3OUT} = (V_{CC}/2\pi)\ (SIG_{IN} – COMP_{IN})$;

$DEMOUT = (SIG_{IN} – COMP_{IN})$

Figure 8. Average Output Voltage vs Input Phase Difference

7 Detailed Description

7.1 Overview

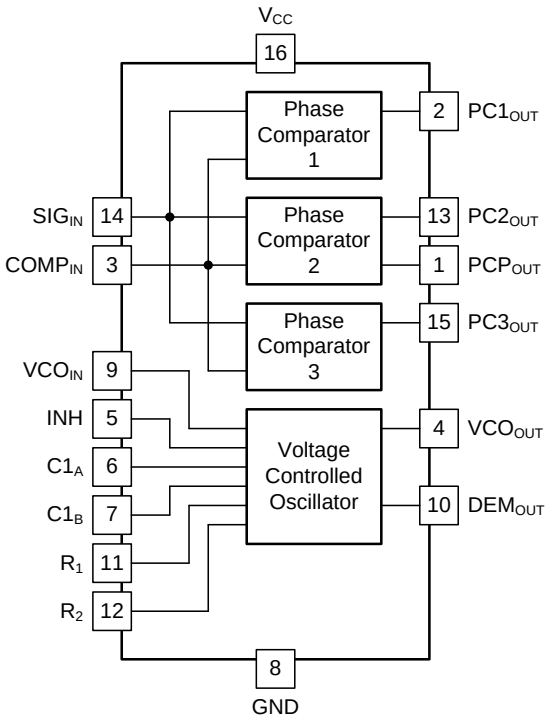
The SN74LV4046A is a high-speed silicon-gate CMOS device that is pin compatible with the CD4046B and the CD74HC4046. The device is specified in compliance with JEDEC Std 7.

The SN74LV4046A is a phase-locked loop (PLL) circuit that contains a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2, and PC3) as explained in the *Features* section. A signal input and a comparator input are common to each comparator as shown in the *Functional Block Diagram*.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive lowpass filter, the SN74LV4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear operational amplifier techniques. Various applications include telecommunications, Digital Phase Locked Loop and Signal generators.

The VCO requires one external capacitor C1 (between C1A and C1B) and one external resistor R1 (between R1 and GND) or two external resistors R1 and R2 (between R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required. The high input impedance of the VCO simplifies the design of lowpass filters by giving the designer a wide choice of resistor or capacitor ranges. In order not to load the lowpass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected through a frequency divider. The VCO output signal has a specified duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

7.2 Functional Block Diagram



7.3 Feature Description

There are three choices for the Phase Comparators in this device which are listed as below:

- Phase comparator 1 (PC1) is an Exclusive OR network. The average output voltage from PC1, fed to VCO input through the low pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the compartor input ($COMP_{IN}$) as shown in Figure 7. The average of V_{DEM} is equal to 1/2 VCC when there is no signal or noise at SIG_{IN}, and with this input the VCO oscillates at the center frequency (fo).
- Phase comparator 2 (PC2) is an Edge-Triggered Flip-Flop. This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a three-state output stage. The circuit functions as an up-down counter where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The average output voltage from PC2, fed to the VCO through the lowpass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$as in Figure 8.
- Phase comparator 3 (PC3) is an positive Edge-Triggered RS Flip-Flop. This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The average output from PC3, fed to the VCO through the lowpass filter and seen at the demodulator at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Figure 9.

The excellent VCO linearity is achieved by the use of linear operational amplifier techniques. It has low standby power consumption using VCO inhibit control. Wide operating temperature range from –40°C to 125°C along with an optimized power supply voltage range from 3 V to 5.5 V.

7.4 Device Functional Modes

The SN74LV4046A device does not feature any special functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The most common use for the digital phased-locked loop (PLL) device is to match the VCO output to the same phase as the incoming signal and produce an error signal (DEM_{OUT}) that indicates the amount of phase shift required for the match. This can be used as part of many complex systems.

8.2 Typical Application

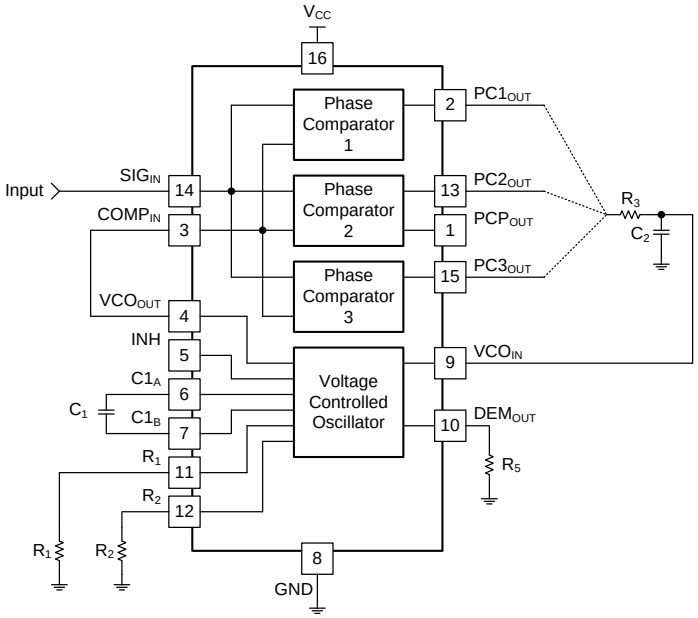


Figure 9. SN74LV4046A Digital Clock Signal Phase Comparison Application

Typical Application (continued)

8.2.1 Design Requirements

Table 1 and Table 2 lists the design requirements of the SN74LV4046A.

Table 1. Component Selection Criteria(1)

COMPONENT	VALUE
R1	3 kΩ to 50 kΩ
R2	3 kΩ to 50 kΩ
R1 || R2	> 2.7 kΩ
C1	> 40 pF
R3	1 kΩ
C2	1 uF
R5	50 kΩ to 300 kΩ

(1) R1 between 3 kΩ and 50 kΩ
R2 between 3 kΩ and 50 kΩ
R1 + R2 parallel value > 2.7 kΩ
C1 > 40 pF

Table 2. C_{PD} (1)

CHIP SECTION	C_{PD}	UNIT
Comparator 1	120	pF
VCO	120	

(1) R1 between 3 kΩ and 50 kΩ
R2 between 3 kΩ and 50 kΩ
R1 + R2 parallel value > 2.7 kΩ
C1 > 40 pF

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   – V_{IH} and V_{IL} for each input can be found in *Electrical Characteristics*.
2. Recommended Output Conditions:
   – Valid load resistor values are specified in *Electrical Characteristics*.
3. Frequency Selection Criterion:
   – Frequency data is found in *Electrical Characteristics*.

8.2.3 Application Curves

Table 3 lists the application curves in the *Typical Characteristics* section.

Table 3. Table of Graphs

GRAPH TITLE	FIGURE
Average Output Voltage vs Input Phase Difference	Figure 6
Average Output Voltage vs Input Phase Difference	Figure 7
Average Output Voltage vs Input Phase Difference	Figure 8

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage ratings located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply. a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

10 Layout

10.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 10 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

10.2 Layout Example

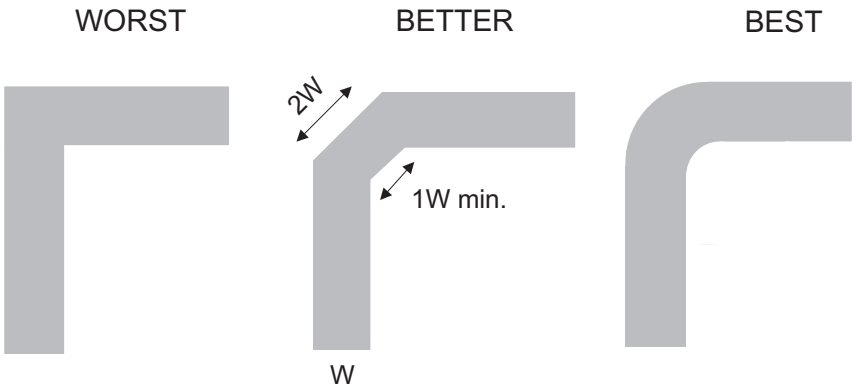


Figure 10. Trace Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4046AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4046A	Samples
SN74LV4046AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4046AN	Samples
SN74LV4046ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4046AN	Samples
SN74LV4046ANS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4046A	Samples
SN74LV4046ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4046A	Samples
SN74LV4046APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples
SN74LV4046APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW046A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

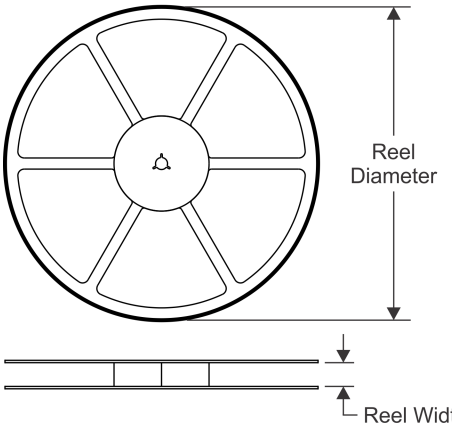
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

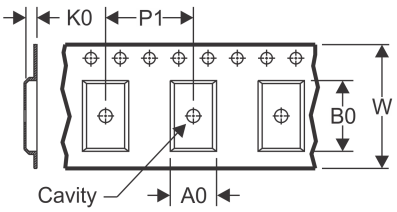
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

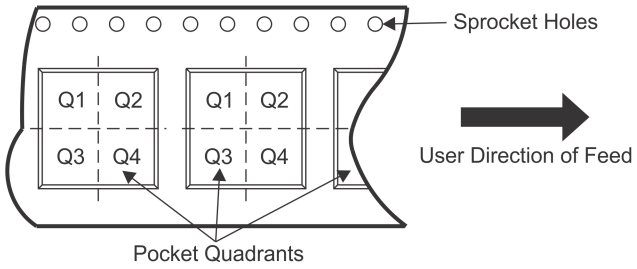


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

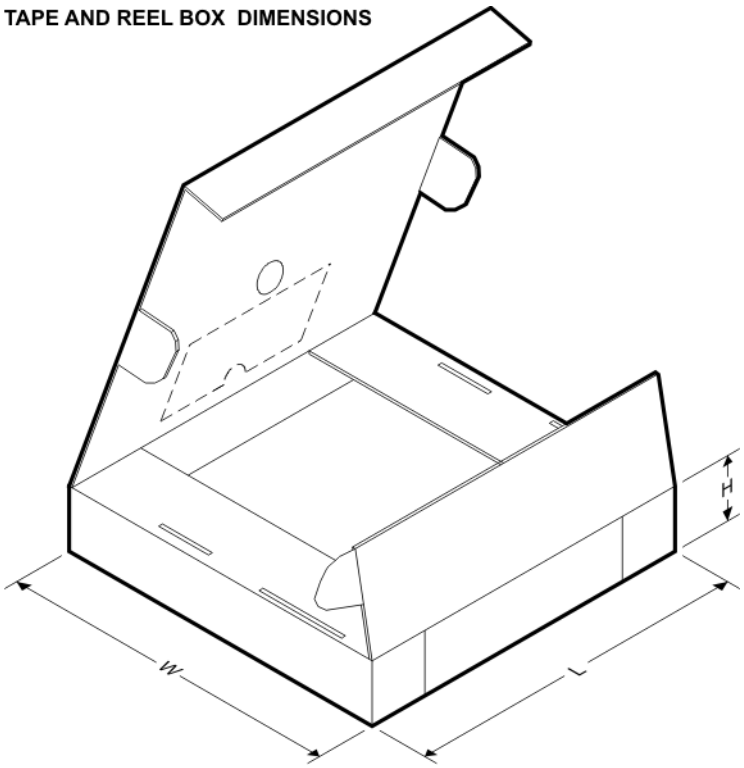
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4046ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4046ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4046ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4046APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



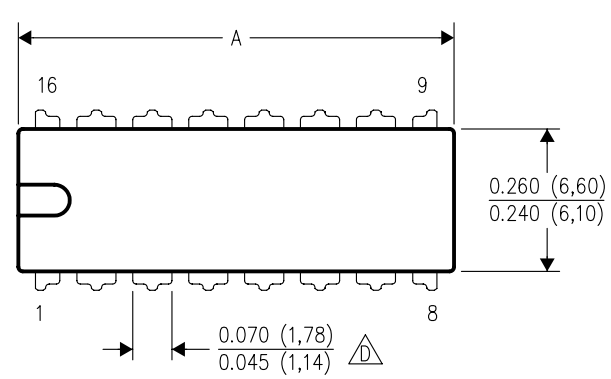
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4046ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV4046ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4046ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV4046APWR	TSSOP	PW	16	2000	367.0	367.0	35.0

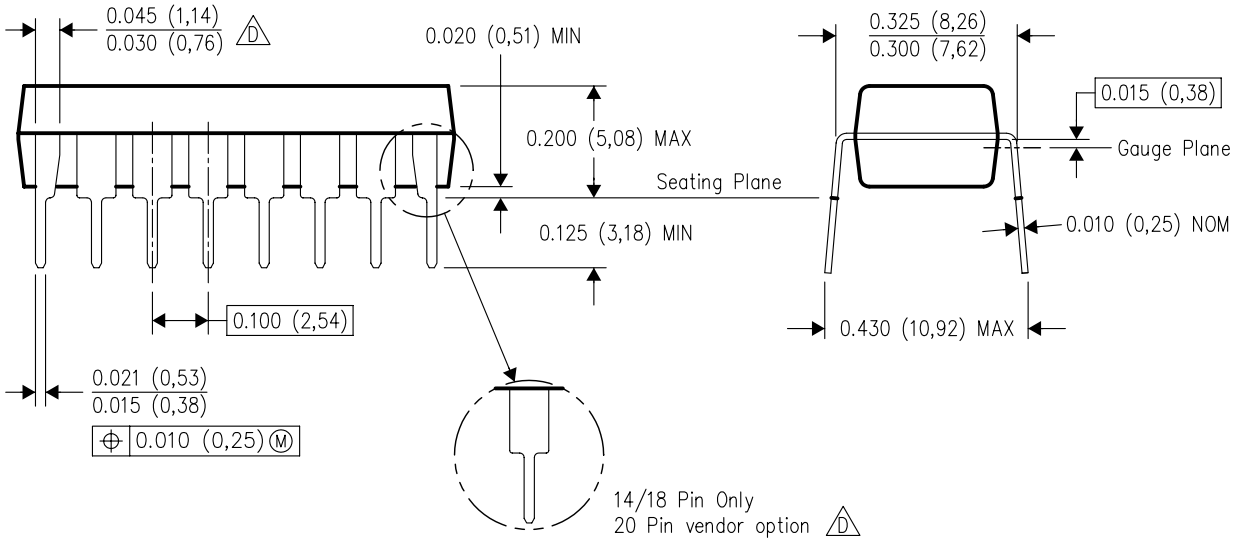
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



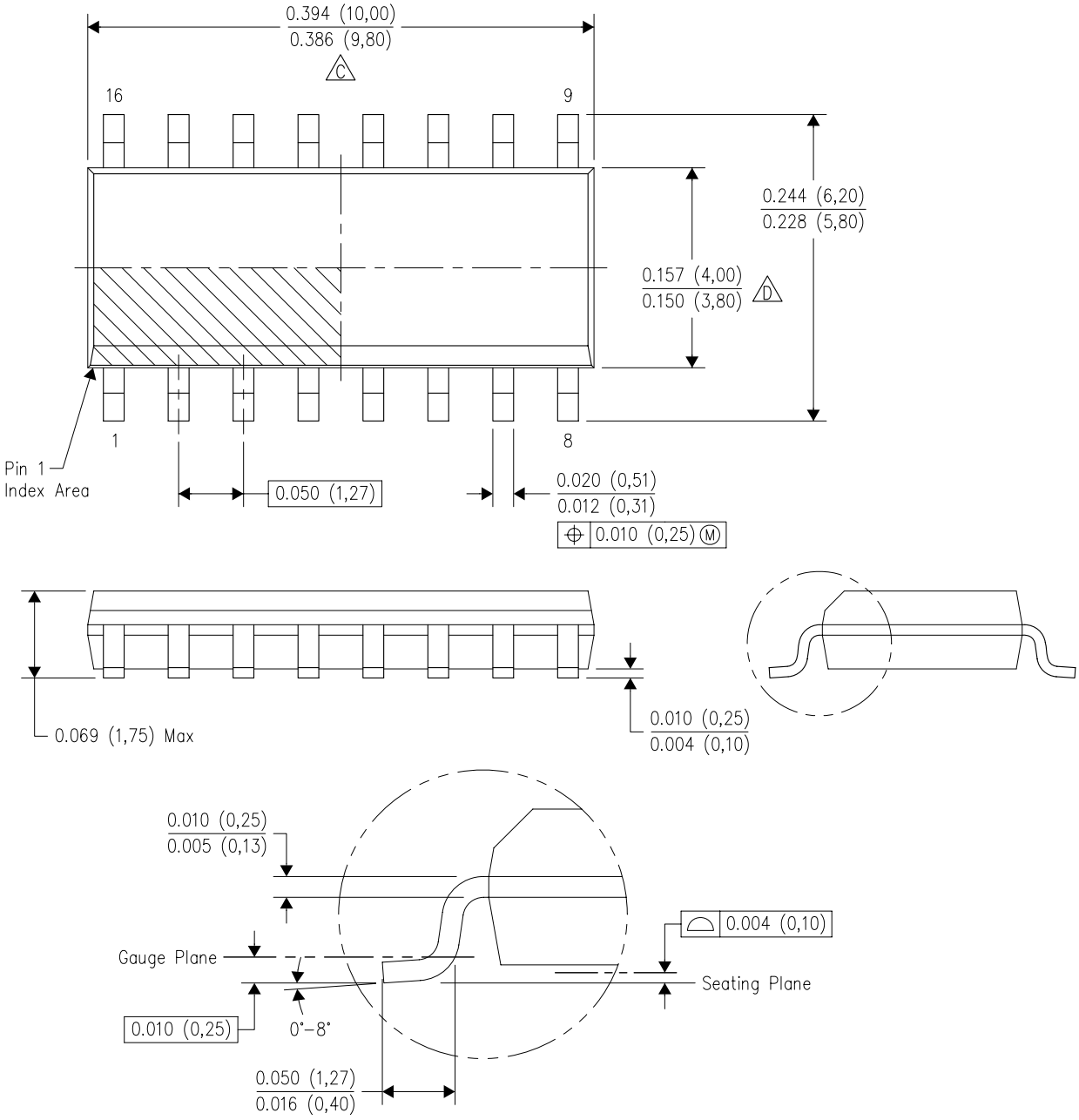
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

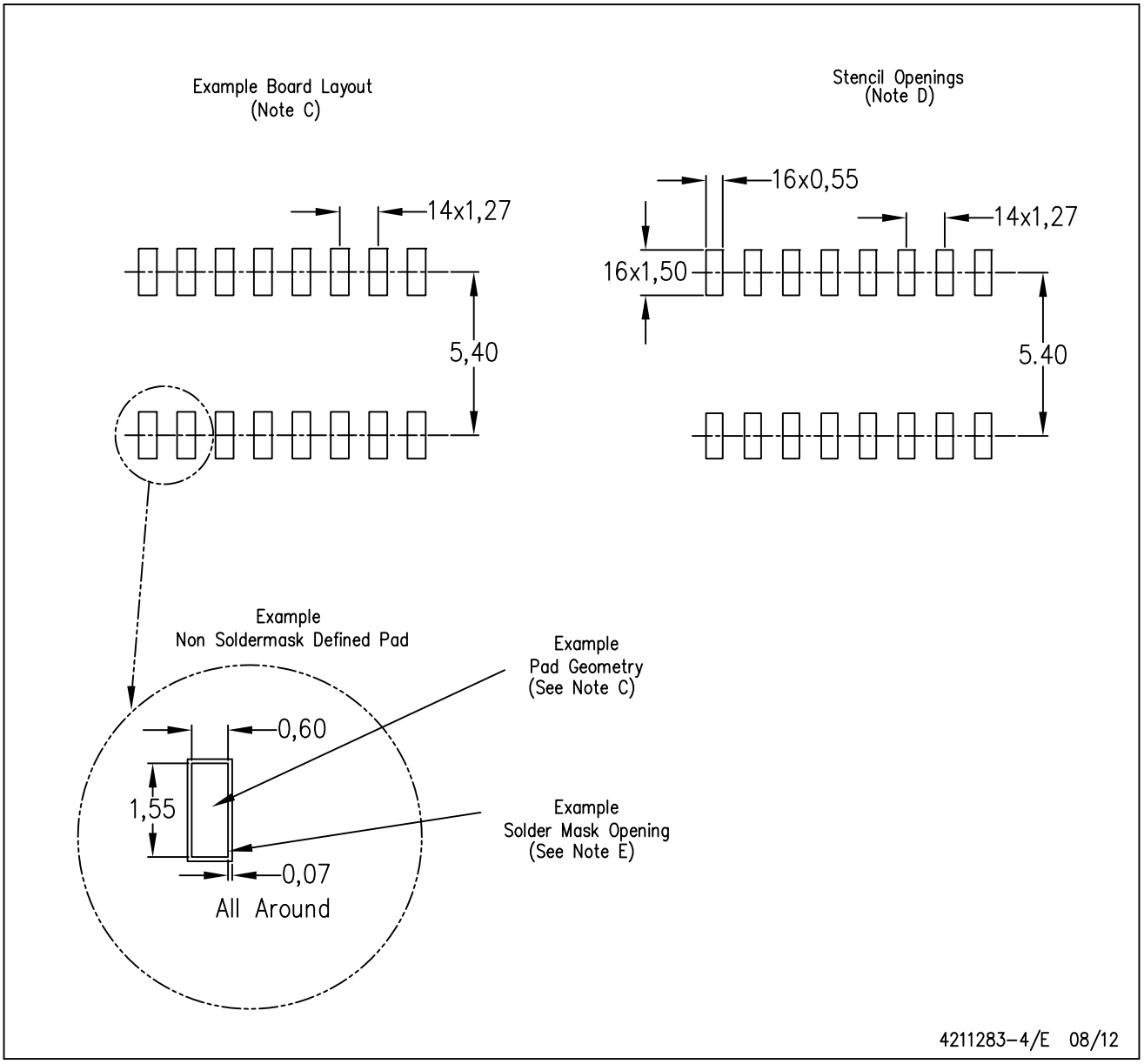
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



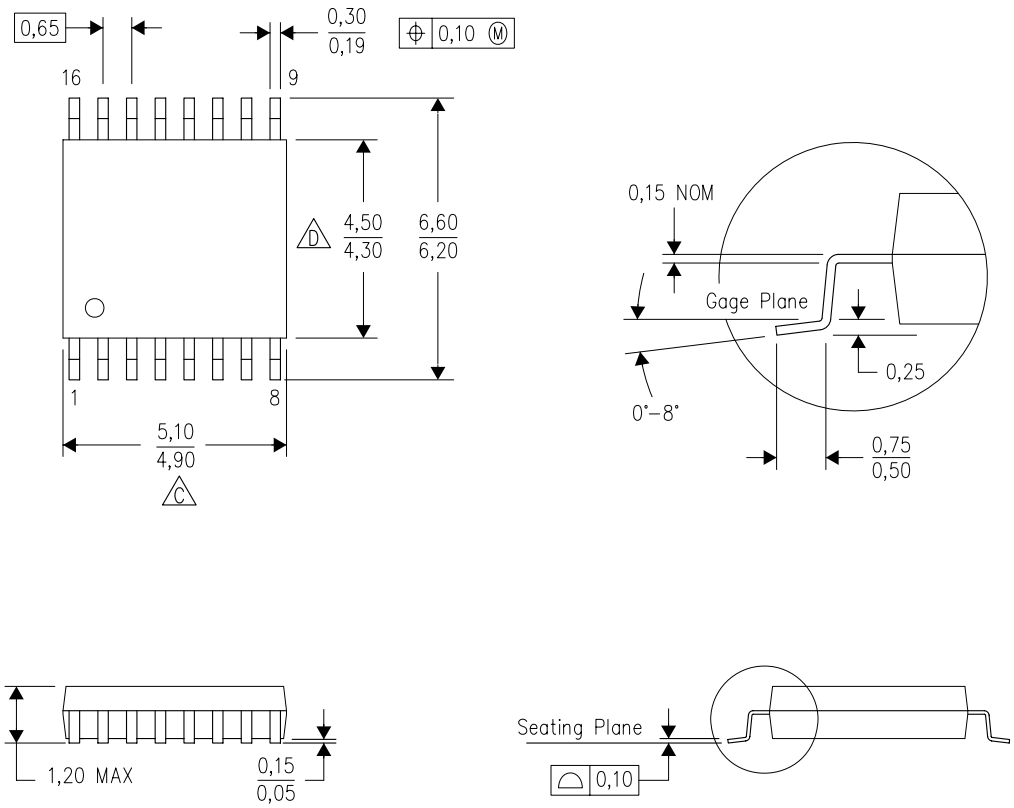
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

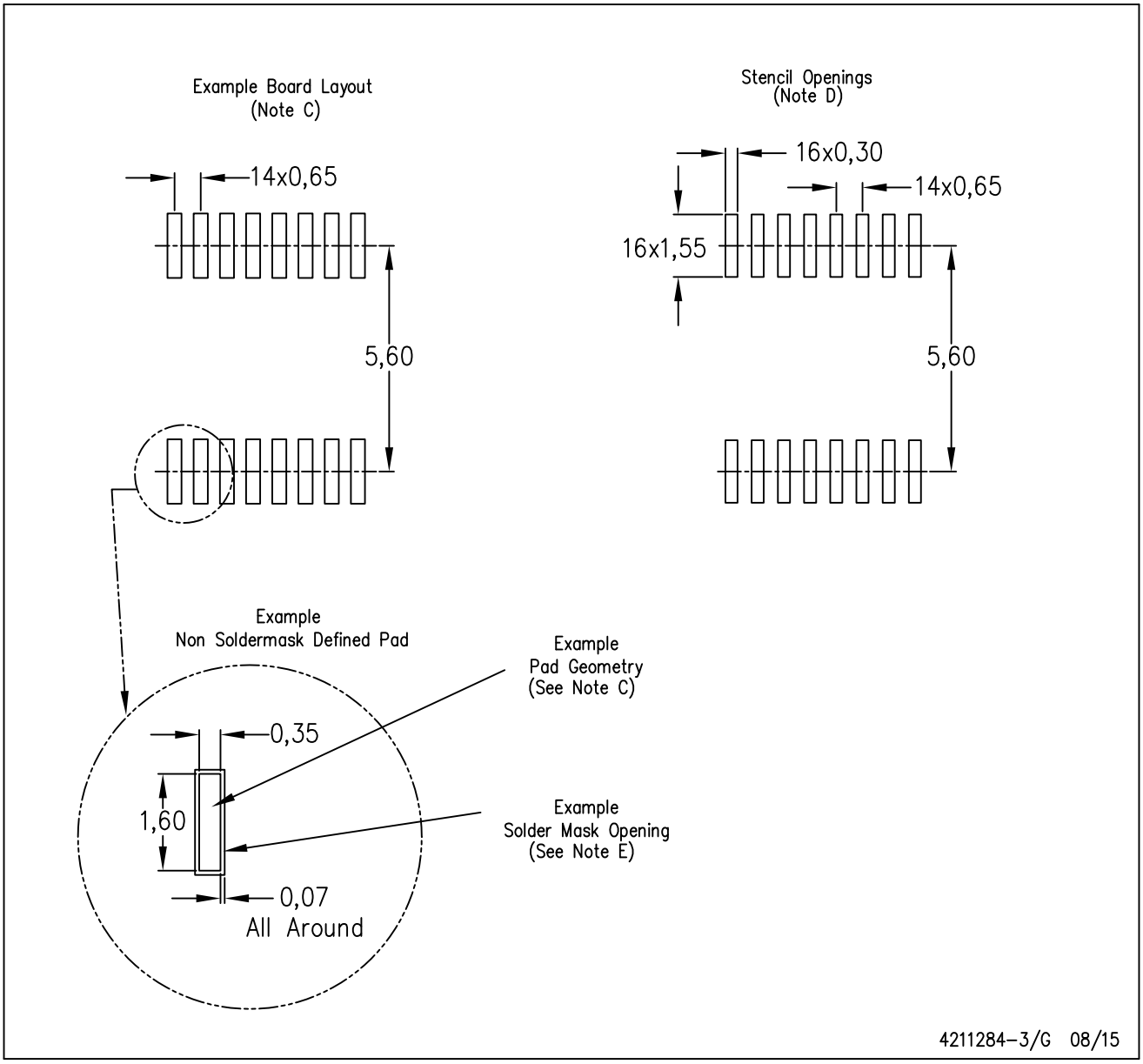
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

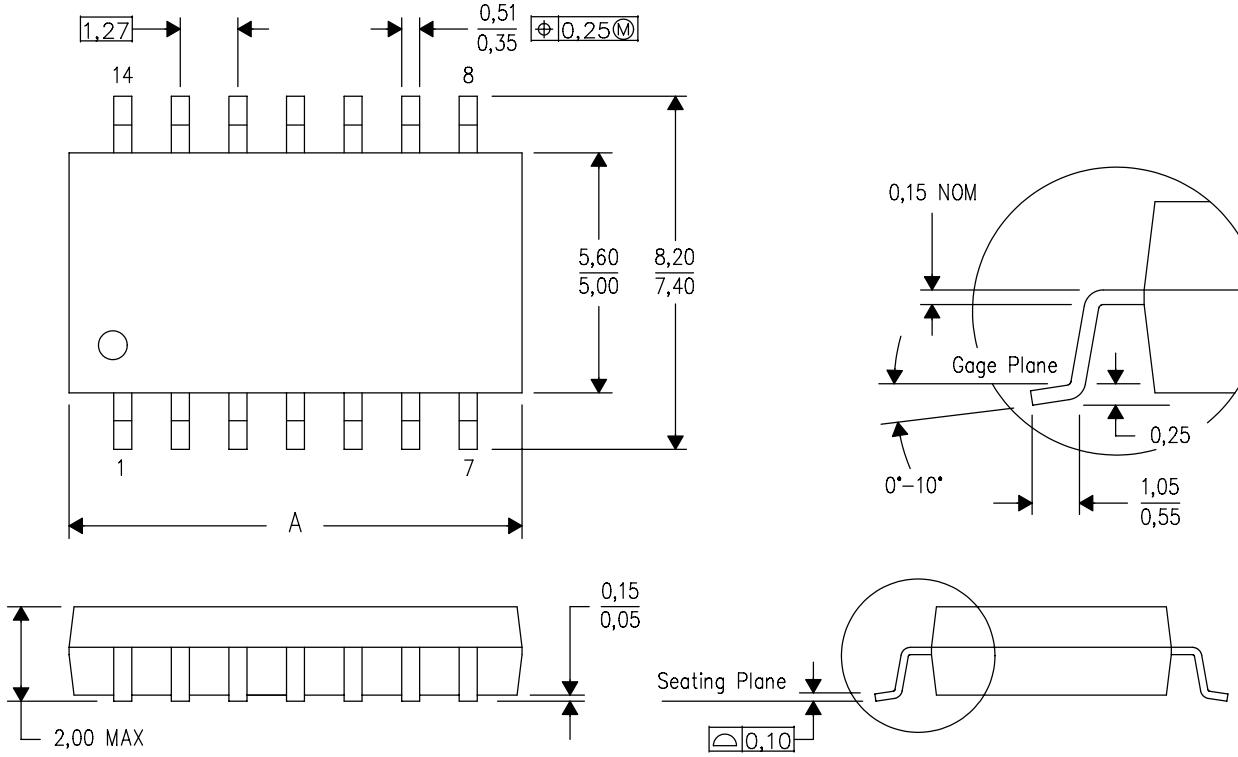


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265