Application Report
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Bus-Hold Circuit

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ABSTRACT

When designing systems that include CMOS devices, designers must pay special attention to the operating condition in which all of the bus drivers are in an inactive, high-impedance condition (3-state). Unless special measures are taken, this condition can lead to undefined levels and, thus, to a significant increase in the device's power dissipation. In extreme cases, this leads to oscillation of the affected components, which has a negative effect on both the reliability – in terms of both functioning and lifetime – and the electromagnetic compatibility of the entire system. This application report addresses a range of circuit design features that minimize these problems. The main purpose of this application report is to present a novel bus-hold circuit that TI™ has integrated into a wide range of modern bus-interface devices. This bus-hold circuit is the ideal way of meeting the demands discussed here, thus helping to ensure the functional reliability of a system.

Contents

List of Figures

List of Tables

1 Introduction

In recent years, CMOS technology has become the technology of choice for development and subsequent production of highly integrated (VLSI) circuits because of the high complexity and low power consumption that can be achieved with these types of circuits. Also, the technology has proved itself with less complex devices, such as the SN74AHC and SN74AC logic families, as well as with the SN74LVC and SN74ALVC logic families developed for use with lower supply voltages. Furthermore, it is possible for important parameters, such as propagation delay time and drive capability, to achieve properties similar to those found in the bipolar circuits that previously dominated this field. In this respect, the particularly powerful SN74ABT and SN74LVT BiCMOS devices, which combine the strengths of CMOS circuits (low power consumption) with those of bipolar circuits (lower propagation delay time and greater drive capability), deserve mention.

When using these integrated CMOS and BiCMOS devices, the designer also must consider certain properties of these devices that the specification sheets deal with only briefly, if at all. This includes, for example, the behavior of the input stages of these components when no defined logic level is established.

2 Behavior of CMOS Input Stages

The input stage of a CMOS circuit consists of an inverter (see Figure 1) that decouples the following internal circuit from the external signal source. Due to the high degree of voltage amplification, this stage regenerates the voltage swing and the rise time of the incoming signal.

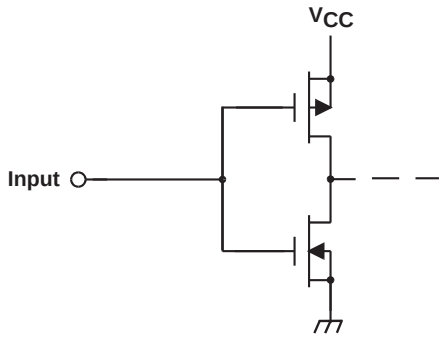

Figure 1. Input Stage of a CMOS Circuit

If there is a valid logic level at the input – the gates of the MOS transistors – of such a circuit, the P-channel transistor conducts if the input is a low level, and the N-channel transistor conducts if the input is a high level. In either case, the complementary transistor is turned off, so that, in both cases, no current flows through the transistors. This is the reason for the low power consumption when CMOS circuits are at rest.

If, on the other hand, an input voltage between these defined logic levels ($V_t < V_i < V_{CC} – V_t$; with V_t = threshold voltage of the transistors) is applied to such an input, both transistors are more or less conducting, leading to an increase in the device's supply current. Figure 2 shows the supply current in relation to the input voltage for AHC and AC devices. In AHC devices, the supply current reaches a peak value of I_{CC} = 2 mA, while in the faster AC devices, currents of about 5 mA can be expected. Accordingly, the device's power consumption also increases, so that, with undefined logic levels, the advantages of CMOS circuit technology are not realized.

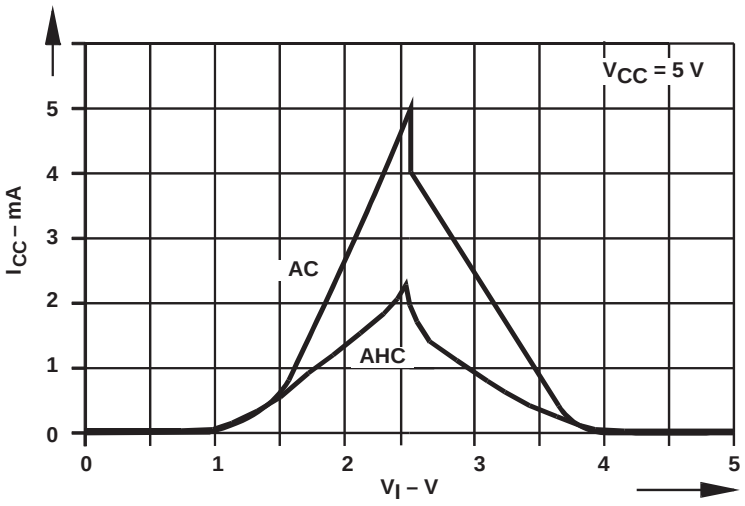

Figure 2. Power Consumption of CMOS Input Stages vs Input Voltage

The effects shown in Figure 2 are typical of all CMOS circuits. Accordingly, this phenomenon also must be taken into account when dealing with VLSI circuits, such as microprocessors or memory devices.

Furthermore, CMOS device data sheets recommend the slowest possible rise time for the input signal to ensure optimum functioning of components. However, slowly rising edges cause fast integrated circuits to malfunction and can, in extreme cases, lead to destruction of the circuit. Figure 3 shows an inverting buffer stage with the parasitic inductances of the package leads (L_P) and the capacitive load (C_L) at the output. If, for example, the input voltage of this kind of circuit rises from low to high, and reaches the threshold voltage, the output switches abruptly from high to low due to the high voltage gain, and discharges C_L. The discharge current causes a voltage drop at the package inductance of the ground terminal, which raises the internal ground potential of the integrated circuit, meaning that the voltage difference between the input and the internal ground potential decreases, giving the appearance of a decrease of the input voltage. If, due to too slow a slew rate, in the meantime, the input voltage has not risen sufficiently, the input stage switches to the opposite state, and the same process repeats, but with the opposite polarity. This process repeats periodically, with the periodicity of the oscillation determined by the device's propagation delay time. In fast logic circuits, the oscillation is above 50 MHz.

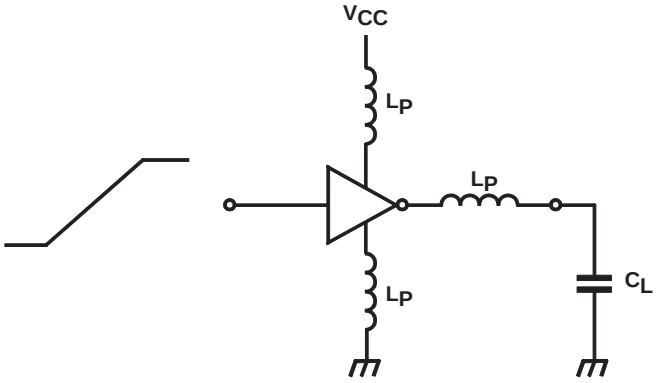

Figure 3. Parasitic Components Causing Circuit Oscillation

Figure 4 shows the oscillation at the output of a CMOS circuit whose input is triggered by a signal with a rise time of t_r = 200 µs. Rise and fall times of this order must be taken into account if, for the operating conditions discussed below, special circuit design techniques are not incorporated to ensure defined signal levels and slew rates.

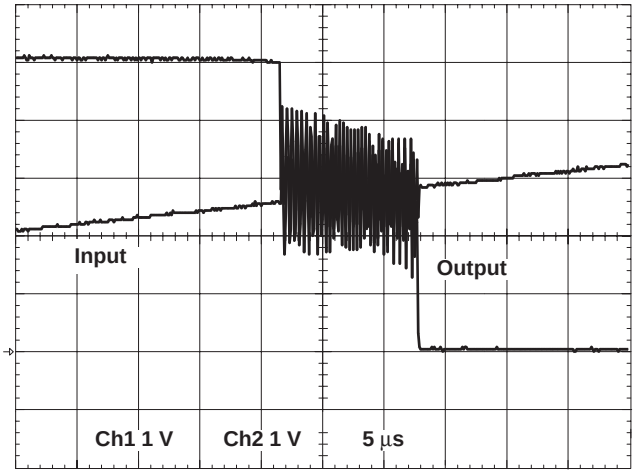

Figure 4. Oscillation at the Output of a CMOS Circuit Whose Input Is Triggered by a Signal With a Rise Time of t_r = 200 ns

In addition to a significant increase in system noise, which compromises the system's electromagnetic compatibility, the circuit's power dissipation rises unacceptably. In MOS circuits, the fact that the transistor's resistance increases as the temperature rises becomes an advantage because this often avoids overloading the circuit. In contrast, with bipolar devices the transistor's current gain increases as the temperature rises. This also applies to BiCMOS devices, such as the SN74ABT and SN74LVT series. Because there are no factors that would reduce power dissipation, these circuits often are overloaded when they oscillate. Experience shows that permanent degradation of devices can be expected if the oscillation lasts for several seconds.

3 Problems Posed by Bus Systems

If only unidirectional transmission lines are involved, the previously mentioned phenomenon of increased power dissipation and oscillation can safely be ignored. With unidirectional transmission lines there is a driver circuit that always is active at one end of the line, thus ensuring defined logic levels (see Figure 5).

Figure 5. Unidirectional Transmission Line

Bus systems (see Figure 6), in which transmission is bidirectional between individual stations, the operating condition in which all of the 3-state output bus drivers are in an inactive, high-impedance state in a 3-state device must be given special attention. Because there is no driver to impose a defined logic level on the lines, a voltage develops that is determined by the leakage currents of the connected components, thus giving rise to an entirely undefined voltage level. In the literature, this state is described as floating inputs. In the case of Widebus™ circuits with 16 channels and AC technology, with a supply voltage of V_{CC} = 5 V, the supply current rises to $I_{CC} = 16 \times 5$ mA = 80 mA (see Figure 2). Under this condition, the power consumption of this component alone increases to 400 mW, which no longer is low power consumption.

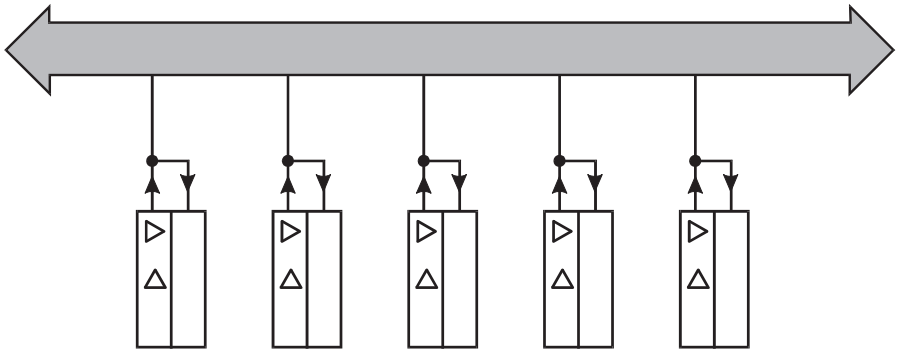

Figure 6. Bidirectional Transmission Line of a Bus System

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4 Avoidance of Undefined Levels in Bus Systems

4.1 Avoidance of Undefined Levels Via Appropriate Bus Control

A simple way to prevent an undefined logic level in bus systems is to ensure, via appropriate control of the bus, that the duration of the inactive state (3-state) is so short that harmful voltages cannot build up. The advantage of this method is that it does not involve any additional costs from using special components.

If we first consider a single device and assume that the maximum leakage current, I_{OZ}, of a 3-state output in the high-impedance state amounts to 10 μA (see Table 1), and that the input and output capacitance, C_S, of the integrated circuit plus the parasitic capacitance of the connection lines (which are related to this particular component) amount to about 20 pF, the voltage on an inactive line drifts away from the defined logic level at a rate that can be calculated using equation 1.

$$\frac{dV}{dt} = \frac{I_{OZ}}{C_S} = \frac{10\ \mu A}{20\ pF} = 0.5\ V/\mu s \qquad (1)$$

If a drift away from the logic level of a maximum of 1 V is permitted, so that the supply current of the affected input stage has not yet risen too sharply (see Figure 2), the bus may remain in an inactive state (3-state) for a maximum of 2 μs. Usually, more than one device is connected to a bus. Where several components are connected to a bus, both their leakage currents and their capacitances are added, and the time constant calculated in equation 1 does not change.

In the data sheets, semiconductor manufacturers give conservative values for the leakage current, I_{OZ}. When determining these values, the leakage current is measured at an ambient temperature of T_A = 25°C and the maximum values to be expected at operating limits are then calculated. However, semiconductor physics predicts a doubling of the leakage current when T_A rises 10°C. Thus, if T_A rises from 25°C to 125°C, the leakage current would rise by a factor of 2^{10} = 1024. However, this fundamentally correct assumption leads to considerably higher values than are measured in practice. Accordingly, one can assume that typical output leakage currents are smaller than the specification sheet limits by an order of magnitude, or more.

Another method of avoiding undefined logic levels in inactive buses involves the last active bus-interface device remaining active (monitored by suitable control logic) until another bus driver takes over control of the line. The PCI bus uses this method, whereby inactive bus phases of any length can be bridged without the extra cost of adding components.

4.2 Pullup Resistors

Another way of ensuring a defined level during a bus's inactive phase is by tying the lines to the supply voltage or to the ground potential via resistors (R_p in Figure 7). This connection pulls inactive lines to a defined logic level (either high or low).

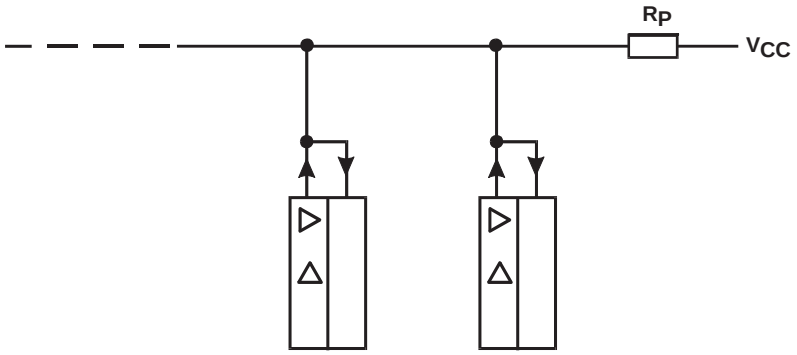

Figure 7. Creating a Defined Level Using Pullup Resistors

Getting the correct impedance for the resistors is not always easy. The resistors should not significantly increase the system's power dissipation; therefore, high-impedance resistors are required (R_p = 10 kΩ to 50 kΩ). The low leakage current of CMOS circuits would permit that. However, it also should be remembered that fast logic circuits need short rise times, t_r, at the inputs to avoid unwanted oscillation which, as mentioned previously, can lead to system malfunction and, possibly, degradation of components. The desired pullup or pulldown resistance, R_p, can be calculated using equation 2:

$$R_p = \frac{t_r}{2.2 \times C_S \times n} \tag{2}$$

Where:

n = number of devices connected to the line

Modern logic circuits and corresponding VLSI circuits demand input signals whose slew rate is $\Delta t/\Delta V$ < 10 ns/V. In the case of a supply voltage of V_{CC} = 5 V, that corresponds to a signal rise or fall time of $t_{r/f} \approx$ 50 ns. Assuming that ten devices, each with a capacitance of C_S = 20 pF per component, are connected to the bus, and that the devices require a maximum rise time t_r = 50 ns, resistance R_p can be calculated using equation 3.

$$R_p = \frac{50\ \text{ns}}{2.2 \times 20\ \text{pF} \times 10} \approx 110\ \Omega \tag{3}$$

When using modern bus-interface circuits whose advantage is their low quiescent current consumption, this outcome is unacceptable. These resistors consume far more current than the logic circuit itself. After all, many logic circuits are not capable of providing the output current needed for such a low-impedance load.

4.3 Bus-Hold Circuit

A considerably more elegant solution is to ensure a defined level for inactive bus lines via bus-hold circuits (see Figure 8). These circuits feed back the output signal of a noninverting buffer circuit to the input via the resistor R_f. This creates a bistable circuit (latch). To understand the circuit, one first assumes that an active bus driver has switched the line to high level. This means that a high level also exists at the output of the bus-hold circuit buffer. Thus, no current flows via the feedback resistor R_f. The leakage currents of the circuit, which are in the microampere region, determine power consumption of the bus-hold circuit. If the output of the bus driver in question changes to the inactive state, the bus-hold circuit holds the high level via the feedback resistor R_f, so that now, apart from leakage currents, no current flows. Only during the transition of the line from high to low, or vice versa, time current spikes, which are unavoidable in CMOS circuits, occur in the bus-hold circuits. However, the dynamic power dissipation involved is several orders of magnitude less than when using pullup resistors described previously.

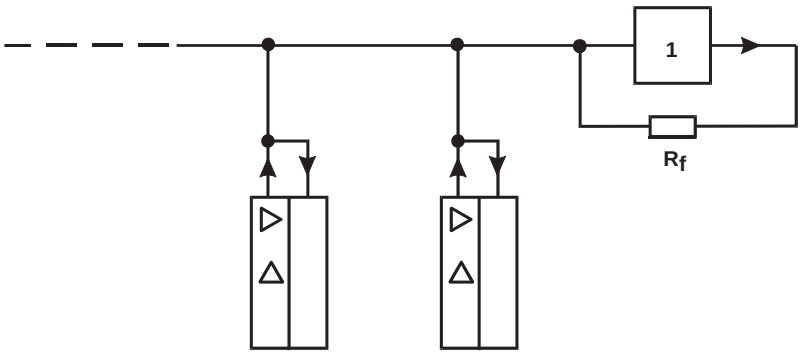

Figure 8. Bus With Bus-Hold Circuit

This kind of circuit can be built simply by using a noninverting buffer circuit, such as the SN74AHCT541, if, as noted previously, the outputs are fed back to the inputs via resistors R_f. The propagation delay time of these components is, in this case, of secondary importance. Whether the CMOS-compatible version (SN74AHC541) or the TTL-compatible version (SN74AHCT541) is used depends on the switching thresholds of the bus-interface device. The impedance of the feedback resistor R_f is decided, taking into account the fact that the voltage drop V_r at the resistor still ensures a sufficient logic level, even at the maximum leakage current I_{OZ} to be expected from the connected devices. Here the number of bus drivers (n) connected to the bus obviously plays a part. In making the calculation it is assumed that, due to its low load, the output voltage of the buffer circuit used in the bus-hold circuit corresponds to the potential of the supply lines (V_{CC} or GND). Thus,

$$R_f \leq \frac{V_r}{I_{OZ} \times n} \tag{4}$$

If we assume that ten bus drivers are connected to the bus line and that the output leakage current of the bus drivers is I_{OZ} = 10 μA, and, if we allow a voltage drop of V_r = 1 V at the feedback resistor R_f, the resistance R_f is:

$$R_f \leq \frac{1\ V}{10\ \mu A \times 10} = 10\ k\Omega \tag{5}$$

Because with this circuit technique no charging of line capacitance is required, rather only the most recent logic level is held, problems relating to signal rise times no longer are expected. Accordingly, the circuit can be designed with considerably higher impedance, and correspondingly lower power consumption, than with the technology described in paragraph 4.2.

5 Integrated Bus-Hold Circuit

For the reasons given in the previous section, a defined logic level must be ensured on bus lines in the high-impedance state. Thus, it makes sense to integrate bus-hold circuits in the inputs of bus-interface devices. Doing so means designers no longer have to concern themselves with the problem, and additional components are not needed to ensure defined logic levels under all operating conditions, markedly improving the reliability of the whole system.

Inputs of all newly developed bus-interface devices have a bus-hold circuit. The additional letter H in the type designation indicates this feature. An ABT device has no bus-hold circuit, while an ABTH device has the additional bus-hold function. The same applies to LVT and LVC circuits versus ALVTH, LVTH, LVCH, and ALVCH circuits.

The additional cost of the bus-hold function in bus-interface devices is not excessive. Figure 9 shows the simplified input circuit found in the modern CMOS and BiCMOS families. The input signal is amplified in the Q1/Q2 inverter. Simultaneously, this stage decouples the following internal circuit from the exterior of the device. The actual bus-hold circuit consists of transistors Q3 and Q4. The signal, after again being inverted, thus going through 360 degrees total, then returns to the circuit's input. From the resulting feedback the two inverters create a latch that continually tries to reach one of its two stable states – high or low. If there is a high level at the circuit input, the output of the second inverter also is high. Therefore, P-channel transistor Q3 conducts. If the input voltage of the integrated circuit drops for any reason, a current is supplied via this transistor, which counteracts any further drop of the line voltage. If, conversely, there is a low level at the circuit input, N-channel transistor Q4 conducts and compensates for the leakage current of the interface devices connected to the bus.

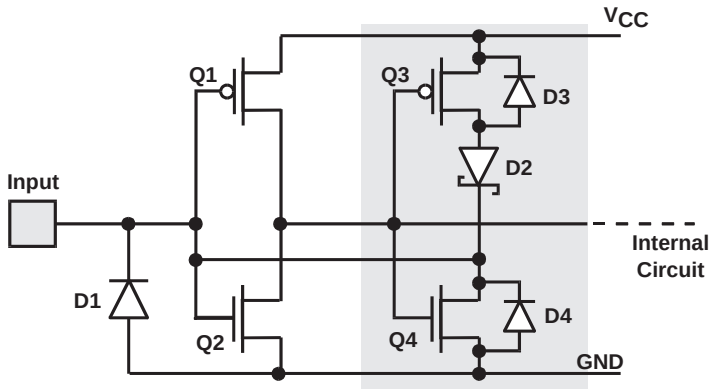

Figure 9. Simplified Circuit Diagram of Bus-Hold Circuits

Transistors Q3 and Q4 in the bus-hold circuit compensate for both their own leakage currents and for those of the connected circuits. Otherwise, they should load the circuit as little as possible, and because of this, these transistors have a comparatively high forward resistance in the on state. (R_{dson} = 5 kΩ). Figure 10 shows the input characteristics of typical bus-interface devices with the bus-hold function.

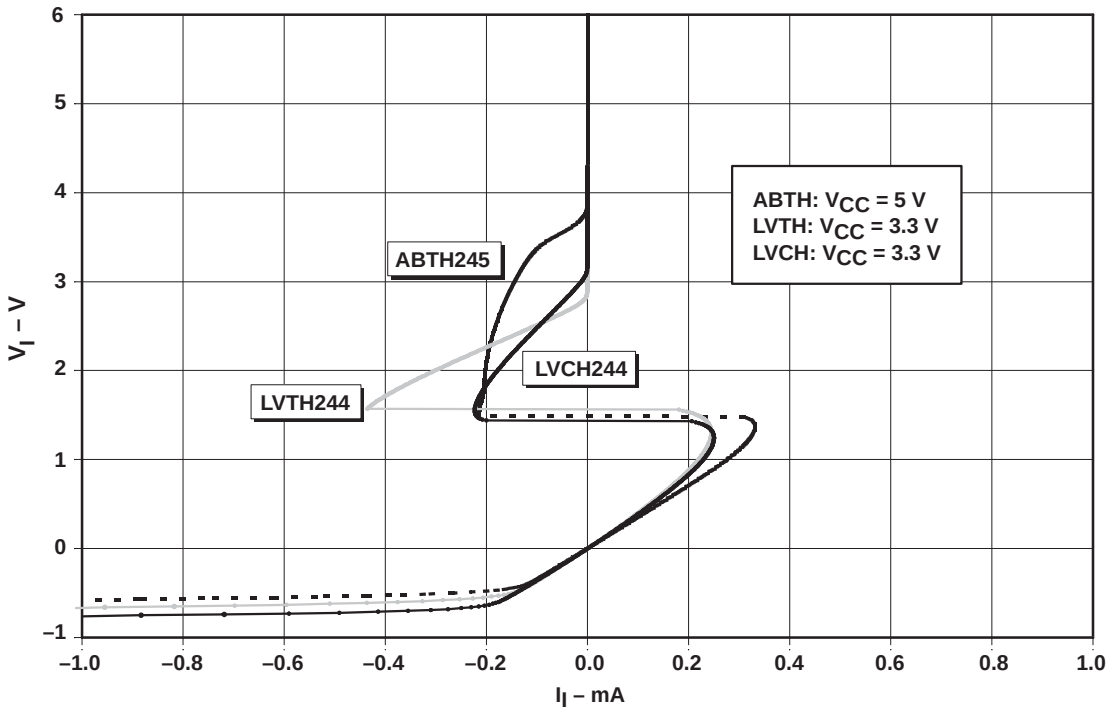

Figure 10. Characteristic Input Curve of Bus-Interface Devices With the Bus-Hold Function

The switching threshold of bus-hold circuits is about 1.5 V in the devices depicted in Figure 10, matching the switching threshold of the appropriate logic circuits. If the input voltage is below this level, N-channel transistor Q4 conducts ($R_{dsontyp}$ = 5 kΩ). This transistor also remains conducting, even when the input voltage falls below 0 V. If the input voltage drops below –0.7 V, clamping diode D1 conducts, which protects the circuit against destruction due to electrostatic discharge and limits negative undershoot stemming from line reflection. Above the cited threshold voltage, P-channel transistor Q3 conducts, pulling the line level to the high potential. Diode D2 in Figure 9 prevents the parasitic diode D3 parallel to transistor Q3 from conducting if the input voltage has a higher positive value than the supply voltage. This last case might occur, for example, when signals with a voltage swing of 5 V control the bus-hold circuit, which is itself operated by a supply voltage of V_{CC} = 3.3 V. This also ensures that the bus-hold circuit remains at the high-impedance state with the supply voltage off. The upper diagram shows the influence of this diode in that the bus-hold circuit already becomes high impedance at markedly less than 3.3 V. In the case of ABTH devices, whose typical high level also is about 3 V despite a supply voltage of 5 V, it would not make sense for the bus-hold circuit to pull the potential significantly above this level. Accordingly, as Figure 10 shows, additional circuit features limit the rise in voltage.

6 Application Information

6.1 Additional Load Caused by Bus-Hold Circuits

The influence of, and the additional load caused by, the bus-hold circuits can be investigated using the example in Figure 11. In this example, a digital signal processor (TMS320C6xx), eight bus-interface devices (SN74LVCH245) with the bus-hold function, and one bus-interface device (SN74AHC245) without the bus-hold function are connected to a system bus. Semiconductor manufacturers still supply devices with 3-state outputs, but without the bus-hold function under discussion. These include, among others, microprocessors, such as digital signal processor TMS320C6xx, or integrated circuit SN74AHC245 used in this example. This leads, in some applications, to a combination of different types of logic circuits. The example illustrated here exemplifies bus systems where circuits with and without the bus-hold function are combined with each other.

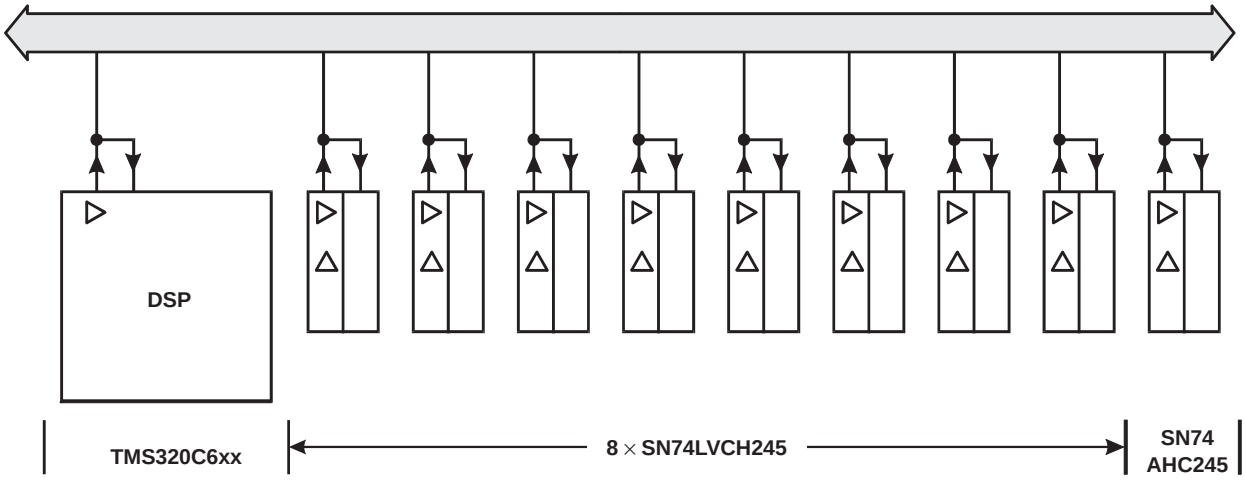

Figure 11. A Simple Bus System

In the data sheets for the SN74LVCH245 and SN74AHC245 devices, and for the digital signal processor TMS320C6201, details of the inputs and outputs are given in Tables 1, 2, and 3.

Table 1. Specifications of the 3-State Outputs With Bus Hold, SN74LVCH245

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = 12 mA	3 V	2.4		V
V_{OL}	I_{OL} = 12 mA	3 V		0.4	V
$I_{I(hold)}$	V_I = 0.8 V	3 V	75		µA
	V_I = 2 V	3 V	–75		µA
	V_I = 0 to 3.6 V	3.6 V		500	µA

Table 2. Specifications of the 3-State Outputs, SN74AHC245

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = 4 mA	3 V	2.48		V
V_{OL}	I_{OL} = 4 mA	3 V		0.44	V
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V		2.5	µA

Table 3. Specifications of the 3-State Outputs, TMS320C6201

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = 12 mA	3.14 V	2.4		V
V_{OL}	I_{OL} = 12 mA	3.14 V		0.4	V
I_{OZ}	V_O = 0 V or D_{VDD}	3.46 V		10	μA

With respect to sufficient logic levels (V_{IL} < 0.8 V, V_{IH} > 2.0 V), the bus-hold circuit in the SN74LVCH245 device supplies a current of $I_{I(hold)}$ > |75 μA|. Assuming a maximum leakage current of I_{OZmax} = 10 μA for 3-state outputs, a single bus-hold device would almost be capable on its own to compensate the leakage currents of the other nine devices connected to the bus and ensure defined levels on the bus lines. This is all the more so that, in practice, as noted above, none of the integrated circuits show the maximum output leakage currents I_{OZ} given in the data sheets. Due to the large variation of the transistor parameters caused by production variations and changes in supply voltage and temperature, the maximum current $I_{I(hold)}$ might rise to 500 μA (see Figure 10). In the example shown here, a single active output also must be able to charge/discharge the device's capacitance and to switch eight inputs with bus hold. The outputs of the LVCH and AHC devices, and the processor, can supply a current of $8 \times I_{I(hold)max}$ = 4 mA (see Tables 1, 2, and 3).

6.2 Influence on the Circuit's Power Loss

When using bus-hold circuits, a current, $I_{I(hold)}$, flows during signal state transition from low to high and from high to low for the duration of the signal slope, which has an influence on the system's power consumption. The resultant power dissipation can be calculated approximately.

According to Table 1, the maximum current in bus-interface device SN74LVCH245 is $I_{I(hold)max}$ = 500 μA at V_{CCmax} = 3.6 V. Because the current during a signal transition follows a roughly triangular shape, we can derive the power consumption, P_{hold}, caused during signal transitions by the bus-hold circuits:

$$P_{hold} = \frac{1}{2} \times V_{CC} \times I_{I(hold)max} \times t_r \times 2 \times f \times n \quad (6)$$

Where:

t_r = signal rise or fall time
f = frequency of signal exchange
n = number of inputs with a bus-hold circuit
$I_{I(hold)max}$ = maximum bus-hold circuit input current

For the SN74LVCH245 device, n = 8. If we assume that the mean frequency, f, of signal transitions at the inputs = 10 MHz, the rise time, t_r = 2 ns, yielding:

$$P_{hold} = \frac{1}{2} \times 3.6\ V \times 500\ \mu A \times 2\ ns \times 2 \times 10\ MHz \times 8 = 0.288\ mW \quad (7)$$

Equation 7 predicts that the parameter P_{hold} increases with longer rise times. In contrast, there is the dynamic power dissipation, P_{dyn}, of the circuit, which, taking the power dissipation capacitance C_{pd} = 31 pF given in the device's data sheet, can be calculated:

$$P_{dyn} = C_{pd} \times V_{CC}^2 \times f \times n = 31\ pF \times 3.6^2 \times 10\ MHz \times 8 = 320\ mW \quad (8)$$

Because power consumption P_{hold} caused by the bus-hold circuit is several orders of magnitude less than this, it safely can be disregarded.

6.3 Presetting Logic Levels

Some applications require specific logic levels on certain bus lines during the initialization phase after the supply voltage is switched on. The microprocessor queries this level and makes certain system settings (start vector, etc.) on the basis of the information it reads. In conventional bus-interface devices, the desired level is generated on the lines in question via pullup or pulldown resistors. Because the input resistances of CMOS circuits are very high, high-impedance resistors (10 kΩ to100 kΩ) do this job very well.

When using interface devices with the bus-hold function, however, additional attention has to be paid to this circuit detail. Hold circuits have an inherent tendency to generate a low level when the supply voltage is switched on. As noted previously, this circuit behaves like a latch. A comparatively large capacitance – the interconnect lines and other circuit components – is connected to its set input (the input of the integrated circuit). This capacitance is discharged when the supply voltage is switched on. This is the reason that a low level is generated there when the voltage is switched on. Because the bus-hold circuit still has a very high impedance during the first moment of the power-on phase ($V_{CC} \leq V_t$), a high-impedance pullup resistor (10 kΩ to 100 kΩ), at this point in time, would be able to put the latch into the opposite logic state and generate a high level at the input of the bus-hold circuit. However, this observation does not take into account the fact that other devices connected to this bus might couple charge into the previously mentioned capacitance during supply-voltage startup, thus forcing a different level from the one expected. In this respect, the outputs of the interface devices connected to the bus are more effective than the bus-hold circuit and an associated preset circuit. If the outputs during the power-on phase briefly enter an undesired active state, they force the bus-hold circuit to the output's state. Then, a high-impedance pullup or pulldown resistor is no longer able to change this state.

Consequently, the only way to force the device to a certain state is to place suitable low-impedance pullup or pulldown resistors. According to the maximum input current to a bus-hold circuit, $I_{I(hold)max}$ = 500 μA. This current flows when a hold-circuit threshold voltage of V_t = 1.5 V is reached (see Figure 10). Taking this figure, the value for pullup resistance, R_p, can be calculated:

$$R_p = \frac{V_{CCmin} - V_t}{I_{I(hold)max}} \tag{9}$$

If an LVCH circuit is connected to the bus, the resistance is calculated as:

$$R_p = \frac{3.0\ V - 1.5\ V}{500\ \mu A} = 3\ k\Omega \tag{10}$$

If several devices with the bus-hold function are connected to the bus, the resistance value must be reduced accordingly.

7 Summary

This application report addresses the question of how to ensure defined levels on bus lines when all bus drivers are in the inactive high-impedance state (3-state). This is of particular importance in the case of smaller CMOS-based systems where, for technical reasons, the lines cannot be terminated by a resistor network matched to the line impedance. This application report presents various different circuit options, with particular reference to a novel bus-hold circuit that TI integrates into modern bus-interface devices. This additional circuit provides an ideal combination of all the functions needed for a bus system to run properly. These include:

- Ensuring a defined logic level when the bus is in the inactive state (3-state).
- Avoiding excessive supply current due to logic levels that lie outside the limits stipulated in data sheets. To this end, a bus-hold circuit often is a must for battery-operated systems.
- The bus-hold circuit also prevents oscillation of the bus-interface devices provoked by undefined logic levels. Combined with appropriate power consumption, this measure promotes both the reliability and the electromagnetic compatibility of the system.

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