Applications of the COS/MOS CD4059A Programmable Divide-by-N Counter: Digital Frequency Synthesis for FM Tuners and CB Transceivers

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This Note describes an FM digital tuner and a citizens band (CB) transceiver digital tuner that were constructed and tested to demonstrate the frequency synthesis capability of the Harris COS/MOS CD4059A programmable divide-by-N counter. The mechanical technique normally used in frequency synthesis consists of varying a capacitor, thus changing the frequency of the local oscillator and, in turn, tuning the receiver to any desired frequency. The digital approach described in this Note allows the desired frequencies to be selected by depressing numbered buttons on a keyboard. By using the appropriate basic circuitry along with a phase-locked-loop, PLL, circuit, the local oscillator of the receiver is adjusted and locked to the proper frequency, thus assuring proper station selection. Alternate methods of station selection that demonstrate the flexibility of the system are also described.

FEATURES OF THE CD4059A

The functional diagram of the CD4059A is shown in Fig. 1. The CD4059A is a divide-by-N down counter that can be programmed to divide an input frequency by any integer N from 3 to 15,999, Fig.2. The output signal is a pulse one-clock-pulse wide that occurs at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down counter is preset by means of 16 jam inputs. The mode of the input decade and the counter length are externally selectable by means of the mode-select inputs. The three mode select inputs Ka, Kb, and Kc determine the modulus (divide-by number) of the first and last counting sections in accordance with the

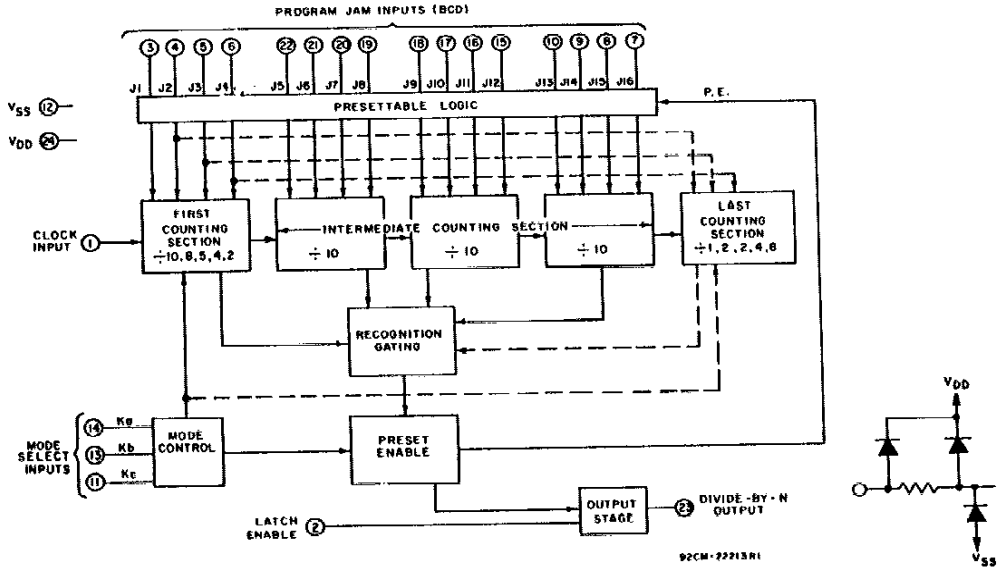

Fig. 1 – Functional block diagram of CD4059A.

The value N is determined as follows:

$$N = |MODE^*| \quad |1000 \times \text{Decade 5 Preset} + 100X \text{ Decade 4 Preset} + 10X \text{ Decade 3 Preset} + 1X \text{ Decade 2 Preset}| + \text{Decade 1 Preset} \tag{1}$$

* MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \tag{2}$$

Examples:

A) N = 8479, Mode = 5

1695 + 4 ← Preset Values

5 | 8479

Mode, N

MODE SELECT = 5

PROGRAM JAM INPUTS (BCD)

				4			1	5				9				6			
Ka	Kb	Kc		J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	1		0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0

To verify the results use equation 1 :

N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4

N = 8479

B) N = 12382, Mode = 8

1547 + 6

8 | 12382

MODE SELECT = 8

PROGRAM JAM INPUTS

				6			1	7				4				5			
Ka	Kb	Kc		J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	0	1		0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0

To verify:

N = 8 (1000 X 1 + 100 X 5 + 10 X 4 + 1 X 7) + 6

N = 12382

C) N = 8479, Mode = 10

0847 + 9

10 | 8479

MODE SELECT = 10

PROGRAM JAM INPUTS

				9				7				4				8			
Ka	Kb	Kc		J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	1	0		1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

N = 10 (1000 X 0 + 100 X 8 + 10 X 4 + 1 X 7) + 9

N = 8479

Fig.2 — How to preset the CD4059A to a desired N.

truth table shown in Table 1. Every time the first (fastest) counting section goes through one cycle it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the divide-by-2 mode only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If divide-by-10 is desired for the first section, set Ka = 1, Kb = 1, and Kc = 0; jam inputs J1, J2, J3, and J4 are used to preset the first counting section; there is no last counting section.

Table I – Truth Table for the CD4059A

MODE	MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			DESIGN COUNTER RANGE		EXTENDED COUNTER RANGE
First counting section divides by:	Ka	Kb	Kc	Divides by:	Can be preset to a maximum of:	Jam inputs used:	Divides by:	Can be preset to a maximum of:	Jam inputs used:	Min.	Max.	Max.
2	1	1	1	2	1	J1	8	7	J2,J3,J4	3	15,999	17,331
4	0	1	1	4	3	J1,J2	4	3	J3,J4	3	15,999	18,663
5	1	0	1	5	4	J1,J2,J3	2	1	J4	3	9,999	13,329
8	0	0	1	8	7	J1,J2,J3	2	1	J4	3	15,999	21,327
10	1	1	0	10	9	J1,J2,J3,J4	1	0	–	3	9,999	16,659
Master Preset (MP)	X	0	0	MP			MP			–	–	–

X = Don't Care

The intermediate counting section consists of three cascaded BCD decade (divide-by-10) counters presettable by means of jam inputs J5 through J16.

The mode select inputs permit frequency synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. In addition, these inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, 100, multiplied by the number of the divide-by-N mode. For example, in the divide-by-8 mode, the number from which counting down begins can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
Last counting section	1000
	2665 x 8 = 21,320

The first counting section can be preset to 7

Therefore, 21,327

is the maximum possible count in the divide-by-8 mode. The highest count of the various modes is shown in the column entitled Extended Counter Range, Max., of Table I.

Control inputs Kb and Kc can be used to initiate and lock the counter in the master preset state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs, and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected. Whenever the master preset mode is used, control signals Kb = 0 and Kc = 0 must be applied for at least 3 full clock pulses. A 1 on the latch input will cause the counter output to remain high until the latch input returns to 0. If the latch input is 0 the output pulse will remain high for only 1 cycle of the clock-input signal.

After the master preset mode inputs have been changed to one of the divide-by-modes, the next positive-going clock transition changes an internal flip-flop so that the countdown begins at the second positive-going clock transition. Thus, after an MP mode, there is always one extra count before the output goes high. See Fig. 3 for total count of 3 (divide-by-8 mode).

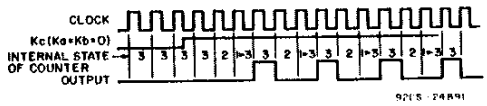

Fig.3 – CD4059A waveforms.

As illustrated in the sample applications, this device is very useful in communication digital frequency synthesis (VHF, UHF, FM, AM, etc.) where programmable divide-by-N counters are an integral part of the synthesizer phase-locked-loop subsystem. Note that the CD4059A can also be used to perform the synthesizer fixed divide-by-R counting function.

DIGITAL FM TUNER

The digital control for an FM/FM stereo tuner shown in block diagram form in Fig. 4 was designed using the CD4059A and other COS/MOS standard parts. A detailed system logic/block diagram of the circuit is shown in Fig. 5. The system is composed of eight major subsystems:

1. Keyboard for Station Selection
2. Up/Down Counter and Memory
3. Keyboard Load Control
4. Station Scan Control
5. Prescaler (÷K)
6. Programmable Divide-by-N Counter and 10.7 MHz Offset
7. Phase Comparator (÷R) and Reference Oscillator
8. Liquid-Crystal-Display Driver

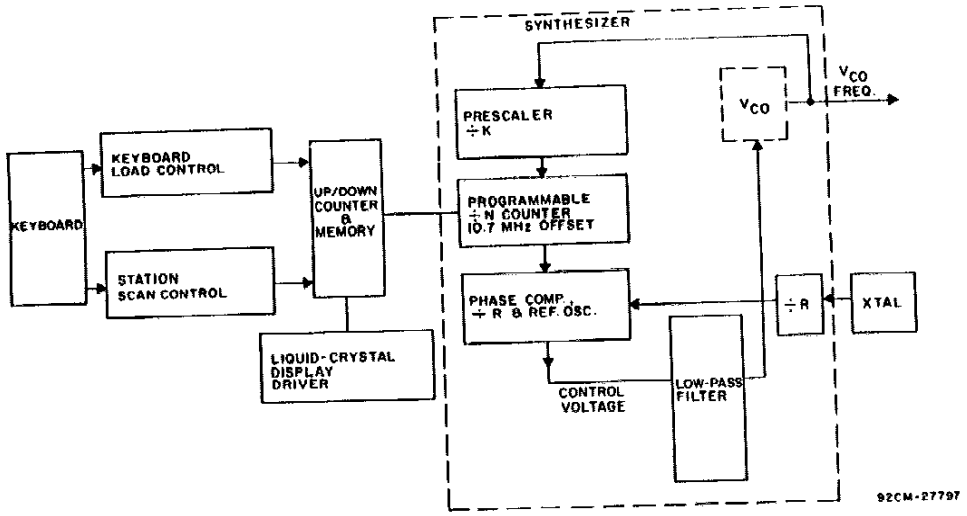

Fig.4 – Block diagram of the FM/FM stereo tuner.

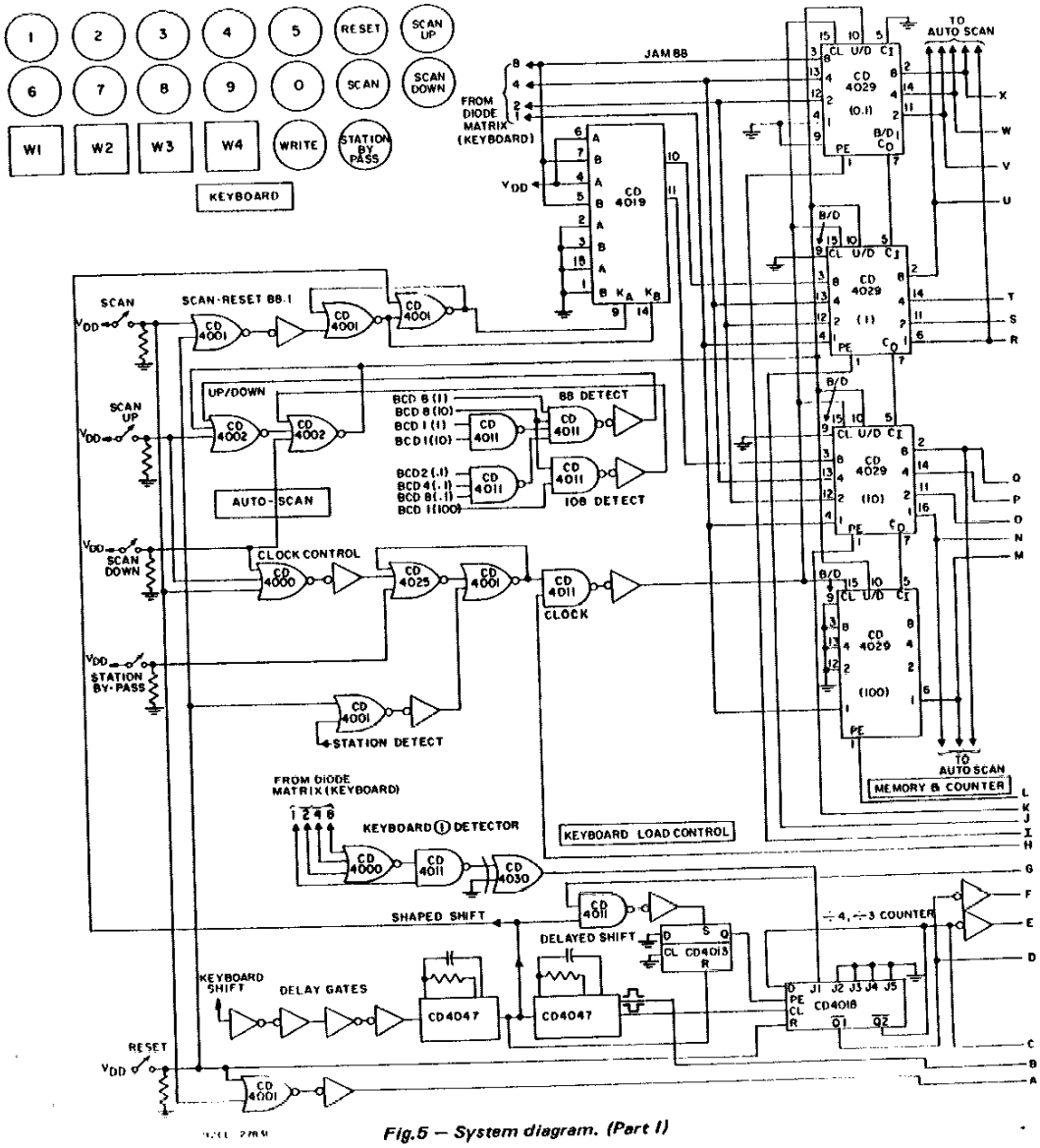

Fig.5 – System diagram. (Part I)

Keyboard and Station Selection

The keyboard consists of 16 pushbutton SPST switches and 4 SPDT toggle switches. The 0 through 9 switches are wired to form a diode matrix that generates a four-line BCD equivalent of the key number depressed. At the same time a high level is generated on a separate line called the keyboard shift line (this line is explained below). The remaining keyboard switches are discussed below along with the functions they control.

Station Selection Techniques

A number of tuning options are available. The system is placed in the first channel location, 88.1 MHz, by depressing the Reset button. This action enables all four up/down counters simultaneously, and the number 88, through the A inputs of the Jam 88 CD4019A, feeds through the system to set the tuner on 88.1 MHz. The display also shows 88.1 at this time. The following options can then be initiated:

Direct Station Selection – Direct station selection is accomplished by means of the keyboard pushbuttons 0-9 (most significant frequency digit first). The channel frequency number will appear on the display and the tuner VCO will lock on that channel.

Scan – When the SCAN button is depressed, the tuner is set to the lowest FM channel (88.1) through the same logic as that in effect when the Reset button is pushed. In addition, the scan input also feeds the auto-scan logic circuits, and the tuner begins to step forward through the

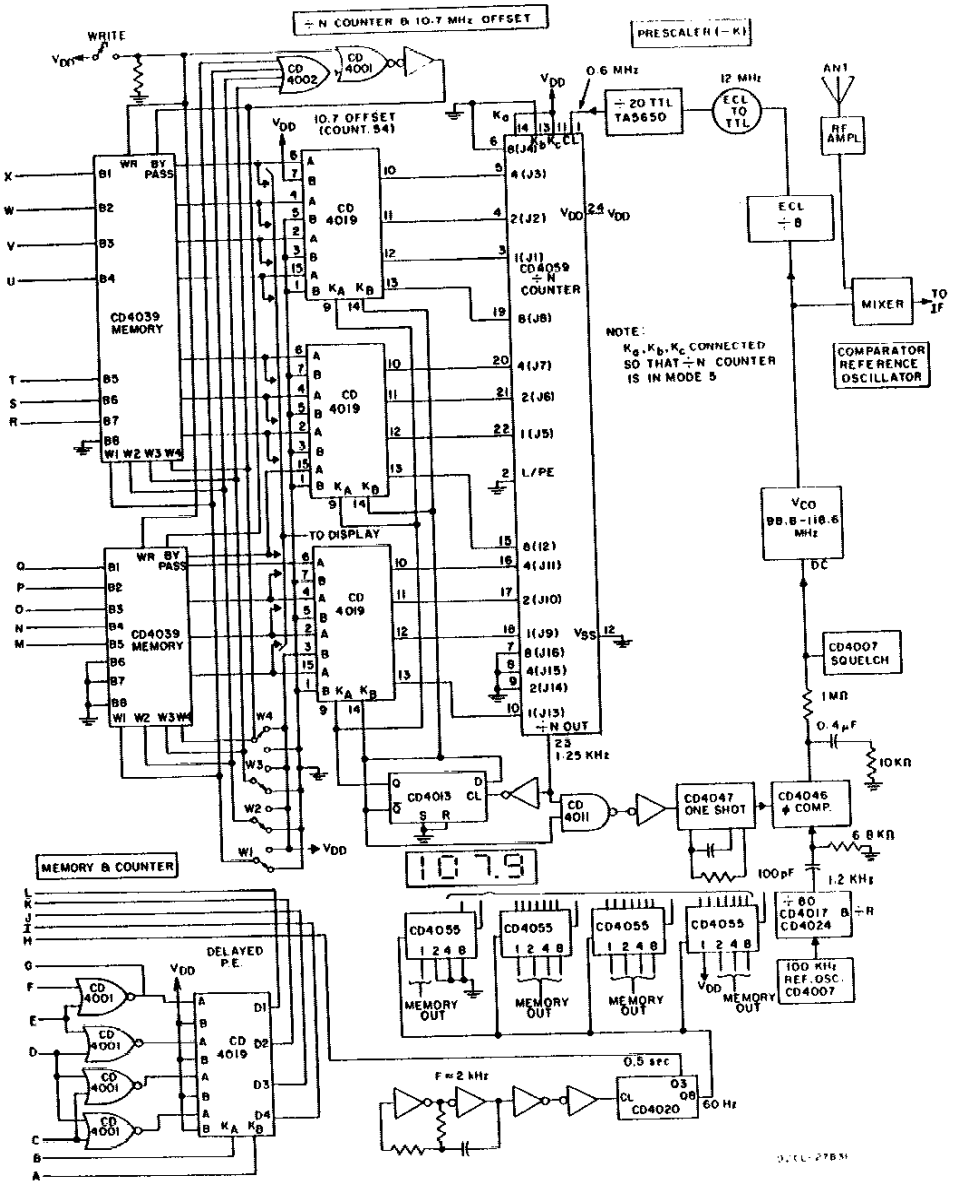

Fig.5 – System diagram. (Part II)

channels until a station is located. At this time a station detect signal is received in the clock-control logic circuits, the scanning ceases, and the frequency of the channel is shown on the liquid-crystal display. To resume scanning, the station-bypass button on the keyboard is depressed. Depressing the Scan-Up button also causes resumption of the scanning operation. The stepping action proceeds in the forward direction until another station is located. When the upper limit of the FM band is reached (107.9) the direction of tuning is reversed and stepping down the band begins. The Scan-Up or Scan-Down buttons override any scanning in process and redirect the tuner to step in the direction indicated.

It may be desirable to design a system without the Scan, Reset, and Station-Bypass buttons; they are included here mainly to demonstrate system flexibility.

Memory Storage – Any channel located during the scan operation or selected by means of the keyboard can be stored in the memory. The four SPDT switches on the keyboard allow four channels to be stored for future pushbutton selection. (This limit of 4 channels is imposed by the size of the memories used in the system.) To store the address of the channel frequency in the memory, a W button is placed in the closed position and the Write pushbutton is then depressed. The Write button disables the memory bypass and enables the station frequency number to be stored in the memory. Any stored number can be erased from the memory by simply entering a new number in the word selected in the memory.

Circuit Operation

Up/Down Counter and Memory – Four CD4029A presettable up/down counters are used to accomplish two functions: First, storage for the selected keyboard numbers (the selected frequency), and second, up or down counting whenever the system is in the scanning mode. The tuner is initialized by depressing the Reset button.

When the first key is depressed, following initialization, a BCD number appears on the jam lines of all four CD4029A counters simultaneously. At the same time the shift signal from the keyboard is processed by the keyboard load control circuit and appears as a preset-enable signal on one of the up/down counters, thus allowing the BCD number to be loaded into that counter. Each time a key is depressed, a different counter is loaded; thus, four CD4029A counters are loaded sequentially.

The CD4039A is a COS/MOS four-word by eight-bit random-access NDRO memory. The CD4039A units in the FM tuner are tied to the CD4029A counter outputs, and are sensitive to the data stored in the counters. Any word-select line of the memory unit that is set high will allow the counter data to be stored in memory when the Write switch is closed. (The word-select switches W1 through W4 and the Write switch are located on the keyboard.) This sequence of events permits any station frequency to be stored in memory at any time, regardless of the mode of operation. During normal operation, in the direct station selection or scan modes of operation, the outputs of the up/down counters are bypassed around the memory units.

Because of the low power dissipation of COS/MOS parts, a stand-by battery incorporated in the system is sufficient to ensure that information in memory will not be destroyed should a power failure occur.

Keyboard Load Logic – The keyboard load logic ensures sequential loading of the counters. Some FM channels are represented by a three digit number (for example, 88.1), others by a four digit number (for example, 107.9); therefore, counters are loaded with either a three or a four-digit number.

A CD4018A counter, with associated decoding gates, addresses the keyboard digits to the proper CD4029A counter in the proper sequence. For example, if a 1 is detected as the first keyboard digit, the CD4018A operates as a divide-by-4 counter and the output from the CD4019A that is connected to the most significant-valued up/down counter enables the preset-enable input of that counter (marked 100). The 1 on the input lines of the 3 most significant up/down counters presets only the most significant counter (100) and thereby stores the first keyboard digit. If the first keyboard digit is any number other than 1, the CD4018A operates as a divide-by-3 counter, and the first output of the CD4019A gates to be energized is the one connected to the CD4029A marked (10). Thus the second keyboard digit selected is stored in the CD4029A marked (10). The other digits are directed to their respective up/down counter in sequence; timing that controls the sequencing is derived from two CD4047A monostable multivibrators. The CD4013A is used in the set-reset mode to determine the first digit and to preset the CD4018A counter.

The CD4019A AND/OR select gate prevents the enabling of any of the four counters while the lines are unstable; i.e., during the time just after a digit has been loaded. Keyboard-switch "bounce" is prevented by use of a CD4047A one-shot circuit and some gate delays. Elimination of bounce eliminates false triggering of the divide-by-four counter.

The Station selection with power on is random; therefore the system should be reset each time power is turned on.

Station Scan Control – When the scan button is depressed, a high-level voltage appears at the K_B input to the delayed

P. E. package CD4019A. The V_{DD} on the B inputs to this package is fed through and enables the P.E. input on the four up/down counters. This high-level voltage allows 88.1 to be jammed into the up/down counters (0.1, 1, 10). The Jam 88 CD4019A controlled by the Scan-Reset 88.1 logic feeds the 88.1 number to the up/down counters. The Scan circuit energizes the Clock-Control circuit and clock pulses are fed into the up/down counters to increase the count toward 107.9. When the tuner locates a station, the station detect signal into the clock control circuit stops the clock and the counters stop counting. The source of the station-detect signal will depend on fabrication of the complete tuner, which is not covered in this Note. If no stations are received in the scan-up period, the counters start counting down automatically after the maximum count (107.9) is reached. The scanning up and down continues indefinitely until a station is received. To start the count again, (if the station received is not desired) the Scan-Up (or Scan-Down) button is depressed. If the Reset button is depressed, it affects the up/down counter in the same manner as the Scan button did previously; the up/down counter starts counting again from 88.1. The Reset button also resets the divide-by-9 counter CD4018A in the keyboard load control subsystem.

Prescaler (divide-by-K) — The CD4059A programmable divide-by-N counter accepts its signal directly from the VCO. Any VCO with a control voltage of 3 to 17 volts will function in the system. Since the upper operating frequency of the CD4059A at a V_{DD} of 5 volts is approximately 1 MHz, a fixed divide-by-K prescaler of 160 was chosen. An ECL divide-by-eight unit feeding into an ECL-to-TTL converter, which in turn feeds a TTL divide-by-20 unit, provides the required operating input frequency for the counter (0.6 MHz).

Programmable Divide-by-N Counter and 10.7 MHz Offset — After prescaling, any of the 100 FM channels selected will appear as a clock input to the CD4059A counter. The clock frequencies representing these channels range between 0.6175 MHz and 0.74125 MHz. Fig. 6 shows the block diagram of the phase-lock-loop. Without a prescaler, the reference frequency (fr) is nominally equal to the channel-spacing frequency (fc). However, where a prescaling counter is employed, the value of fr must be reduced by a division by K.

Referring to Fig. 6:

$$f_o = KNf_n$$

$$\text{and } f_r = f_x/R \quad .$$

When the loop is phase-locked:

$$f_n = f_r$$

and thus:

$$f_o = \frac{K}{R} N f_x \quad .$$

In this design:

$$K = 160$$

$$R = 80$$

$$f_x = .1 \text{ MHz}$$

and $N = 5\,(\# + 10.7)$

where # = FM channel frequency in MHz; i.e., $88.1 \leqslant \# \leqslant 107.9$, and 10.7 is the offset of the local oscillator above the channel to be tuned.

Thus:

$$f_r = \frac{.1}{80} \text{ MHz} = 1.25 \text{ kHz}$$

and

$$f_o = \frac{160}{80} 5\,(\# + 10.7)\ (.1) \text{ MHz}$$

$$= (\# + 10.7) \text{ MHz} \quad .$$

In operation:

$$98.8 \leqslant f_o \leqslant 118.6 \text{ MHz}$$

$$617.5 \leqslant f_k \leqslant 741.25 \text{ kHz}$$

and

$$494 \leqslant N \leqslant 593.$$

In the FM band, the channel spacings are $f_c = 200 \text{ kHz} = 160\,(1.25) \text{ kHz} = Kf_r$.

When N is 494 and the VCO frequency is 98.8 MHz, the CD4059A counter output, fn, is 1.25 kHz. The 98.8 MHz VCO frequency is the frequency desired when the system is tuned to the lowest FM channel.

The CD4059A counter, after prescaling, is clocked by the VCO frequency, which is 10.7 MHz (if frequency = 10.7 MHz) higher than the FM channel frequency (88.1 + 10.7 = 98.8). Therefore, the 10.7 MHz offset number must be added to the keyboard number to raise it to the VCO number. Thus, the keyboard number of 88.1 (which yields an N of 440) will appear as 98.8, which corresponds to an N of 494 at the jam input lines. The offset of 10.7 MHz is equivalent to an offset of N of

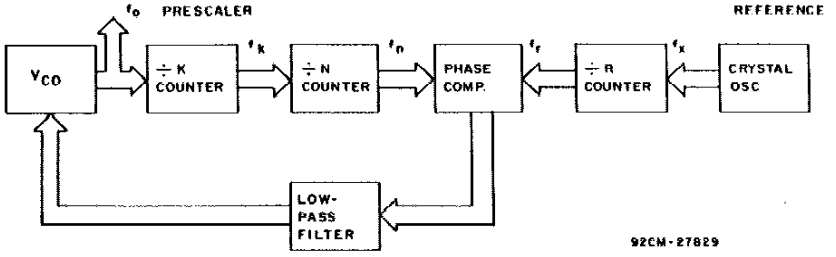

Fig.6 — Block diagram of synthesizer (PLL) subsystem.

Table II — Tuner Data

STATION FREQ.	JAM INPUT	N (÷ 5 Mode)	FIXED OFFSET	TOTAL ÷ N
88.1	088 + 0	440	+54	= 494
88.3	088 + 1	441	+54	= 495
88.5	088 + 2	442	+54	= 496
88.7	088 + 3	443	+54	= 497
88.9	088 + 4	444	+54	= 498
89.1	089 + 0	445	+54	= 499
89.3	089 + 1	446	+54	= 500
89.5	089 + 2	447	+54	= 501
89.7	089 + 3	448	+54	= 502
89.9	089 + 4	449	+54	= 503
90.1	090 + 0	450	+54	= 504
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
107.9	107 + 4	539	+54	= 593

54. Table II shows the tuner keyboard (station) frequencies, divide-by-N input jam numbers, and total divide-by-N numbers (including offset).

The offset is accomplished by using the three CD4019A AND-OR-select gates, the CD4013A flip-flop and the CD4011A NAND gate. The function of the CD4019's is to transform the single set of divide-by-N jam inputs into two sets of inputs, each independently connected to the counter. The actual keyboard number is on one set of inputs (the "A" inputs); the fixed offset number, 54, is on the other set of inputs (the "B" inputs). Initially, the keyboard number is connected to the divide-by-N counter jam line, and the counter counts down from the input jam number. Table II shows that 88.1 MHz is equivalent to N = 440. The following example shows how the up/down counters and the divide-by-N counter establishes this equivalency.

An 88.1 input from the keyboard through the top three up/down counters results in a jam input to the divide-by-N counter of 88 + 0. The + 0 results from the fixed ground on the 1 input of the top CD4029A. Because the divide-by-N counter is in the divide-by-5 mode, the 88 + 0 jam input is 88 x 5 or 440. A signal that appears at the counter output at the completion of the count clocks the flip flop and causes it to change state. This change is used to switch the jam inputs to a condition that results in an N of 54, and once again the counter counts down. The inputs that result in an N of 54 are fed into the divide-by-N counter when the K_B is energized. The V_{DD} on the top CD4019A puts a 1 on the J3 input of CD4059A. The ground on the other B inputs puts zeros on the J2 and J1 inputs. The result is a 4 for the "plus portion" of the N number.

The V_{DD} on the B input of the bottom CD4019A puts a 1 on the J9 input to the CD4059A and the ground on the other B inputs puts zeros on the J10,J11, and J12 inputs. The result is a 1 from the divide-by-10 decade and, because the divide-by-N counter is in the divide-by-5 mode, the total number from the divide-by-10 decade is 1 x 10 x 5 or 50. The total offset number is 50 plus 4 (from J1, J2, J3 decade) or offset N = 54. The second output of the counter is allowed to appear at the "true" input. The result is two countdowns totalling the 494 required. *Note that this system provides total compatibility between keyboard and jam numbers.*

Because the least significant digit of valid FM channels is always odd, the BCD 1 input of the top CD4029A is hardwired to ground, and the 8, 4, 2 outputs from this counter are logically connected to the BCD 4, 2, 1 inputs, respectively, of the first section of the divide-by-N counter (J3, J2, J1). This modification makes the least significant digits of the keyboard numbers appear in the "plus portion" of the divide-by-N counter as follows: a BCD 1 (the 1 in 88.1 for example) results in a 0, a BCD 3 in a 1, a BCD 5 in a 2 etc. (see Table II). Therefore, as each successive station number appears, one count is added to the N number of the divide-by-N counter.

Phase Comparator and Reference Oscillator — A CD4046A phase-comparator circuit is used in the phase-lock-loop system. A phase difference between the divide-by-N counter output and the reference frequency produces a correction voltage at the output of the phase comparator. The polarity of this correction voltage is such that it pulls the VCO frequency in a direction that causes the divide-by-N output frequency to phase-track the reference frequency.

The CD4046A phase comparator is used in this application because it does not lock in harmonics of the signal-input reference

frequency. In addition, the duty cycle of the output of the divide-by-N counter is not 50 percent (a pulse output), hence phase comparator II, which is an edge-controlled digital memory network, is feasible for this system. Inputs to the comparator consist of the divide-by-N output and a reference signal derived from a 100-kHz crystal-controller oscillator that employs a CD4007A inverter unit. A reference frequency of 1.25 kHz is obtained by using a CD4017A decade counter and a CD4024A divide-by-eight counter. The reference signal pulse is also shaped by means of an RC coupled circuit.

Liquid-Crystal-Display Driver — A four-digit, seven-segment, numeric liquid-crystal display cell is used to display the selected FM channel. Four CD4055A liquid-crystal BCD-to-7-segment decoder drivers are used to drive the cell. BCD data is taken from the memory input lines and used as the input for the liquid-crystal drivers. Hence, the number displayed always represents the station selected, regardless of mode of operation.

The low-frequency (60-Hz) signal required to drive the liquid-crystal cell is generated from a CD4007A RC oscillator, which drives a CD4020A counter. A counter output is used as a clock signal for the CD4029A up/down counter when the system is operating in the scan mode. The scan rate can be varied by selecting the desired output counter stage.

CB TRANSCEIVER WITH PHASE-LOCK-LOOP DIGITAL TUNING

The basic requirement of a CB transceiver is to receive any one of 23 channels in the 27.420 to 27.710 MHz frequency range with a very high degree of accuracy, because of the very narrow bandwidth involved (10 kHz), and to transmit on any one of these same channels with crystal accuracy. These requirements normally call for designs incorporating a large number of crystals, (as many as 25, one for each channel plus 2 for local oscillators) and cumbersome switching techniques. The system described below employs frequency-synthesis techniques to fulfill all of the above requirements with one crystal and digital tuning.

Circuit Operation

Fig. 7 contains a block diagram of the 27-MHz CB synthesizer. The RF oscillator, Fig. 8, operating as the V_{CO}, is designed to cover all transmit frequencies in the citizens band along with all frequencies required of the local oscillator in the receive mode. The exact frequency of oscillation is determined by the dc voltage at the V_{CO}. The generation of this dc voltage is described below.

The output of the V_{CO} is fed to a prescaler that reduces the 27 MHz by a factor of 50 by means of an MC1013 ECL divide-by-two counter, an MC5490 divide-by-five counter, and a CD4018A presettable counter

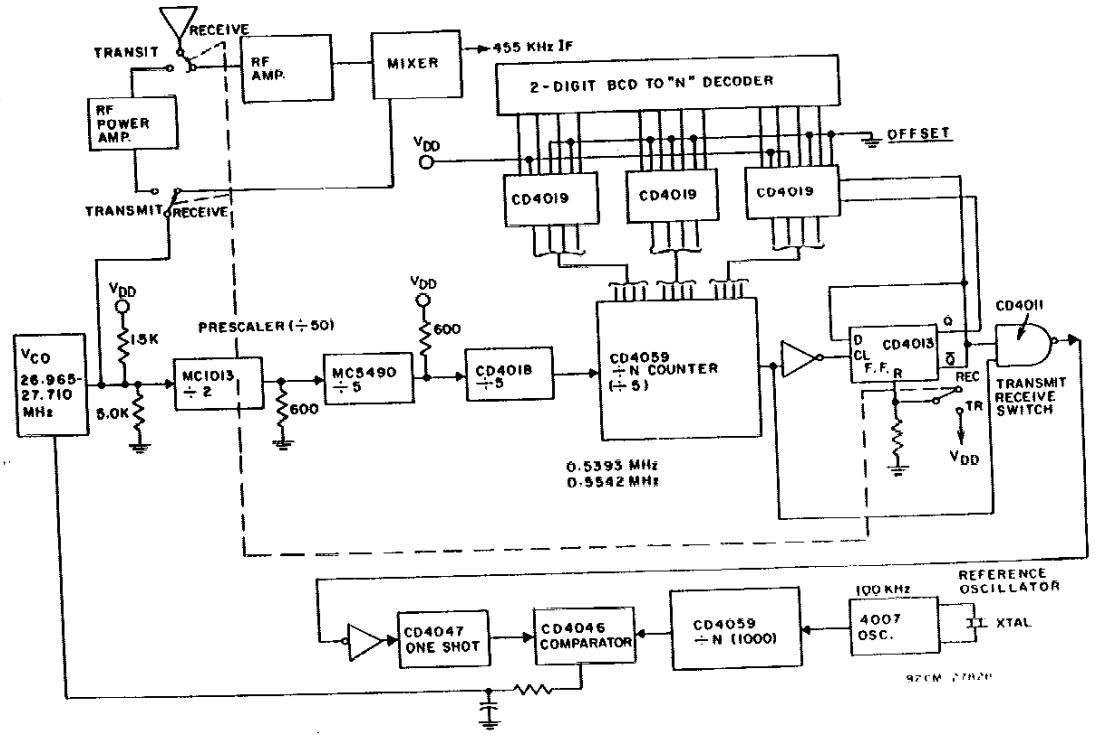

Fig.7 – 27-MHz CB synthesizer.

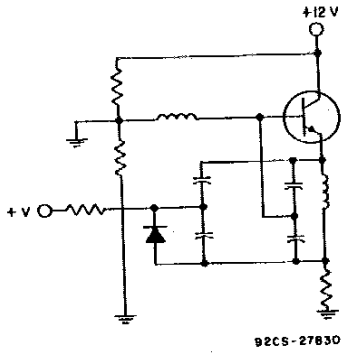

Fig.8 – 27-MHz VCO.

in a divide-by-five mode. The output of the prescaler supplies the clock input to the CD4059A divide-by-N counter. The CB channels now appear as a frequency range of 0.5393 to 0.5542 MHz; the prescaler has brought the V_{CO} frequency range to within the operating-frequency range of the CD4059A.

The reference frequency, f_r, is normally equal to the channel spacing, f_c. However, when prescaling is employed, the value of f_r must be reduced by a division by the prescaling factor. Hence, since the channel spacing is 10 kHz and the prescaling factor is 50, the reference frequency, f_r, should be:

$$f_r = \frac{10\,\text{kHz}}{50} = 200\,\text{Hz}$$

However, since the CB frequencies involved are not divisible by 10, double spacing is employed, which, in effect, reduces channel spacing to 5 kHz. The reference frequency then becomes:

$$f_r = \frac{5\,\text{kHz}}{50} = 100\,\text{Hz}$$

This requires only that the N of the divide-by-N counter change two digits rather than one for system compatibility.

To accommodate a channel spacing of 5 kHz, the counter operates in a divide-by-five mode, Table III. A divide-by-two mode can also be used, Table IV. At phase lock, the divide-by-N output (f_n) tracks the reference frequency, f_r, so that $f_n = f_r$. Furthermore, the modulus of the divide-by-N counter, N, uniquely determines the output frequency, f_o, that will satisfy the equation:

$$f_o = f_n\,KN$$

where f_o ranges between 26,965 MHz and 27.710 MHz. Therefore, the range of N is

Table III – CB Band Transmit and Receive Frequencies with Required Divide-by-N Mode = 5

Chan	Transmit Freq.(MHz)	÷N Req'd for Transmit Freq.	JAM # in CD4059A in ÷5 Mode	Receiver L.O. Freq(MHz)	÷N Req'd For Receive	JAM # in CD4059A in ÷5 Mode With Offset
1	26.965	5393	1078 + 3	27.420	5484	1096 + 4
2	26.975	5395	1079	27.430	5486	1097 + 1
3	26.985	5397	1079 + 2	27.440	5488	1097 + 3
4	27.005	5401	1080 + 1	27.460	5492	1098 + 2
5	27.015	5403	1080 + 3	27.470	5494	1098 + 4
6	27.025	5405	1081	27.480	5496	1099 + 1
7	27.035	5407	1081 + 2	27.490	5498	1099 + 3
8	27.055	5411	1082 + 1	27.510	5502	1100 + 2
9	27.065	5413	1082 + 3	27.520	5504	1100 + 4
10	27.075	5415	1083	27.530	5506	1101 + 1
11	27.085	5417	1083 + 2	27.540	5508	1101 + 3
12	27.105	5421	1084 + 1	27.560	5512	1102 + 2
13	27.115	5423	1084 + 3	27.570	5514	1102 + 4
14	27.125	5425	1085	27.580	5516	1103 + 1
15	27.135	5427	1085 + 2	27.590	5518	1103 + 3
16	27.155	5431	1086 + 1	27.610	5522	1104 + 2
17	27.165	5433	1086 + 3	27.620	5524	1104 + 4
18	27.175	5435	1087	27.630	5526	1105 + 1
19	27.185	5437	1087 + 2	27.640	5528	1105 + 3
20	27.205	5441	1088 + 1	27.660	5532	1106 + 2
21	27.215	5443	1088 + 3	27.670	5534	1106 + 4
22	27.225	5445	1089	27.680	5536	1107 + 1
23	27.255	5451	1090 + 1	27.710	5542	1108 + 2

Table IV – CB Band Transmit and Receive Frequencies with Required Divide-by-N Mode = 2

Chan	Transmit Freq.(MHz)	÷N Req'd for Transmit Freq.	JAM # in CD4059A in ÷2 Mode	Receiver L.O. Freq.(MHz)	÷N Req'd For Receive	JAM # in CD4059A in ÷2 Mode With Offset
1	26.965	5393	2696 + 1	27.420	5484	2742
2	26.975	5395	2697 + 1	27.430	5486	2743
3	26.985	5397	2698 + 1	27.440	5488	2744
4	27.005	5401	2700 + 1	27.460	5492	2746
5	27.015	5403	2701 + 1	27.470	5494	2747
6	27.025	5405	2702 + 1	27.480	5496	2748
7	27.035	5407	2703 + 1	27.490	5498	2749
8	27.035	5411	2705 + 1	27.510	5502	2751
9	27.065	5413	2706 + 1	27.520	5504	2752
10	27.075	5415	2707 + 1	27.530	5506	2753
11	27.085	5417	2708 + 1	27.540	5508	2754
12	27.105	5421	2710 + 1	27.560	5512	2756
13	27.115	5423	2710 + 1	27.570	5514	2757
14	27.125	5425	2712 + 1	27.580	5516	2758
15	27.135	5427	2713 + 1	27.590	5518	2759
16	27.155	5431	2715 + 1	27.610	5522	2761
17	27.165	5433	2716 + 1	27.620	5524	2762
18	27.175	5435	2717 + 1	27.630	5526	2763
19	27.185	5437	2718 + 1	27.640	5528	2764
20	27.205	5441	2720 + 1	27.660	5532	2766
21	27.215	5443	2721 + 1	27.670	5534	2767
22	27.225	5445	2722 + 1	27.680	5536	2768
23	27.255	5451	2725 + 1	27.710	5542	2771

given by:

$$N = \frac{f_O}{f_C}$$

$$N\ max = \frac{f_O\ max}{f_C} = \frac{27{,}710\ MHz}{5\ kHz} = 5542$$

$$N\ min = \frac{f_O\ min}{f_C} = \frac{26{,}965\ MHz}{5\ kHz} = 5393$$

When N is 5393 and the counter output frequency is 100 Hz, the VCO frequency is 26.965 MHz. This is the frequency that corresponds to channel 1.

Tables III and IV indicate that the proper local-oscillator frequency for channel 1 is 27.420 MHz. This frequency beats with the incoming VCO frequency, 26.965 MHz, to generate a 455-kHz frequency. The if frequency is represented by an N equal to 5484 ($N = \frac{f_O}{f_C}$), a number exactly 91 units higher than the N required for the transmit frequency (N = 5393). The offset number, 91, is added to the N (5393) of the counter in the receive mode for channel 1.

The offset number is added to the N of the counter by using CD4019A-AND-OR-select gates, a CD4013A flip flop, and a CD4011A NAND gate. The function of the CD4019A is to transform the single set of divide-by-N jam inputs to two sets of inputs, both connected independently to the counter. One set of inputs carries the actual N number required for the transmission frequency of the channel desired, the other set of inputs carries the fixed offset number, 91. Initially, the set of inputs carrying the transmission-frequency N is connected to the divide-by-N counter jam lines, and the counter counts down from that number. A signal that appears at the counter output is used, in turn, to switch the jam inputs to the fixed count of 91, and once again the counter counts down. The second output of the counter is the true output. Thus, there have been two countdowns totaling 5484 (5393 + 91), and either the transmit or the receive local oscillator frequency is available. The

offset can be employed or not depending on whether the flip flop (CD4013A) is held in reset or not. The flip-flop reset switch switches from the transmit to the receive frequency.

The output of the phase comparator II of the CD4046A is used in the phase-lock-loop circuit. A phase difference between the divide-by-N counter and the difference frequency produces a correction voltage at the output of the phase comparator. The polarity of this correction voltage pulls the VCO frequency in a direction that causes the divide-by-N output frequency to phase-track the reference frequency. Inputs to the comparator consist of the divide-by-N output and a reference derived from the 100-kHz crystal-controlled oscillator. The oscillator is built from a CD4007A dual complementary pair plus inverter; a reference of 100 Hz is obtained by using a CD4059A with an N of 1000. The output of the comparator is fed through an RC filter to the VCO.