Simplified Design of Astable RC Oscillators Using the CD4060B or Two CMOS Inverters

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Application Notes are available that deal with theoretical approaches to oscillator design; this Note stresses practical aspects of design and provides easy-to-use algebraic equations that permit values of R and C for a given oscillator frequency to be quickly determined.

Astable Design Approach

The most basic RC oscillator circuit is that shown in Fig. 1. The time period T for one cycle of this oscillator is given by the equation:[1]

$$T = -RC\left[\ln\frac{V_{DD}-V_{TR}}{V_{DD}} + \ln\frac{V_{TR}}{V_{DD}}\right] \quad (1)$$

where:

V_{DD} = supply voltage
V_{TR} = transfer voltage

By letting $V_{TR} = 0.5\ V_{DD}$, equation 1 can be simplified to:

$$T = -RC\,(\ln 0.5 + \ln 0.5)$$
$$T = 1.39\,RC \quad (2)$$

The problem with this circuit is that transfer voltage can vary from 33 to 67 percent of V_{DD}. Therefore, the maximum variation in the time period, T, can be as high as 9 percent, with a ±33 percent variation in transfer voltage from unit to unit.

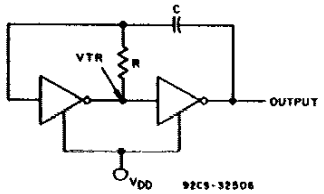

Fig. 1 · The most basic RC oscillator circuit.

An improvement to this basic circuit can be made by adding resistor R_S, as shown in Fig. 2. The resistor makes the frequency independent of supply-voltage variations and reduces the time-period variations to less than 5 percent with variations in transfer voltage.

Rs should be 10 times the value of Rx. If Rs is made less than 10 Rx, the variation in period T increases to about 10 percent as the value of Rs approaches zero.[1] If Rs is made too large, a time constant and phase shift is produced by Rs and stray wiring and breadboard capacitance. This shift creates a switching delay in the circuit which changes the time period.

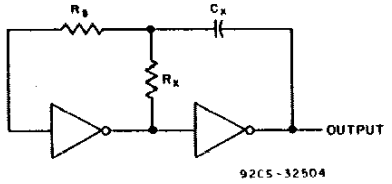

Fig. 2 · An improved oscillator circuit made by adding resistor R_S to the circuit of Fig. 1.

The time period T for the circuit in Fig. 2 is:[1]

$$T = -R_xC_x\left[\ln\frac{V_{TR}}{V_{DD}+V_{TR}} + \ln\frac{V_{DD}-V_{TR}}{2\,V_{DD}-V_{TR}}\right] \quad (3)$$

If $V_{TR} = 0.5\ V_{DD}$, equation 3 can be simplified to:

$$T = -R_xC_x\,(\ln \tfrac{1}{3} + \ln \tfrac{1}{2})$$
$$T = 2.2\,R_xC_x \quad (4)$$

Equation 4 will only be true in the CD4060B for values of R greater than 50 kilohms and for values of C greater than 1000 picofarads. At values of C less than 1000 picofarads, stray capacitance will have a much greater effect on the entire system.

It is advised that a buffer circuit, Fig. 3, be added to the circuit of Fig. 2 to prevent the jitter that would otherwise be introduced into the circuit by noise picked up by connecting cables and by stray wiring and breadboard capacitance. The buffer circuit is not needed with the CD4060B since it has an internal buffer and is internally connected to a counter.

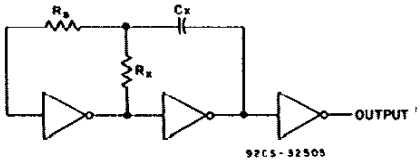

Fig. 3 · A buffer circuit used to improve the performance of the circuit of Fig. 2.

Compensation for 50-Percent Duty Cycle

A true square-wave pulse is obtained only when the transfer voltage occurs at the 50-percent point. If the transfer voltage is at either 33 or 67 percent, the duty cycle will not be 50 percent. The duty cycle can be controlled, however, if part of the resistance of the RC time constant is shunted out with a diode, as shown in Fig. 4.

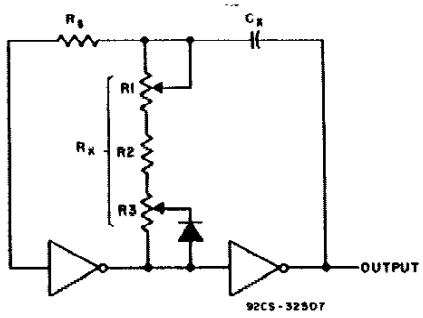

Fig. 4 · Method of controlling the duty cycle of the RC oscillator.

Because adjustment of this diode shunt to obtain a specific pulse factor causes the frequency of the circuit to stray, a frequency control, R1, is added. This circuit is not needed when using the CD4060B since it is used in conjunction with a counter. A 50-percent duty cycle will be derived from the divider/counter outputs.

References and Bibliography

1. "Astable and Monostable Oscillators Using Harris COS/MOS Digital Integrated Circuits", Harris Application Note AN6466.
2. "COS/MOS 14-Stage Ripple Carry Binary Counter/Divider and Oscillator", Harris Data Sheet File Number 1120.