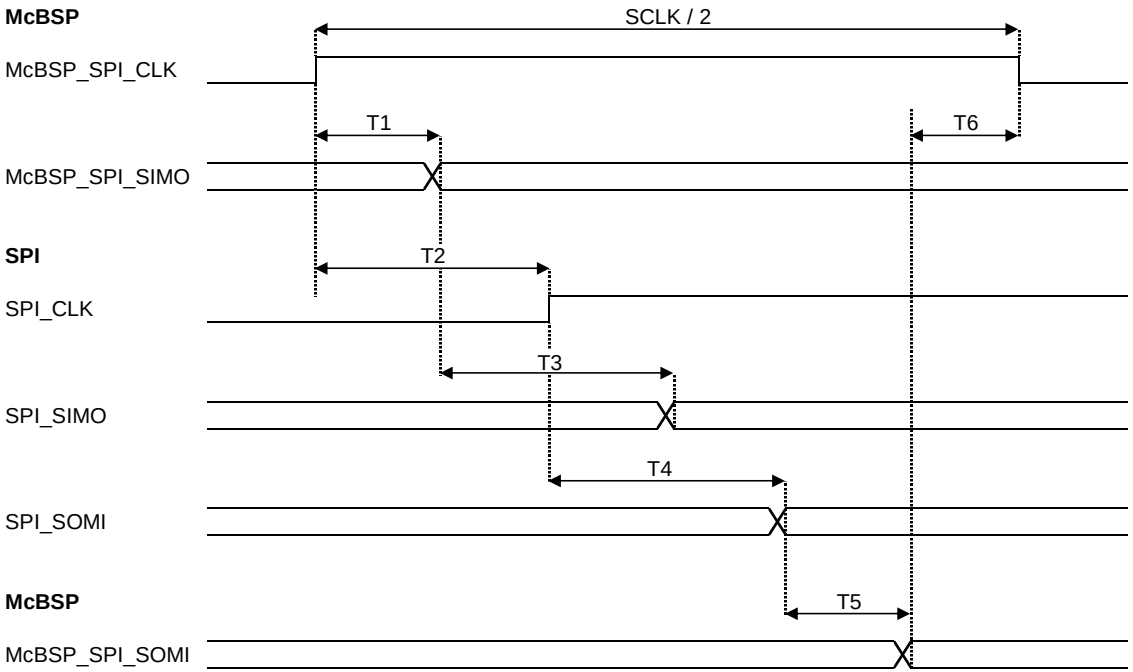
**McBSP is master**




| Timing Parameter | Description | Delay (ns) |
|---|---|---|
| T1 | Clock to valid data out for McBSP master operation. Parameter M55 in fig 6-48 | Unresolved |
| T2 | PCB delay for McBSP clock out to SPI clock in. Series R=1k, trace capacitance + DSP input capacitance=25pF. | 25 |
| T3 | PCB delay for McBSP data out to SPI data in. Series R + Cin as per parameter T2 | 25 |
| T4 | Clock to valid data out for SPI slave operation. Timing parameter 15 in table 6-26 of SPRS 1740 | (0.375 * SCLK) - 10 |
| T5 | PCB delay for SPI data out to McBSP data in. Series R + Cin as per parameter T2 | 25 |
| T6 | Data setup time before clock edge. Timing parameter M58 in Table 6-55 of SPRS1740 | 30 |

To determine max freq of the spi clock, SCLK:
0.5 * SCLK = T2 + T4 + T5 + T6
0.5 * SCLK = 25 + (0.375 * SCLK) - 10 + 25 + 30
SCLK = 560ns (1.78MHz)