| | | | | | | |
|---|---|---|---|---|---|---|
| INT13 | 13 | 0x00000D1A | 2 | ~~External Interrupt 13 (XINT13) or~~ CPU-Timer1 (3) | 17 | - |
| INT14 | 14 | 0x00000D1C | 2 | CPU-Timer2 (for TI/RTOS use) | 18 | - |
| DATALOG | 15 | 0x00000D1E | 2 | CPU Data Logging Interrupt | 19 (lowest) | - |
| RTOSINT | 16 | 0x0000 0D20 | 2 | CPU Real-Time OS Interrupt | 4 | -- |
| EMUINT | 17 | 0x0000 0D22 | 2 | CPU Emulation Interrupt | 2 | - |
| NMI | 18 | 0x0000 0D24 | 2 | External Non-Maskable Interrupt | 3 | - |
| ILLEGAL | 19 | 0x0000 0D26 | 2 | Illegal Operation | -- | - |
| USER1 | 20 | 0x0000 0D28 | 2 | User-Defined Trap | -- | - |
| USER2 | 21 | 0x0000 0D2A | 2 | User Defined Trap | -- | - |
| USER3 | 22 | 0x0000 0D2C | 2 | User Defined Trap | -- | - |
| USER4 | 23 | 0x0000 0D2E | 2 | User Defined Trap | -- | -- |
| USER5 | 24 | 0x0000 0D30 | 2 | User Defined Trap | -- | - |
| USER6 | 25 | 0x0000 0D32 | 2 | User Defined Trap | -- | - |
| USER7 | 26 | 0x0000 0D34 | 2 | User Defined Trap | -- | - |
| USER8 | 27 | 0x0000 0D36 | 2 | User Defined Trap | -- | - |
| USER9 | 28 | 0x0000 0D38 | 2 | User Defined Trap | -- | - |
| USER10 | 29 | 0x0000 0D3A | 2 | User Defined Trap | -- | - |

(1) Reset is always fetched from location 0x003F FFC0 in Boot ROM.
(2) All the locations within the PIE vector table are EALLOW protected.
(3) ~~CPU-Timer1 is reserved for TI software use. The interrupt XINT13, however, can be freely used by customer applications.~~

**Figure 1-15. CPU-Timer Interrupts Signals and Output Signal**