# 24V – 15V DC-DC Converter ESD Problem and proposed solutions

## General description of the problem.

The power supply inputs 24V DC from a higher powered switch-mode power supply. The 24V DC is galvanically isolated from ground, i.e. floating w.r.t. ground.

The printed circuit board is mounted in a plastic enclosure.

Below the printed circuit board is a large metallic mass (heatsink casting) which is grounded.

ESD contact discharge onto the heatsink @ 2.2kV triggers a shutdown of the 15V power supply. The reset time looks the same as that which would occur if an over-current is detected, the SS capacitor is slowly discharged until it reaches the reset level. Shorting pins 7 and 8 does not make any difference! This suggests that the noise is coupled into the chip by some other means when the high dv/dt appears on the heatsink.

## Some design details

### Schematic



TR27 is used to change the overcurrent detection level.

### PCB Layout

The PCB is a 4 layer with 1 oz copper. All components are mounted on one side (layer 1).

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Layer 1

+24V supply track passes under TPS40200 (IC21)

Layer 2: 0V fill only

Layer 3

IC21

Turquoise track is the +15V output of the 24V – 15V power supply controlled by IC21

Brown track is the -15V output of a different power supply which inputs +15V and outputs -15V.

Purple is +24V supply. Fill is used because +24V feeds several power supplies and low impedance is required.

+24V supply goes off board here through a connector to a daughter board. If the PCB which this connector feeds is disconnected, the ESD threshold increases from 2.2kV to 4.4kV.

Layer 4

+5V supply track passes under TPS40200 (IC21)

+Green is 0V fill

## Improvements already made

The design has been changed twice already:

1. In response to the initial test failure @ 2.2kV we added a ferrite choke in series with the +24V power track feeding the daughter board, in the location of the arrow from the top callout of the Layer 3 picture above (L3 on the silk screen). This allowed a pass of the ESD test @ 6.6kV, the target level for the ESD test. We made this change because we found that if the daughter board was disconnected, the ESD threshold increased from 2.2kV to 4.4kV.

This indicates that the problem is related to noise coupled into the +24V track by the circuits on the daughter board. The +24V track in the current layout ‘circles’ the TPS40200 (IC21) – see Layer 3 picture above.
2. With change # 1 in place we repeated the ESD test with the PCB mounted on a smaller heatsink. The pass level reduced to 4.3kV.

We can raise this pass level to 6.3kV by adding 1uF filter capacitors from each side of the ferrite, L3, to 0V and changing L3 to a type with much higher impedance in the GHz ranges.

## Further Improvements that we are considering

Because we have a minimum ESD pass level of 6.6kV and we cannot reach this level (currently 6.3kV), and we would really like to reach the 8.3kV pass level of the other product using the same circuit on a different printed circuit board, we are proposing all the following changes:

1. On layer 1 we will move the +24V track from under IC1 and fill the area under IC1 with 0V fill.
2. We will make provision for a filter resistor (10R?) to be connected between +24V and the TPS40200 VDD pin (pin 8). Also, the decoupling capacitor connected between pin 8 and pin 5 and the RC timing network connected to pin 1 will be fed from the ‘filtered’ +24V of the decoupling capacitor.
3. We will move the filter capacitor C47 between pins 7 and 8 to be adjacent to these pins.
4. We will modify the layer 3 fill areas to expand the +24V fill so that it is underneath IC21. The +15V and -15V fill areas will be taken onto layer 4 at a point to the left of IC21 and routed away from IC21:

This change is based upon a theory that in the current layout the dv/dt of the heatsink is coupling common mode noise into the +24V and 0V rails on the PCB, but the TPS40200 has different levels of common mode coupling from these fill areas on the PCB, because the +24V fill circles IC21 but the 0V fill is an almost complete solid plane (layer 2).

The comparator which compares VDD – 100mV with the signal on pin 7 (ISNS) might produce an output pulse and trip the latch if the +24V rail has a different noise level to the 0V rail.

If the +24V fill is expanded as shown, the coupling will be more balanced from the +24V and 0V fill areas into IC21.

If the above theory is incorrect, and the noise is coupling into IC21 by noise currents flowing in the +24V fill which ‘circles’ IC21 (i.e. magnetically), then by increasing the +24V fill area as shown the magnetic coupling will be reduced.

In addition, we have another product which uses this power supply design on a different printed circuit board. This has been ESD tested mounted on the same heatsink and it can reach 8.3kV before the power supply shuts down. The layout of this PCB has +24V fill underneath the TPS40200.

Expand the +24V fill to include this area.

A glitch here will trip the latch and shut down the power supply.

1. We will move the +5V track passing under IC21 on layer 4 away from IC21 as a precaution.