EV220x Evaluation Board
PIC Interface Commands

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EV2200 EVALUATION BOARD

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INTRODUCTION

This document covers the command instructions and sequences required to interface and IBM compatible PC with the Texas Instruments EV2200.

The EV2200 currently supports the following Texas Instruments devices.

bq2013H	bq2050H
bq2014H	bq2052
bq2018	bq2060
bq2019	bq2092
bq2040	bq2945

PIC 16C66 RS-232 INTERFACE

Commands and data are passed between the EV2200 board and the PC are RS-232 signals with the following protocol:

* 9600 baud (default) or 19200
* 8 data bits
* no handshaking
* no parity
* 1 stop bit

Upon reset the EV board will be set to 9600 baud. Any unrecognized byte will cause a switch to the next available baud rate.

Bytes are oriented with the least significant bit (LSB) leading the data stream.

Commands consist of five bytes and ***MUST*** **be five bytes in length**, byte 1 being the sync byte (0xAA), byte 2 being the command byte, and bytes 3-5 used for miscellaneous address, sub-command, data, or echo information.

COMMAND BLOCK SUMMARY

Command	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Echo Block	0xAA	8	echo 1 byte	echo 2 byte	echo 3 byte
Request Version	0xAA	10	-	-	-
Read A to D Converter (4)	0xAA	11	Channel #	-	-
Request Board Status	0xAA	80	-	-	-
Read SMBus Word	0xAA	20	sub-cmd*	-	-
Read SMBus Word with 1ms timer	0xAA	21	sub-cmd*	-	-
Read SMBus Word w/PEC	0xAA	22	sub-cmd*	-	-
Read SMBus Word with 1ms timer and PEC	0xAA	23	sub-cmd*	-	-
Read last SMBus PEC	0xAA	2F	-	-	-
Write SMBus Word	0xAA	60	sub-cmd*	LS data	MS data
Write SMBus Word w/PEC	0xAA	61	sub-cmd*	LS data	MS data
Write SMBus Word w/ BAD PEC (3)	0xAA	62	sub-cmd*	LS data	MS data
Read SMBus Block	0xAA	30	sub-cmd*	-	-
Read SMBus Block with 1ms timer	0xAA	31	sub-cmd*	-	-
Read SMBus Block w/PEC	0xAA	32	sub-cmd*	-	-
Read SMBus Block with 1ms timer and PEC	0xAA	33	sub-cmd*	-	-
Write I^2C Byte	0xAA	40	address	Data	-
Read I^2C Byte	0xAA	0	address	-	-
EEPROM on/off	0xAA	41	on=1, off=0	-	-
Change Slave	0xAA	42	New SMBus slave address hex	-	-
Read HDQ8-1	0xAA	50	Command code	-	-
Write HDQ8-1	0xAA	51	Command code	Data	
Break HDQ8-1	0xAA	52	-	-	-
Read HDQ8-2	0xAA	53	Command code	-	-
Write HDQ8-2	0xAA	54	Command code	Data	-
Break HDQ8-2	0xAA	55	-	-	-
Break HDQ16-1	0xAA	58	-	-	-
Read HDQ16-1	0xAA	59	Command code	-	-
Write HDQ16-1	0xAA	5A	Command code	Data	Data
Break HDQ16-2	0xAA	5B	-	-	-
Read HDQ16-2	0xAA	5C	Command code	-	-
Write HDQ16-2	0xAA	5D	Command code	Data	Data
Read DQ-1	0xAA	A0	Command code	-	-
Write DQ-1	0xAA	A1	Command code	Data	-
Break DQ-1	0xAA	A2	-	-	-
Read DQ-2	0xAA	A3	Command code	-	-
Write DQ-2	0xAA	A4	Command code	Data	-
Break DQ-2	0xAA	A5	-	-	-

Notes:
1. All Values are in HEX
2. * See table 7, pg. 18, bq 204x/9x specification (code column) for information on bq204x/9x access codes.
3. Transmits an inverted good PEC value.
4. Used in factory version only

Table 1. Command Block Summary

RESPONSE BLOCK SUMMARY

Command	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Echo Block	0xAA	8	NOT (echo 1 byte)	NOT (echo 2 byte)	NOT (echo 3 byte)
Request Version	0xAA	10	LS version	MS version	-
Read A to D Converter	0xAA	11	Channel # shifted Left	LS byte	MS byte
Request Board Status	0xAA	80	LS status	MS status	-
Read SMBus Word	0xAA	20	sub-cmd*	LS byte	MS byte
Read SMBus Word with 1 ms timer	0xAA	**21	sub-cmd*	MS byte	MS byte
Read SMBus Word w/PEC	0xAA	22	sub-cmd*	LS byte	MS byte
Read SMBus Word with 1 ms timer w/PEC	0xAA	**23	sub-cmd*	MS byte	MS byte
Read Last PEC following Read	0xAA	2F	PEC Calculated	PEC Transmitted	Final Result
Read Last PEC following Write	0xAA	2F	-	-	PEC Transmitted
Write SMBus Word	0xAA	60	LS status	MS status	-
Write SMBus Word w/PEC	0xAA	61	LS status	MS status	-
Read SMBus Block	0xAA	30	sub-cmd*	number of bytes	16 ASCII bytes
Read SMBus Block with 1 ms timer	0xAA	**31	sub-cmd	Number of bytes	16 ASCII bytes
Read SMBus Block w/PEC	0xAA	32	sub-cmd*	number of bytes	16 ASCII bytes
Read SMBus Block with 1 ms timer w/PEC	0xAA	**33	sub-cmd	Number of bytes	16 ASCII bytes
Write I2C Byte	0xAA	40	LS status	MS status	-
Read I2C Byte	0xAA	0	Address	data	-
EEPROM on/off	0xAA	41	on=1, off=0	-	-
Change Slave	0xAA	42	New SMBus slave address hex	-	-
Read HDQ1	0xAA	50	Command code	Data	-
Write HDQ1	0xAA	51	Command code	Data	0
Break HDQ1	0xAA	52	-	-	-
Read HDQ2	0xAA	53	Command code	Data	-
Write HDQ2	0xAA	54	Command code	Data	0
Break HDQ2	0xAA	55	-	-	-
Break HDQ16	0xAA	58	-	-	-
Read HDQ16	0xAA	59	Command code	LS Data	MS Data
Write HDQ16	0xAA	5A	Command code	LS Data	MS Data
Break HDQ16 com 1	0xAA	5B	-	-	-
Read HDQ16 com 1	0xAA	5C	Command code	LS Data	MS Data
Write HDQ16 com 1	0xAA	5D	Command code	LS Data	MS Data
Read DQ 1	0xAA	A0	Command code	Data	-
Write DQ 1	0xAA	A1	Command code	Data	-
Break DQ 1	0xAA	A2	-	-	-
Read DQ 2	0xAA	A3	Command code	Data	-
Write DQ 2	0xAA	A4	Command code	Data	-
Break DQ 2	0xAA	A5	-	-	-

Notes:

1. ** Commands 21, 23, 31 and 33 add a 2 byte timer that increments every 1 ms. Command 21 and 23 are 7 bytes long and commands 31 and 33 are 22 bytes long. The timer is sampled immediately upon receiving the command and then sent at the end of the response with the LSB sent first and MSB second
2. Byte 2 always reflects the command byte
3. Read SMBus Block command returns a 20 byte block regardless of the size of “number of bytes”
4. Echo response bytes 1-3 are the ones compliment of the Echo command bytes 1-3.
5. An error on any Command Block will return the “Request Board Status” response.
6. The SMBus is monitored for a valid idle bus before any transmission is attempted.
7. Maximum scan rate is 5-7 microseconds.

Table 2. Response Byte Summary

STATUS BYTES DEFINITION

Only one of the error conditions in the Status LS Byte can be valid at any one time. For example, it is not possible to have a bad RS232 sync bit and a SMBus error indicated during the same received status byte. All errors are cleared after every successful RS232 command.

Status bits are high for the given condition to be present.

LS Byte Definition

	Bit							
State	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Set Condition	-	-	-	-	HDQ Error	SMBus Error	I^2C Error	RS-232 sync byte Error

Figure 1. Status LS Byte Definition

MS Byte Definition

	Bit							
State	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Set Condition	-	-	-	-	-	-	-	-

Figure 2. Status MS Byte Definition

Data in the MS status byte is only valid if a SMBus or I^2C error is indicated by the LS byte. This status byte provides additional information concerning only SMBus and I^2C errors. The following values will be returned by the MS byte depending on the error conditions:

SMBus
1. SMBC locked low by device (bus is still busy) or clock stretch timeout
2. SMBD locked low by device (bus is still busy)
3. No acknowledge from device (no handshake)
4. SMBD not released for master to generate STOP bit
5. Bus locked before trying to transmit

I^2C
1. I^2C bus locked low
2. I^2C EEPROM no acknowledge

RS-232
1. RS-232 sync byte error

SMBUS PROTOCOLS

Write Word

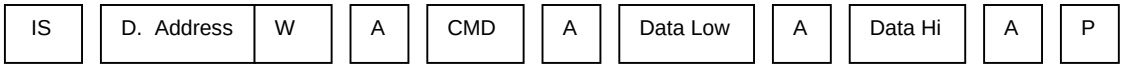

Figure 3. SMBus Write Word Protocol

Read Word

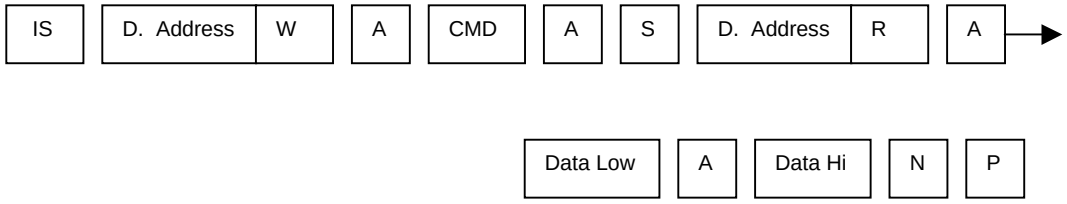

Figure 4. SMBus Read Word Protocol

Where:

IS	Idle Monitor with Start Bit
S	Start Bit
W	Write Bit
R	Read Control Bit
A	Acknowledge Expected from Slave
N	No Acknowledge

EV2201 EVALUATION BOARD

Contents

Introduction

This document covers the command instructions and sequences required to interface and IBM compatible PC with the Texas Instruments EV2201.

The EV2201 currently supports the following Texas Instruments devices.

bq2023

PIC 16C66 RS-232 INTERFACE

Commands and data are passed between the EV2201 board and the PC are RS-232 signals with the following protocol:

* 9600 baud (default) or 19200
* 8 data bits
* no handshaking
* no parity
* 1 stop bit

Upon reset the EV board will be set to 9600 baud. Any unrecognized byte will cause a switch to the next available baud rate.

Bytes are oriented with the least significant bit (LSB) leading the data stream.

KEY:

= Manual communication command bytes

= Manual communication response bytes

NA = Not supported at this time

NOTE 1: The following responses are valid:
0x00 presence pulse not found
0x01 presence pulse found

NOTE 2: The value indicates the number of bytes to the end of the command, past this byte:
0x03 3 bytes
0x08 8 bytes

NOTE 3: The following subcommands are valid:
0x00 Read with page CRC - The communication will include sending the command code for the operation and the two bytes of the start address (LB, HB). The response will have the CRC of the command and address.
0x01 Read with field CRC -The communication will include sending the command code for the operation and the two bytes of the start address (LB, HB) . The response will have the CRC of the command and address.

The selection used for the ‘Read Data’ command must also be used for the ‘Read Next Address command’

NOTE 4: When the CRC is reported, these two bytes return garbage data, which should be ignored.

COMMAND AND RESPONSE DATA

Command	Sync Byte	Cmd Byte	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7	Data 8	Data 9	Data 10
Reset	0xAA	0x90	0x00	0x00	0x00							
	0xAA	0x90	Note(1)	0x00	0x00							
Profile CMD	0xAA	0x91	0x00	0x00	0x00							
	0xAA	0x91	0x00	Code	0x00							
Read ID	0xAA	0x92	0x00	0x00	0x00							
	0xAA	0x92	0x00	Note(2)	LSB ID	7SB ID	6SB ID	5SB ID	4SB ID	3SB ID	2SB ID	MSB ID
Match ID	0xAA	0x93	0x00	Note(2)	LSB ID	7SB ID	6SB ID	5SB ID	4SB ID	3SB ID	2SB ID	MSB ID
	0xAA	0x93	0x00	0x00	0x00							
(NA) Search ID	0xAA	0x94										
(NA)	0xAA	0x94										
Skip ID	0xAA	0x95	0x00	0x00	0x00							
	0xAA	0x95	0x00	0x00	0x00							
Write Memory	0xAA	0x96	LSB Addr	MSB Addr	Data							
	0xAA	0x96	0x00	CRC	0x00							
Read Data	0xAA	0x97	Note(3)	LSB Addr	MSB Addr							
	0xAA	0x97	0x00	CRC	Data							
Erase FLASH Page	0xAA	0x98		LSB Page Code	MSB Page Code							
	0xAA	0x98	0x00	CRC	0x00							
(NA) Write Memory Block	0xAA	0x9A										
(NA)	0xAA	0x9A										
Read Memory Block	0xAA	0x9B	Note(3)	Note(2)	LSB Addr	MSB Addr	# Bytes to Read					
	0xAA	0x9B	Note(3)	Num of Bytes to Follow	CRC	1st Byte of Data	2nd Byte of Data	… Bytes of data to N-1 …				Nth Byte of Data
Program Code (0x5A)	0xAA	0x9C	0x00	0x00	0x00							
	0xAA	0x9C	0x00	Data Written	0x00							
Read Next Address	0xAA	0x9D	0x00	0x00	0x00							
	0xAA	0x9D	Data or CRC	LSB Addr Note(4)	MSB Addr Note(4)							
Write Next Flash Address	0xAA	0x9E	0x00	Data	0x00							
	0xAA	0x9E	0x00	CRC	0x00							
Write Next RAM Address	0xAA	0x9F	0x00	Data	0x00							
	0xAA	0x9F	0x00	CRC	Data							