bq20z70 and bq20z90

Application Book

Literature Number: SLUA404
December 2006

Texas Instruments

Contents

Impedance Track™ Gas Gauge for Novices – bq20z70/z90

PMP Portable Power

ABSTRACT

This document introduces the bq20z70/z90 Impedance Track™ and bq29330 chipset gas gauge solution.

1.1 Introduction

This application report provides an introductory overview of the following bq20z70/z90 Impedance Track™ gas gauge topics:

- The Basics
  - bq20z70/z90 Impedance Track™ gas gauge overview
  - Impedance Track™ technology operation principle
  - Gas gauge hardware
    - bq29330 analog front-end protector
    - How the bq20z70/z90 and bq29330 operate together
    - bq2941x 2nd-Level overvoltage protector
  - bq20z70/z90EVM-001 evaluation module
  - bqEVSW software for use with bq20z70/z90
- Next Steps
  - Developing a PCB for bq20z70/z90/bq29330/bq2941x chipset
  - Solution development process
  - Mass production setup
- Glossary
- Reference design schematic

1.2 The Basics

bq20z70/z90 Impedance Track™ Gas Gauge Overview

1.2.1.1 Key Features:

- Patented Impedance Track™ technology accurately measures available charge in Li-ion and Li-polymer batteries.
- Better than 1% capacity estimate error over the lifetime of the battery
- Instant capacity estimate accuracy – no learning cycle required
- Automatically adjust for battery aging, battery self-discharge and temperature inefficiencies
- Supports the Smart Battery Specification SBS V1.1
- Works with the TI bq29330 analog front-end (AFE) protection IC to provide a complete pack electronics solution
- Full array of programmable voltage, current, and temperature protection features
- Integrated time base removes need for external crystal (bq20z90 also comes with optional crystal input)
- Supporting 2-, 3-, and 4-cell battery packs with few external components
- Based on a powerful low-power RISC CPU core with high-performance peripherals
- Integrated, field-programmable flash memory eliminates the need for external configuration memory
- Measures charge flow using a high-resolution, 16-bit integrating delta-sigma converter
- Uses 16-bit delta-sigma converter for accurate voltage and temperature measurements
- Extensive data reporting options for improved system interaction
- Optional pulse charging feature for improved charge times
- Drives 3-, 4-, or 5-segment LED display for remaining capacity indication (bq20z90 only)
- Optional cell-balancing feature for increased battery life
- Supports SHA-1 authentication
- Lifetime data logging
- bq20z70: 20-pin TSSOP (DBT) package
  bq20z90: 30-pin TSSOP (DBT) package

The bq20z70 and bq20zz90 are advanced, SBS v1.1-compliant, feature-rich battery gas gauge ICs, designed for accurate reporting of available charge of Li-ion or Li-polymer batteries. The bq20z70/z90 incorporates the patented Impedance Track™ technology, whose unique algorithm allows for real-time tracking of battery capacity change, battery impedance, voltage, current, temperature, and other critical information of the battery pack. Unlike the *current integration*- or *voltage-correlation*-based gas gauge algorithms, the Impedance Track™ algorithm takes full advantage of battery response to electronic and thermal stimuli and therefore maintains the best capacity estimate accuracy over the lifetime of the battery. The bq20z70/z90 automatically accounts for charge and discharge rate, self-discharge, and cell aging, resulting in excellent gas-gauging accuracy even when the battery ages. The IC also provides a variety of battery performance parameters to a system host over a standard serial communication bus (SMBus).

The difference between bq20z70 and bq20z90 lies in their target applications. The bq20z90 offers highest performance available to date with support of five LED display channels. The bq20z70, with largely the same feature set as those in bq20z90 but no LEDs, reduces overall system implementation cost for the growing *low-cos*t notebook battery packs.

The heart of the bq20z70/z90 programmable battery management IC is a high-performance, low-power, reduced instruction-set (RISC) CPU, which offers powerful information-processing capability that is crucial to battery management functional calculation and decision-making. The IC also integrates plenty of program and data flash memory and an array of peripheral and communication ports, facilitating rapid development of custom implementations and eliminating the need for external configuration memory.

The bq20z70/z90 is equipped with two high-resolution, analog-to-digital converters (ADC) dedicated for accurate coulomb counting and voltage/temperature measurements. These low-power analog peripherals improve accuracy beyond discrete implementations. The bq20z70/z90 is designed to work with the bq29330 analog front-end (AFE) protection IC to provide a complete pack electronics solution. Figure 1 shows a simplified system diagram of a typical multicell gas-gauging solution consisting of the bq20z70/z90 and the bq29330. The main task of the AFE bq29330 is to provide safety protection of overcharge, overload, and short-circuit of the battery. The AFE can be configured to autonomously shut off the field-effect transistor (FET) drives at overload or short-circuit conditions. In addition, the AFE serves as a voltage translator for the bq20z70/z90 gas gauge IC, providing individual cell or battery voltages to the gas gauge IC. In case of overvoltage and undervoltage conditions as detected by the gas gauge IC, the AFE performs actions such as turning on/off charge/discharge FETs as instructed or programmed by the gas gauge IC.

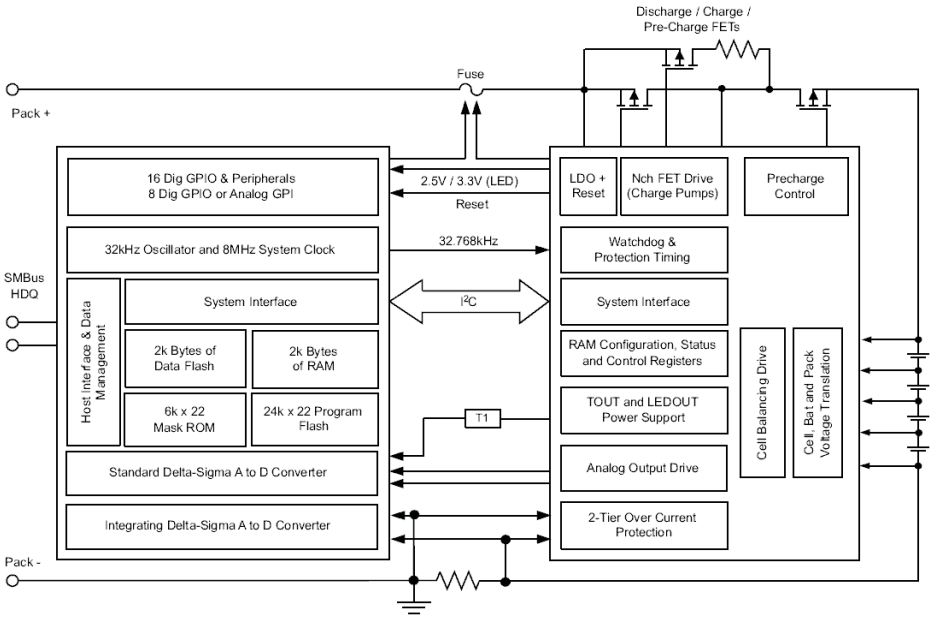


Figure 1. Battery Management Unit Block Diagram

The bq20z70/z90 measures individual cell and pack voltages, temperature, current, and integrated passed charge using the analog interface of the bq29330 AFE and the two delta-sigma ADCs of the bq20z70/z90.

Impedance Track™ Technology Operation Principle

What makes the Impedance Track™ technology unique and much more accurate than existing solutions is a self-learning mechanism that accounts for the change of (1) battery impedance and (2) the no-load chemical full capacity (Qmax) due to battery aging. A fact that is often ignored is that battery impedance increases when the battery ages. As an example, typical Li-ion batteries double the impedance after approximately 100 cycles of discharge. Furthermore, battery impedance also varies significantly between cells and at different usage conditions, such as temperature and state-of-charge. Therefore, to achieve sufficient accuracy, a large, multidimension impedance matrix must be maintained in the IC flash memory, making the implementation difficult. Acquiring such a database is also time-consuming. The Impedance Track™ technology significantly simplifies gas-gauging implementation by continuously updating the battery impedance during the usage lifetime of the battery, and thus only needs a simple, initial impedance database. Temperature and load effects are automatically accounted for when calculating the full-charge capacity (FCC) and the remaining capacity (RM). On the other hand, the Qmax is also calculated and updated during the usage of the battery — only in more strict conditions as mentioned later in this section.

The full-fledged monitoring mechanisms of the bq20z70/z90 allow for accurate measurement of the following key properties:

- OCV: Open-circuit voltage of a battery, usually assuming the battery is already in relaxation mode

- Battery impedance: $\frac{OCV - BatteryVoltageUnder\ Load}{AverageLoad\ Current}$
- PassedCharge: Coulomb counter integrated charge during battery charge or discharge
- SOC: State-of-charge at any moment, defined as SOC=Q/Qmax, where Q is the PassedCharge from the full-charge state
- DOD: Depth of discharge; DOD= 1-SOC
- DOD_0: Last DOD reading before charge or discharge
- DODcharge: DOD for a fully charged pack
- Qstart: Charge that would have passed to make DOD = DOD_0
- Qmax: Maximum battery chemical capacity
- RM: Remaining capacity
- FCC: Full-charge capacity, the amount of charge passed from the fully charged state to the Terminate Voltage

Figure 2 illustrates charge, discharge, and relaxation modes of the battery.

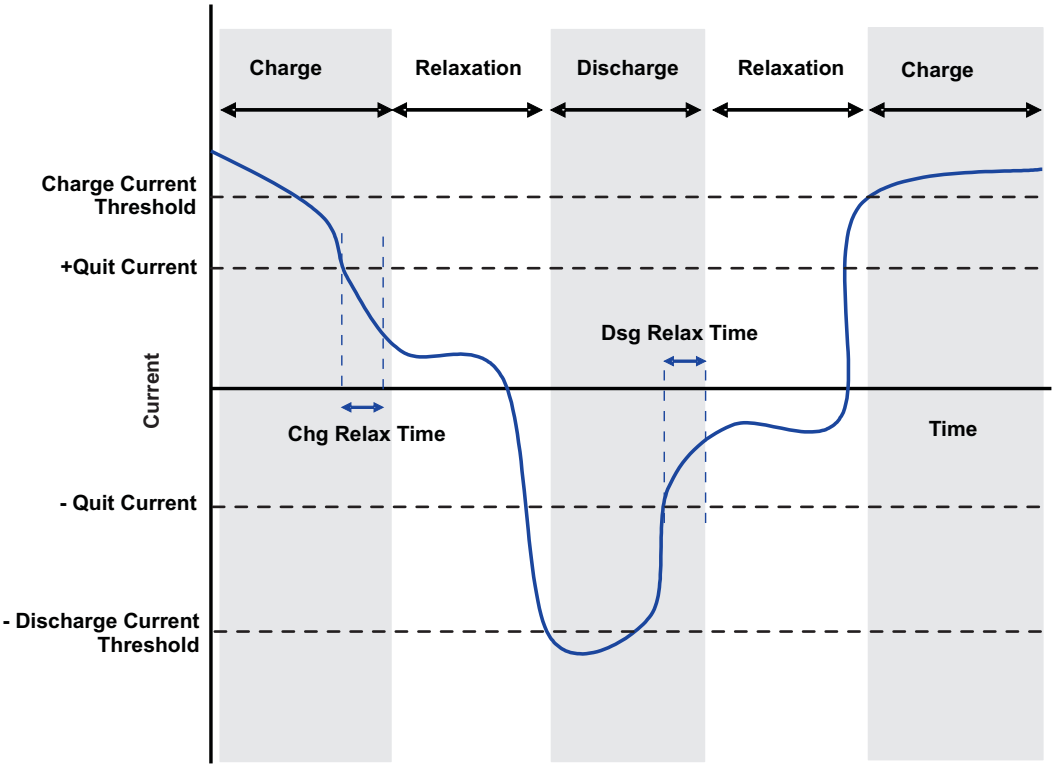


Figure 2. Algorithm Operation Mode Changes With Varying Battery Current

The SOC is estimated based on the OCV of the battery because of a strong correlation of SOC to OCV for a particular battery chemistry, shown in Figure 3 as an example. In the relaxation mode, where no load current is present and the current is below a user-chosen *quit current* level, the SOC is determined using the measured cell voltage (must meet certain voltage settling criteria; for details, see the*Gas Gauging* sections in the chipset technical reference manuals SLUU250 and SLUU251) and the predefined OCV versus SOC relationship.

During charging and discharging, the SOC is continuously calculated using the relationship of present Qmax to the integrated passed charge measured by the coulomb counter ADC:

$$Q_{max} = \frac{Passedcharge}{|SOC1 - SOC2|} \quad (1)$$

The derivation of this equation is discussed in the following paragraphs. Figure 4 graphically illustrates some of the Impedance Track™ terminology.

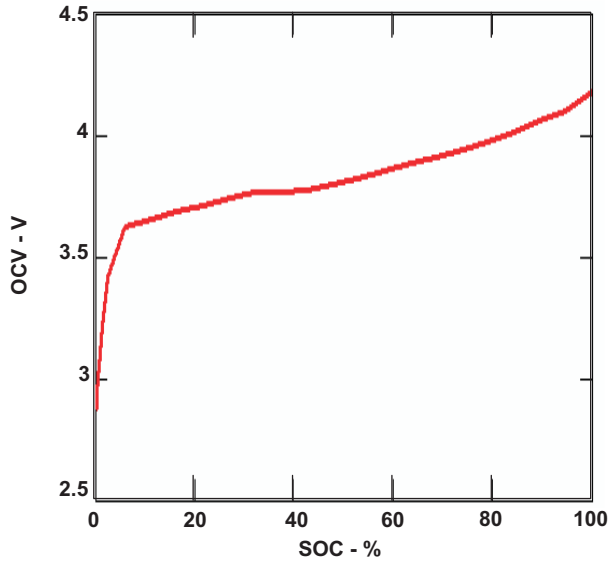


Figure 3. SOC Dependency on OCV

It is most effective to familiarize the reader with some important Impedance Track™ terminologies using Figure 4.

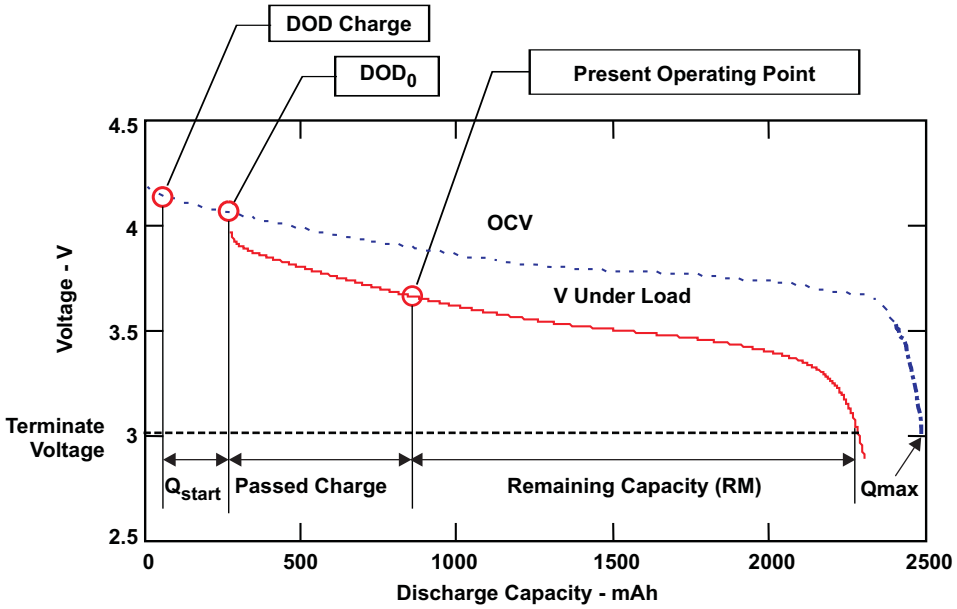


Figure 4. OCV Characteristics (Dotted Curve) and Battery Discharge Curve Under Load (Solid Curve)

Qmax is calculated with two OCV readings (leading to calculation of two SOC values, SOC1 and SOC2) taken at fully relaxed state (dV/dt < 4 µV/s) before and after charge or discharge activity and when the passed charge is more than 37% of battery design capacity, using Equation 2:

$$SOC1 = \frac{Q1}{Qmax},\ SOC2 = \frac{Q2}{Qmax} \quad (2)$$

Subtracting these two equations yields

$$Q_{max} = \frac{Passedcharge}{|SOC1 - SOC2|},\ \text{where Passedcharge} = |Q1 - Q2|. \quad (3)$$

This equation demonstrates that it is unnecessary to have a complete discharge cycle to learn the battery chemical capacity.

When an external load is applied, the impedance of each cell is measured by finding the difference between the measured voltage under load and the open-circuit voltage (OCV) specific to the cell chemistry at the present state-of-charge (SOC). This difference, divided by the applied load current, yields the impedance. In addition, the impedance is correlated with the temperature at time of measurement to fit in a model that accounts for temperature effects.

With the impedance information, the remaining capacity (RM) can be calculated using a voltage simulation method implemented in the firmware. The simulation starts from the present DOD, i.e., DOD_{start} and calculates a future voltage profile under the same load with a 4% DOD increment consecutively:

$$V(DOD_I,T) = OCV\ (DOD_I,T) + I \times R(DOD_I,T),$$

where $DOD_I = DOD_{start} + I \times 4\%$ and I represents the number of increments, and $R(DOD_I,T)$ is the battery impedance under DOD_I and temperature T. Once the future voltage profile is calculated, the Impedance Track™ algorithm predicts the value of DOD that corresponds to the system termination voltage and captures this as DOD_{final}. The remaining capacity then is calculated using:

$$RM = (DOD_{final} - DOD_{start}) \times Q_{max}$$

FCC (full-charge capacity) is the amount of charge passed from the fully charged state to the Termination Voltage, and can be calculated using:

$$FCC = Qstart + PassedCharge + RM$$

The following section presents a more detailed description of the gas gauge hardware.

Gas Gauge Hardware

1.2.3.2 The bq29330 Analog Front-End Protector The bq29330 AFE serves an important role for the bq20z70/z90 2-, 3-, or 4-cell lithium-ion battery pack gas gauge chipset solution. The bq29330 powers the bq20z70/z90 directly from its 2.5-V, 16-mA low-dropout regulator (LDO), which is powered by either the battery voltage or the pack+ voltage. The AFE also provides all the high-voltage interface needs (the battery cell voltage levels need to be down-converted to meet the input range requirement of bq20z70/z90 ADC) and current protection features. The AFE offers an I^2C-compatible interface to allow the bq20z70/z90 to have access to the battery information and to configure the AFE's protection features. Other features of the AFE include cell balance control, thermistors drive circuit, precharge function, etc. A functional block diagram is provided in Figure 5.

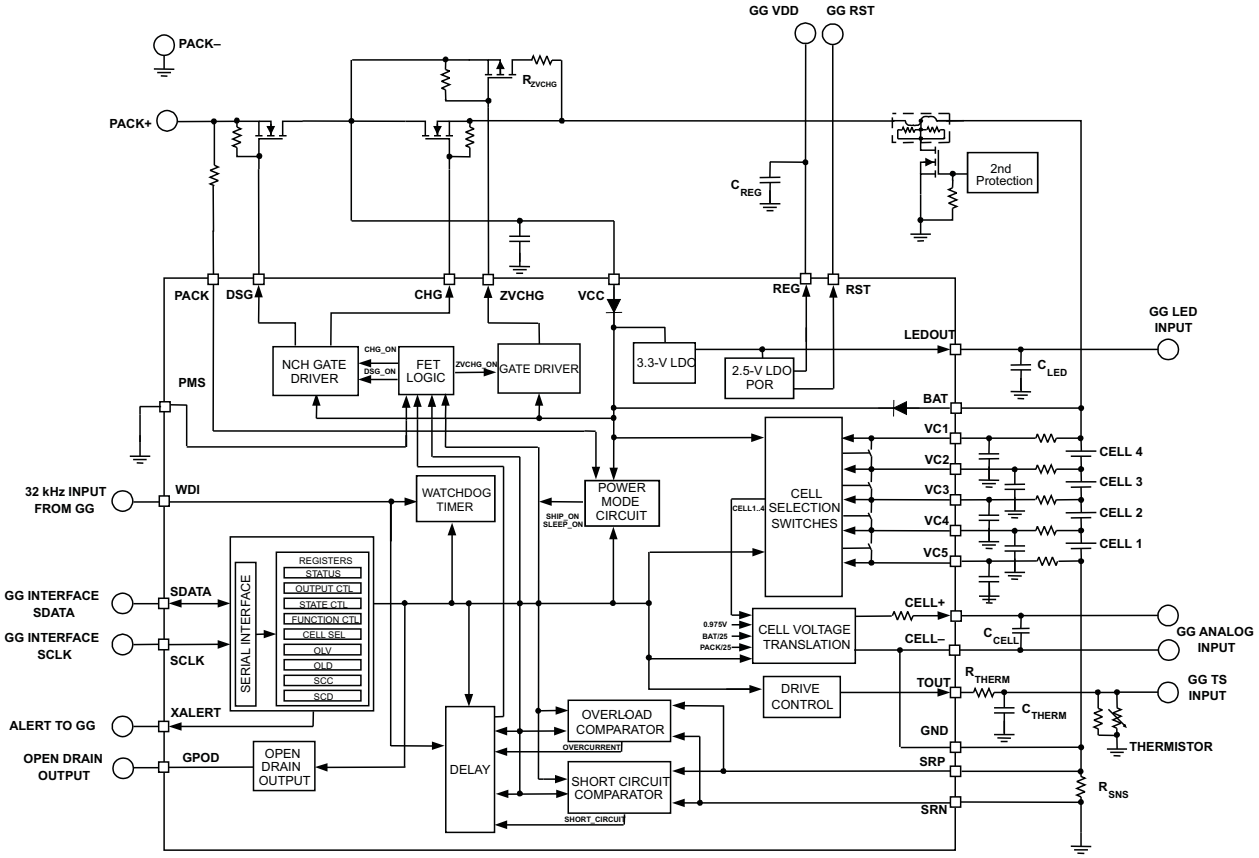


Figure 5. bq29330 Functional Block Diagram

The AFE can be configured to translate each of the series cell voltages or the pack voltage into ground-referenced voltage, which can be measured by the bq20z70/z90 gas gauge IC. The allowable AFE input range for an individual cell is 0 V to 4.5 V. Because voltage measurement accuracy is crucial for minimizing battery capacity estimate errors, the bq29330 AFE provides means for the bq20z70/z90 to measure its voltage monitor amplifier offset and gain errors, leading to accurate gas gauge calibration.

In many situations, the state-of-charge (SOC) of the individual cells may differ from each other in a multicell battery pack, causing cell imbalance and voltage difference between cells. The bq29330 AFE incorporates a bypass path for each of the series element. These bypass paths can be used to reduce the charging current into any cell and thus allow for an opportunity to balance the SOC of the cells during charging. The bq20z70/z90 enables and disables these paths as needed through the I^2C bus.

The bq29330 is also responsible for overload and short-circuit detection and protection of the pass FETs (i.e., charge and discharge FETs), cells, and any other inline components from excessive current conditions. The overload detection is used to detect excessive currents in the discharge direction, whereas the short-circuit detection is used to detect excessive current in either the charge or discharge direction. Threshold and delay time of overload and short-circuit can be programmed by bq20z70/z90. When an overload or short-circuit is detected and a programmed delay time has expired, the FETs are turned off and the details of the condition are reported in the Status (b0:b2) register of bq29330. Next, the XALERT output is triggered, signaling the bq20z70/z90 to investigate the failure.

Another feature of the AFE is the precharging function. In some cases, the battery that needs to be charged is deeply depleted. When the CHG-FET is turned on, the voltage at the pack pin of bq29330 is as low as the battery voltage, which can be too low for the AFE to operate. The bq29330 provides three precharging/0-V charging options to remedy this problem.

1.2.3.3 How the bq20z70/z90 and bq29330 Operate Together The bq20z70/z90 is the master of this chipset because it implements the entire Impedance Track™ algorithm. The bq29330 is configured by the bq20z70/z90 for how it should respond to handle gas-gauging situations. These include when and which cell voltage information it needs to provide to the gas gauge IC, and what overload and short-circuit threshold and delay value should be used.

On the other hand, the bq20z70/z90 requires the bq29330 to create a full solution for 2-, 3- or 4-series-cell Li-ion battery packs. The bq20z70/z90 cannot operate without the AFE. As shown in Figure 1, the bq20z70/z90 relies on the AFE to provide scaled cell/pack voltage information to perform gas gauging and voltage/current protection functions. The bq20z70/z90 can only access the charge and discharge FETs by sending control commands to the AFE. The bq20z70/z90 has two tiers of charge/discharge overcurrent protection settings, and the AFE provides a third level of discharge overcurrent protection. In case of a short-circuit condition, which does not need more than a brief time to damage the circuit, the gas gauge chipset entirely depends on the AFE to autonomously shut off the FETs before such damage occurs.

1.2.3.4 The bq2941x 2nd-Level Overvoltage Protector Although the bq20z70/z90 and its associated AFE provide overvoltage protection, the sampled nature of the voltage monitoring limits the response time of this protection system. Most applications require a fast-response, real-time, independent overvoltage monitor that operates with the bq20z70/z90 and the AFE. Texas Instruments offers the bq2941x 2nd-level protector IC for this purpose. The bq2941x monitors individual cell voltages independently of the gas gauge and AFE and provides a logic-level output that toggles if any of the cells reaches a hard-coded overvoltage limit. The response time of the IC is determined by the value of an external delay capacitor. In a typical application, the output of the bq2941x would be tied to a heater fuse or other fail-safe protection device.

bq20z70/z90 Evaluation Module

The bq20z70EVM-001 and bq20z90EVM-001 evaluation modules (EVM) are complete evaluation systems for the bq20z70/z90/bq29330/bq29412 battery pack electronics system. The EVM includes:

1. One bq20z70/z90/bq29330/bq29412 circuit module
2. A current sense resistor
3. Two thermistors
4. An EV2300 PC interface board for gas gauge interface
5. A PC USB cable
6. Windows™-based PC software

The circuit module includes one bq20z70/z90 IC, one bq29330 IC, one bq29412 IC, and all other onboard components necessary to monitor and predict capacity, perform cell balancing, monitor critical parameters, protect the cells from overcharge, overdischarge, short-circuit, and overload in 2-, 3-, or 4-series-cell Li-ion or Li-polymer battery packs. The circuit module connects directly across the cells in a battery. With the EV2300 interface board and software, the user can read the bq20z70/z90 data registers, program the chipset for different pack configurations, log cycling data for further evaluation, and evaluate the overall functionality of the bq20z70/z90/bq29330/bq29412 solution under different charge and discharge conditions.

bqEVSW Software for Use With the bq20z70/z90

The bqEVSW is a Windows™-based evaluation software program provided by TI for functional evaluation of the bq20z70/z90/bq29330/bq2941x chipset. The bqEVSW provides the standard Smart Battery System (SBS) data commands as well as extended SBS commands. On opening the software, it automatically detects the presence of EV2300 USB module and the chipset. Once the device type and version of firmware are identified, the software displays the SBS interface. The users may also toggle between SBS, Data Flash, Calibration, and Pro screens for a variety of information about the battery pack and the chipset settings. The bqEVSW also can be used to program or update the firmware of the bq20z70/z90 and for battery cycle data logging. See the bq20z70/z90 EVM user's guide and application reports for more information.

1.3 Next Steps

Developing a PCB for the bq20z70/z90 and bq29330 Chipset

Using the bq20z90 3-cell reference design schematic in section 4.1 as a guide, a battery pack schematic should be designed to meet the individual requirements. Start with the number of cells. Note that in this schematic, pins VC1 and VC2 are connected on both the bq29330 and the bq29412. For packs with 2-series cells, connect VC1, VC2, and VC3 of each device together and remove the filter components R10, C17, R6, and C8. For a 4-cell design, follow the pattern of the 3-cell schematic but add an additional RC network at the VC1 input of both ICs.

Next, the current-sense resistor should be selected. As a general guideline, 20 mΩ is appropriate for a single (1P) string of 18650 cells, whereas 10 mΩ is recommended for a 2P pack. See the bq29330 data-sheet tables to ensure that the desired short-circuit and overcurrent protection levels fall within the available range for the selected sense resistor.

The use of a chemical fuse is recommended. Using information from the fuse data sheet, ensure that the FET used to ignite the fuse has a low enough on-resistance to succeed in opening the fault. Also, note that the gate of Q1 (see the reference design schematic in section 4.1) is driven by a 2.5-V output port from the bq20z90 in series with a Schottky diode. Ensure that the selected FET turns on adequately to provide the required ignition current. The output voltage of the bq29412 is approximately 6 V, providing an adequate 3 V to the gate of Q1.

The bq29330 is flexible with regard to the precharge function. The reference design schematic uses the *Common FET* mode for precharge, where the Charge FET is turned on at initialization allowing for precharge current to flow. Two other precharge modes also are supported, but require the use of a dedicated precharge FET. The data sheet of bq29312A, although an earlier device, contains detailed theory of operation for each mode.

Printed-circuit board layout requires careful consideration when developing a smart battery application. The high currents developed during a battery short-circuit event can be incompatible with the micropower design of the semiconductor devices. It is important to realize that battery transients can be capacitively or magnetically coupled into low-level circuits resulting in unwanted behavior. Success with a first-pass design can depend on realizing that parallel circuit board traces are indeed small capacitors and current transformers. The ideal board layout would have the entire high-current path physically located away from the low-current electronics. Because this is not often possible, the coupling principle must be taken into account. Short-circuit, ESD, and EMI testing should be part of the initial checkout of a new design.

With regard to component placement, several components surrounding the bq20z90 need special attention. Most important are the two, power-supply decoupling capacitors C14. This must be close to the gas gauge device and have low-resistance/low-inductance connections that do not form a large loop, C14 should be placed between pins 25 and 26. D7 must either be placed close to U3 or connect to it with a trace shielded to ground on both sides to prevent RF interference.

Proper sensing of voltage and current requires the use of Kelvin connections at the sense resistor and at the top and bottom battery terminals. If top and bottom connections to the cells allow too much voltage drop, then the resulting error in cell voltage measurement has an effect on the measurement accuracy of battery capacity and therefore the remaining run time.

It Is important to have correct grounding. On the reference design schematic, note that the low-level ground connects to Pack– at the sense resistor. The Pack– terminal (also known as ESD ground) is the suggested return point for C23, SW1, and the D8 network. For additional information, see the TI application report *Avoiding ESD and EMI Problems in bq20zxxx Battery Pack Electronics* (SLUA368).

Solution Development Process

Browsing the data flash screens of the bq20z70/z90 evaluation software can be a challenging experience. Approximately 300 individual settings are possible. However, the default value for most of them can be easily used. The first step is to set up the data flash values for the number of cells and the coulomb capacity for a specific application. This simple process is described in detail in the application report *bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity* (SLVA208). This report applies directly to the bq20z70/z90.

With different numbers of cells, several voltage settings must change. Application report SLVA208 presents the suggested default settings for Pack Over Voltage, Pack Under Voltage, Safety Over Voltage, Charging Voltage, Design Voltage, Cell Configuration, Flash Update OK Voltage, Shutdown Voltage, Charger Present Voltage, and Charge Terminate Voltage.

With different types of cells and number of parallel cells, capacity settings are different. Suggested values are presented for Qmax Cells, Qmax Pack, Design Capacity, and Design Energy in the same application report (SLVA208).

With the preceding changes in place, the evaluation module should function normally with the target cell configuration. The next step is to review all of the selectable features in the configuration registers A and B. Use the technical reference manuals to review each configuration bit in these registers and configure them for a specific application. Note that if you use the default of 0 for the NR bit in Configuration Register B, then a System_Present signal needs to be implemented on the pack connector. See the EVM user's guide (SLUU234 and SLUU242) schematic or reference schematic in this document for implementation details.

Mass Production Setup

One of the main benefits of Impedance Track™ technology is the significant reduction in the complexity of battery pack mass production. Because many data flash values are adaptively derived with use, it is possible to simply transfer the knowledge gained from a single *golden* pack to each individual pack as it leaves the assembly line. Charging and discharging each pack in order to force it to learn its capacity are unnecessary. Although the individual packs will contain cells with varying impedances, that is quickly corrected during normal use as impedance is constantly measured and updated by the bq20z70/z90 gas gauge.

A good strategy for production is a 7-step process flow:

1. Write the data flash image to each device. This image was read from a *golden* pack
2. Calibrate the device.
3. Update any individual flash locations, such as serial number, lot code, and date.
4. Perform any desired protection tests.
5. Connect the cells.
6. Initiate the Impedance Track™ algorithm (MFR access code 0x21).
7. Seal the pack (MFR access code 0x20).

The TI application report *Data Flash Programming/Calibrating the bq20z70/z90 Gas Gauges* (SLUA379) discusses the first three steps in detail. TI application report *Pack Assembly and the bq20z80* (SLUA335) discusses step 5 in detail. Calibration is presented as sample VB6 code for those who wish to develop their own calibrator. However, Texas Instruments has higher-level support for high-speed programming and calibration steps. A single channel test and calibration program is available, with open-source code. Also, a multistation test system is available at nominal cost.

For additional application reports covering various aspect of bq20z70/z90 Impedance Track™ solution, see the Texas Instruments bq20z70/z90 online product folder.

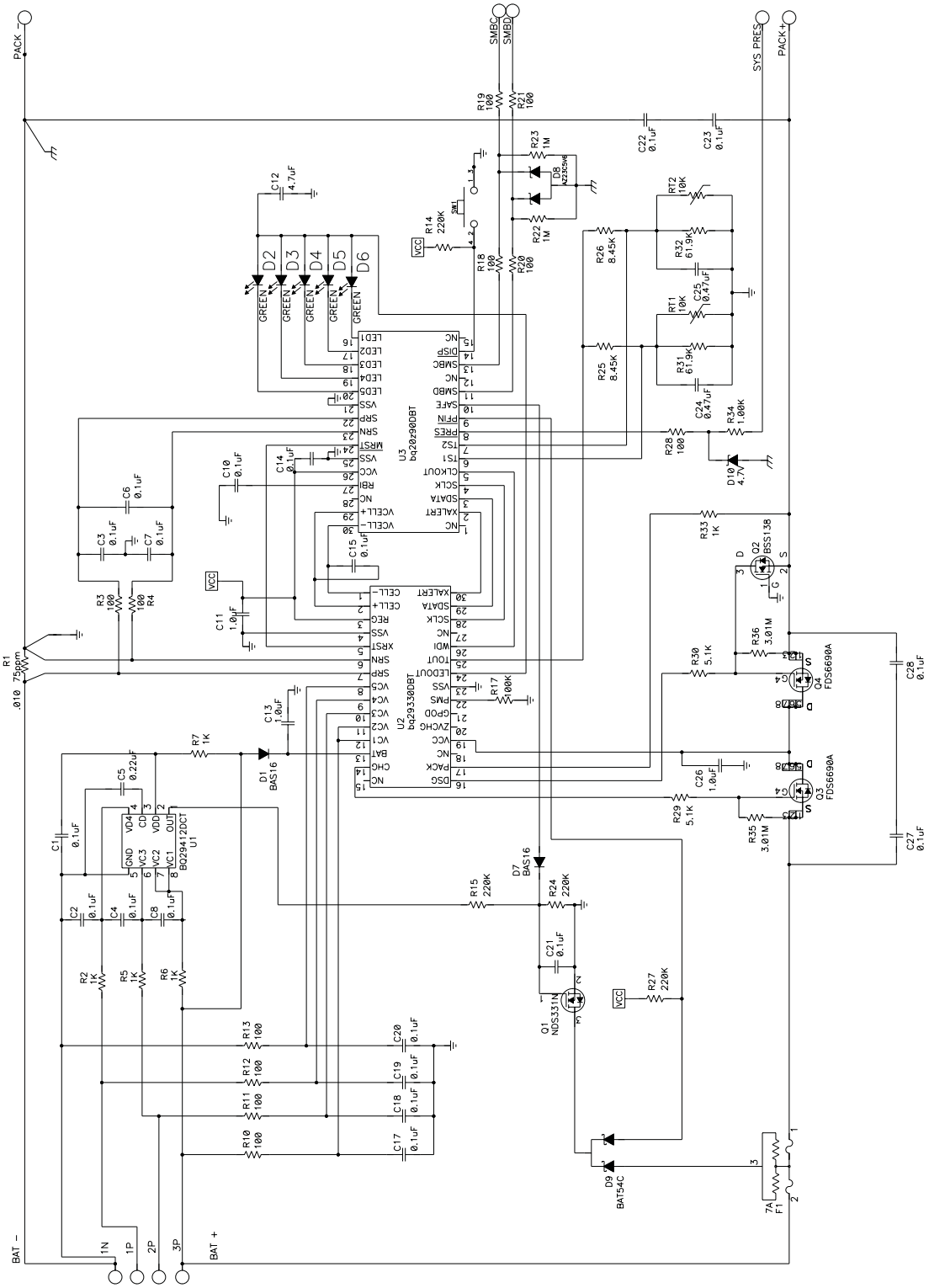
1.4 Glossary

- OCV: Open-circuit voltage of a battery
- Passed Charge: Coulomb counter integrated charge during battery discharge or battery charge
- Qmax: Maximum battery chemical capacity
- Design Capacity: Cell chemical capacity specified by cell manufacturer times number of paralleled cells
- SOC: State-of-charge at any moment, defined as SOC=Q/Qmax (usually in %), where Q is the Passed Charge from full charge state
- DOD: Depth of discharge; DOD= 1-SOC (usually in %)
- DOD_0: Last DOD reading before charge or discharge
- DODcharge: DOD for a fully charged pack
- Qstart: Charge that would have passed from fully charged state to make DOD = DOD_0
- RM: Remaining capacity, in mAh or mWh

- FCC: Full-charge capacity, the amount of charge passed from the fully charged state to the terminate voltage, in mAh or mWh
- Quit current: user-defined current levels for both charge and discharge, usually about ~10 mA
- Relaxation mode: the state of the battery when the current is below user-defined *quit current* levels and after a user-defined minimum charge relax time (see Figure 2)
- AFE: Analog front-end, in this document, this refers to the bq29330

Reference Design Schematic

The reference design schematic is affixed to this page.



Configuring the bq20z90 Data Flash

Battery Management

ABSTRACT

The bq20z90 has numerous data flash constants that can be used to configure the device with a variety of different options for most features. The data flash of the bq20z90 is split into sections which are described in detail within this document.

2.1 Glossary

ASOC: **Absolute State of Charge**

Bit: **This word has a different meaning than Flag. This word is used to refer to a configuration setting bit. It is primarily used in data flash settings.**

Blink, Flash and Delay: **There are 3 different display modes for the LEDs in this document that need clarification.**

- **Blinking: When the display is said to be blinking, then the word "blinking" is used to refer to the LED located closest to the LED used to indicate 100% that is illuminated and "blinking" when the LED display is activated and displaying SOC (state of charge). Only this "topmost" activated LED in the display blinks. All other LEDs that are activated is steady state when activated. (see *LED Blink Rate*)**
- **Flashing: When the display is said to be flashing, then the word "flashing" means all LEDs that are activated to indicate the SOC will flash with a period of (2 ×*LED Flash Rate*).**
- **Delay: When the display is activate, all LEDs that are required to indicate the SOC may not illuminate at the same time. Starting from the LED that represents the lowest SOC, there can be a delay (*LED Delay*) between each LED illuminating from the LED that represents the lowest possible SOC up to the LED that represents the present SOC.**

***Cell Voltage(Max)*:** **This represents the maximum value among all the SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)**

***Cell Voltage(Min)*:** **This represents the minimum value among all the SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)**

***Cell Voltage(Any)*:** **This represents any of the possible SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)**

[DSG] in *Battery Status*: **SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. This can be confused in many descriptions in this document because different functions require different methods for determining charging or discharging. The SBS description sometimes does not give enough resolution for correct part function so these functions require other data flash registers as described in their respective definitions. SBS states that if the battery is charging then [DSG] is 0, and any other time (Current less than or equal to 0), the [DSG] flag is set. The actual formula that the bq20z90 uses for setting or clearing the [DSG] flag are as follows:**

[DSG] clear: **[DSG]=0 if *Current* >= Chg Current Threshold**

[DSG] set: **[DSG]=1 if**

1. **Current <= Dsg Current Threshold or**
2. **Relaxation Mode which is defined by one of the following statements:**
   - **A) *Current* transitioning from below (–)*Quit Current* to (above (–)*Quit Current* and below *Quit Current*) for *Dsg Relax Time***
   - **B) *Current* transitioning from above *Quit Current* to (below *Quit Current* and above (–)*Quit Current*) for *Chg Relax Time***

FCC: Full Charge Capacity

FET opened/Closed: It is common to say FET opened or FET closed. This is used throughout this document to mean the FET is turned off or the FET is turned on respectively.

Flag: This word is usually used to represent a read only status bit that indicates some action has occurred or is occurring. This bit usually cannot be modified by the user.

Precharge/ZVCHG: The words Precharge and ZVCHG are interchangeable throughout the document

RCA: Remaining Capacity Alarm

RM: Remaining Capacity

RSOC: Relative state of Charge

RTA: Remaining Time Alarm

SAFE and $\overline{\text{SAFE}}$: These words are used throughout this document to represent 2 output pins on the bq20z90. SAFE is pin 7 on the bq20z90 and $\overline{\text{SAFE}}$ is pin 12. When this document discusses permanent failures, it normally includes a discussion of these two pins. When a permanent failure happens and its control bit is enabled, then these 2 pins are activated to either blow a fuse or to activate some hardware protection. The reason there are 2 outputs is for backwards compatibility with bq20z8X parts and to give options for an application. Both outputs are activated at the same time when enabled, but the $\overline{\text{SAFE}}$ pin is active low so it is driven low when activated while the SAFE pin is active high and is driven high when activated.

SOC: This is used as a generic meaning of State-of-Charge. It can mean RSOC, ASOC, or percentage of actual chemical capacity.

System: The word system is sometimes used in this document. It always means a host system that is consuming current from the battery pack that includes the bq20z90.

***Italics*:** All words in this document that are in italics represent names of data flash locations exactly as they are shown in the EV software.

***Bold Italics*:** All words that are bold italic represent SBS compliant registers exactly as they are shown in the EV software.

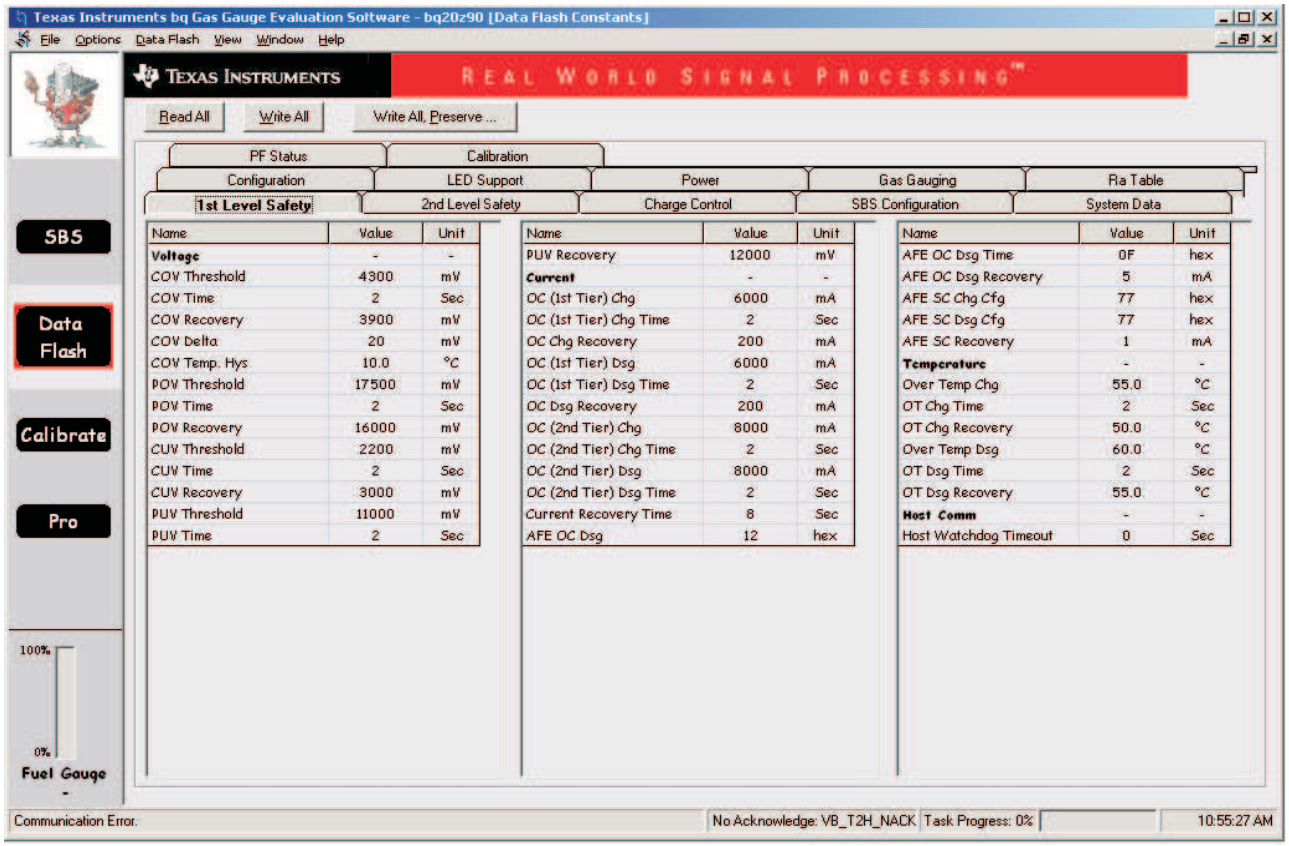
[brackets]: All words or letters in brackets represent bit/flag names exactly as they are shown in the SBS and Data Flash in the EV software.

(–): This is commonly used in this document to represent a minus sign. It is written this way to ensure that the sign is not lost in the translation of formulas in the text of this document.

2.2 Data Flash Descriptions

1st Level Safety

All 1st Level Safety functions are temporary. There should be no permanent failures or damage to the battery if any of the 1st Level Safety functions are triggered.



Name	Value	Unit
Voltage	-	-
COV Threshold	4300	mV
COV Time	2	Sec
COV Recovery	3900	mV
COV Delta	20	mV
COV Temp. Hys	10.0	°C
POV Threshold	17500	mV
POV Time	2	Sec
POV Recovery	16000	mV
CUV Threshold	2200	mV
CUV Time	2	Sec
CUV Recovery	3000	mV
PUV Threshold	11000	mV
PUV Time	2	Sec

Name	Value	Unit
PUV Recovery	12000	mV
Current	-	-
OC (1st Tier) Chg	6000	mA
OC (1st Tier) Chg Time	2	Sec
OC Chg Recovery	200	mA
OC (1st Tier) Dsg	6000	mA
OC (1st Tier) Dsg Time	2	Sec
OC Dsg Recovery	200	mA
OC (2nd Tier) Chg	8000	mA
OC (2nd Tier) Chg Time	2	Sec
OC (2nd Tier) Dsg	8000	mA
OC (2nd Tier) Dsg Time	2	Sec
Current Recovery Time	8	Sec
AFE OC Dsg	12	hex

Name	Value	Unit
AFE OC Dsg Time	0F	hex
AFE OC Dsg Recovery	5	mA
AFE SC Chg Cfg	77	hex
AFE SC Dsg Cfg	77	hex
AFE SC Recovery	1	mA
Temperature	-	-
Over Temp Chg	55.0	°C
OT Chg Time	2	Sec
OT Chg Recovery	50.0	°C
Over Temp Dsg	60.0	°C
OT Dsg Time	2	Sec
OT Dsg Recovery	55.0	°C
Host Comm	-	-
Host Watchdog Timeout	0	Sec

Voltage

COV Threshold

When any cell voltage measured by ***Cell Voltage (Any)*** rises to this threshold, then the Cell Over Voltage (COV) protection process is triggered, initiating a [COV] in ***Safety Alert*** for *COV Time*. If the COV condition clears prior to the expiration of the *COV Time* timer, then [COV] in *Safety Alert* is cleared and no [COV] flag is set in ***Safety Status***. If the COV condition does not clear, then [COV] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. Setting *COV Time* to 0 completely disables this function.

Normal Setting: Default is 4300 mV. This cell is chemistry dependent, but 4200-4300 is the most common settings.

COV Time

See *COV Threshold*. This is a buffer time allotted for a COV condition. The timer starts after [COV] is set in ***Safety Alert***. When it expires, then the bq20z90 forces [COV] set in ***Safety Status*** and opens the Charge FET. If the condition clears prior to the expiration of the *COV Time* timer, then the [COV] is cleared in ***Safety Alert*** and the COV Time timer resets without setting [COV] in ***Safety Status***. Setting *COV Time* to 0 completely disables *COV Threshold*.

Normal Setting: This is normally set to 2 seconds, but depends on the application.

COV Recovery

When a [COV] is set in ***Safety Status***, it is only cleared when **ALL** cell voltages as measured by ***Cell Voltage(All)*** fall below this threshold.
Normal Setting: This defaults to 3900 mV. It must be set low enough that the hysteresis between *COV Threshold* fault and this recovery prevents oscillation of the Charge FET.

COV Delta

The actual trigger value for *the COV Threshold* is adjusted down by this amount if ***Temperature*** rises above (*Over Temperature Threshold – COV Temp Hys*). The actual Data Flash location for *COV Threshold* is not modified, just the trigger value. It returns to normal if the temperature falls below (*Over Temperature Threshold – COV Temp Hys*). If this time is set to 0, then the *COV Threshold* trigger value is not modified based on the temperature.

Normal Setting: This value is normally set to 20 mV. This is application and cell chemistry dependent.

COV Temp Hys

See *COV Delta*. This is the delta temperature below the *Over Temperature Threshold* where the *COV Threshold* is modified by *COV Delta*.

Normal Setting: This value is normally set to 100 in 0.1°C. This is application and cell chemistry dependent.

POV Threshold

When the pack voltage measured by ***Voltage*** rises to this threshold, then the Pack Over Voltage (POV) protection process is triggered. This process starts by setting [POV] in ***Safety Alert*** for POV Time. If the POV condition clears prior to the expiration of the *POV Time* timer, then the [POV] is cleared in ***Safety Alert*** with no [POV] being set in ***Safety Status***. If the POV condition does not clear, then [POV] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. Setting *POV Time* to 0 completely disables this function.

Normal Setting: This register defaults to 17500 which is for a 4-cell pack. This is high, but it depends on the cell chemistry and the number of cells in series for an application. It is normally set to the (number of cells × 4300 mV). (i.e., 8600 mV for 2-cell applications, 12900 mV for 3-cell, and 17200 mV for 4-cell applications)

POV Time

See *POV Threshold*. This is a buffer time allotted for a POV condition. The timer starts after the [POV] is set in ***Safety Alert***. When it expires, then the bq20z90 forces [POV] set in ***Safety Status*** and opens the Charge FET. If the condition clears prior to the expiration of the *POV Time* timer, then [POV] is cleared in ***Safety Alert*** and the *POV Time* timer resets. Setting *POV Time* to 0 completely disables *POV Threshold*.

Normal Setting: This is normally set to 2 seconds, but depends on the application.

POV Recovery

When [POV] is set in ***Safety Status***, it is only cleared when the pack voltage measured by ***Voltage*** falls below this threshold.

Normal Setting: This defaults to 16000 mV. It must be set low enough that the hysteresis between *POV Threshold* fault and this recovery prevents oscillation of the Charge FET.

CUV Threshold

When any cell voltage measured by ***Cell Voltage(Any)*** falls below this threshold, then the Cell Under Voltage (CUV) protection process is triggered, initiating a [CUV] flag getting set in ***Safety Alert*** for *CUV Time*. If the CUV condition clears prior to the expiration of the *CUV Time* timer, then [CUV] is cleared in ***Safety Alert*** and no [CUV] is set in ***Safety Status***. If the CUV condition does not clear, then a [CUV] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [TDA] and [FD] in ***Battery Status*** to be set. It also causes [XDSG] in ***Operation Status***. Setting *CUV Time* to 0 completely disables this function.

Normal Setting: Default is 2200 mV. This is cell chemistry dependent but 2200 mV–2300 mV is the most common setting.

CUV Time

See *CUV Threshold*. This is a buffer time allotted for a CUV condition. The timer starts after [CUV] is set in ***Safety Alert***. When it expires, then the bq20z90 forces [CUV] set in ***Safety Status*** and opens the Charge FET. If the condition clears prior to the expiration of the *CUV Time* timer, then [CUV] is cleared in ***Safety Alert*** and the *CUV Time* timer resets. Setting *CUV Time* to 0 completely disables *CUV Threshold*.

Normal Setting: This is normally set to 2 seconds but depends on the application.

CUV Recovery

When [CUV] is set in ***Safety Status***, it is only cleared when **ALL** cell voltages as measured by ***Cell Voltage(All)*** rise above this threshold.

Normal Setting: The default for this register is 3000 mV. It must be set high enough that the hysteresis between *CUV Threshold* fault and this recovery prevents oscillation of the Discharge FET.

PUV Threshold

When the pack voltage measured by ***Voltage*** falls below this threshold, then the Pack Under Voltage (PUV) protection process is triggered, initiating a [PUVt] in ***Safety Alert*** for *PUV Time*. If the PUV condition clears prior to the expiration of the *PUV Time* timer, then [PUV] is cleared in ***Safety Alert*** and [PUV] are not set in ***Safety Status***. If the PUV condition does not clear, then a [PUV] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [TDA] and [FD] in ***Battery Status*** to be set. It also causes [XDSG] in ***Operation Status***. Setting *PUV Time* to 0 completely disables this function.

Normal Setting: This register defaults to 11000 which is for a 4-cell pack. This is very application and cell chemistry dependent. It also depends on the number of cells in series for an application. A very common setting is the (number of cells $\times$ 2750 mV). i.e., 5500 mV for 2-cell applications, 8250 mV for 3-cell, and 11000 mV for 4-cell applications)

PUV Time

See *PUV Threshold*. This is a buffer time allotted for a PUV condition. The timer starts after [PUV] is set in ***Safety Alert***. When it expires, then the bq20z90 forces [PUV] set in ***Safety Status*** and opens the Discharge FET. If the condition clears prior to the expiration of the *PUV Time* timer, then [PUV] is cleared in ***Safety Alert*** and the *PUV Time* timer resets. Setting *PUV Time* to 0 completely disables *PUV Threshold*.

Normal Setting: This is normally set to 2 seconds but depends on the application.

PUV Recovery

When [POV] is set in ***Safety Status***, it is only cleared when the pack voltage measured by ***Voltage*** falls below this threshold.

Normal Setting: The default for this register is 12000 mV. Set high enough that the hysteresis between *PUV Threshold* fault and this recovery prevents oscillation of the Discharge FET.

Current

There are 3 levels or tiers of current protection in the bq20z90. The first 2 levels, 1st Tier and 2nd Tier are slow responding (>1 second). The third level is a quick responding current protection controlled directly by the bq29330.

It is important that the bq29330 makes the triggering decision for any of the AFE fault conditions. This is to ensure quick response to dangerous faults. It is also designed in such a way that the AFE can act completely autonomously in the event of damage to the bq20z90 in the triggering of any AFE fault. The bq29330 cannot; however, clear the fault condition. It is cleared only by the bq20z90. The AFE data is transferred to the bq29330 on reset and (if enabled in the **AFE Verification** subclass) is continually monitored by the bq20z90 to ensure no corruption has occurred at any time. If corruption has occurred, the bq20z90 attempts to make corrections. If after repeated attempts (as set in the **AFE Verification** subclass), it cannot correct the condition, then it sets a permanent failure. If enabled in *Permanent Fail Cfg*, then the SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. (See *Permanent Fail Cfg*)

OC (1st Tier) Chg

When current measured by ***Current*** reaches up to or above this threshold during charging, then the 1st Tier Over Current in the Charge [OCC] protection process is triggered, initiating an [OCC] in ***Safety Alert*** for *OC (1st Tier) Chg Time* in seconds. If the 1st Tier OCC condition clears prior to the expiration of the *OC (1st Tier) Chg Time* timer, then [OCC] in ***Safety Alert*** is cleared and no [OCC] is set in *Safety Status*. If the 1st Tier OCC condition does not clear, then a [OCC] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.

Normal Setting: This register is application dependent. It should be set above the absolute maximum expected discharge current. It should be set high enough that unexpected mild charge spikes or inaccuracies do not create a false over current trigger, but low enough to force the Charge FET to open before damage occurs to the pack.

OC (1st Tier) Chg Time

See *OC(1st Tier) Chg*. This is a buffer time allotted for a 1st tier Over Current condition. The timer starts every time the [OCC] in ***Safety Alert*** is initially set. When the timer expires, then the bq20z90 forces an [OCC] in ***Safety Status*** and opens the Charge FET. If [OCC] in ***Safety Alert*** clears prior to the expiration of the *OC (1st Tier) Chg Time* timer, then [OCC] in ***Safety Alert*** is cleared and the *OC (1st Tier) Chg Time* timer resets. Setting the *OC (1st Tier) Chg Time* to 0 disables OC (1st Tier) Chg.

Normal Setting: This is normally set to 2 seconds, but depends on the application. It must be set long enough to prevent false triggering of the [OCC] in ***Safety Status***, but short enough to prevent damage to the battery pack.

OC Chg Recovery

OC Chg Recovery is one of several recovery methods used for both 1st and 2nd level Over Current in the charge direction faults. This value is used for either nonremovable packs ([NR] in *Operation Cfg B =1)* or for removable packs configured ([OCC] in *Non-Removable Cfg)*. With either of these settings, ***Average Current*** must fall below this value for *Current Recovery Timer* in seconds to clear the [OCC] or the [OCC2] in ***Safety Status*** if either is set.

Normal Setting: This register is application dependent, but is normally set low enough that it prevents quick oscillation in the Charge FET. ***Average Current*** is used for this recovery function and falls every second that it is recomputed with ***Current*** at or near 0. If this recovery is set too high, then the Charge FET can oscillate with a frequency that is fast enough to cause damage to the battery pack because the ***Average Current*** falls below this value quickly.

OC (1st Tier) Dsg

When current measured by ***Current*** falls down to or below this threshold during discharging then the 1st Tier Over Current in discharge (OCD) protection process is triggered, initiating an [OCD] in ***Safety Alert*** for *OC (1st Tier) Dsg Time* in seconds. If the 1st Tier OCD condition clears prior to the expiration of the *OC (1st Tier) Dsg Time* timer, then the [OCD] is cleared and no [OCD] is set. If the 1st Tier OCD condition does not clear, then a [OCD] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [XDSG] and [XDSGI] in ***Operation Status*** to be set. It also causes ***Charging Current*** to be set to 0.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent. It should be set **below** the absolute maximum expected discharge current. It must be set **low** enough that unexpected mild discharge spikes or inaccuracies do not create a false over current trigger, but **high** enough to force the Discharge FET open before damage occurs to the pack.

OC (1st Tier) Time Dsg

See *OC(1st Tier) Dsg*. This is a buffer time allotted for a 1st tier Over Current in the discharge direction condition. The timer starts every time [OCD] in ***Safety Alert*** is initially set. When the timer expires, the bq20z90 forces an [OCD] Alarm in ***Safety Status*** and opens the Discharge FET. If [OCD] in Safety Alert clears prior to the expiration of the *OC (1st Tier) Time Dsg* timer, then the [OCD] in ***Safety Alert*** is cleared and the *OC (1st Tier) Time Dsg* timer resets. Setting the *OC (1st Tier) Time Dsg* to 0 disables *OC (1st Tier) Dsg*.

Normal Setting: This is normally set to 2 seconds, but depends on the application. It should be set long enough to prevent false triggering of the [OCD] in *Safety Status*, but short enough to prevent damage to the battery pack.

OC Dsg Recovery

OC Dsg Recovery is one of several recovery methods used for both 1st and 2nd level Over Current in the discharge direction Faults. This value is used for either nonremovable packs ([NR] in *Operation Cfg B = 1*) or for removable packs configured ([OCD] in *Non-Removable Cfg*). With either of these settings, ***Average Current*** must rise **above** this value for *Current Recovery Timer* in seconds to clear the [OCD] or the [OCD2] in ***Safety Status*** if either is set.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent but is normally set **high** enough that it prevents quick oscillation in the Discharge FET. ***Average Current*** is used for this recovery function and moves closer to 0 every second that it is recomputed with *Current* at or near 0. If this recovery is set too **low**, then the Discharge FET can oscillate with a frequency that is fast enough to cause damage to the battery pack because the ***Average Current*** moves **above** this value quickly.

OC (2nd Tier) Chg

When current measured by ***Current*** reaches up to or above this threshold during charging then the 2nd Tier Over Current in Charge [OCC2] protection process is triggered, initiating an [OCC2] in ***Safety Alert*** for *OC (2nd Tier) Chg Time* in seconds. If the 2nd Tier Over Current condition clears prior to the expiration of the *OC (2nd Tier) Chg Time* timer, then [OCC2] in ***Safety Alert*** is cleared and no [OCC2] is set in ***Safety Status***. If the 2nd Tier Over Current condition does not clear, then a [OCC2] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.

Normal Setting: This register is application dependent. It should be set above the *OC (1st Tier) Chg* threshold and should be set high enough that unexpected mild charge spikes or inaccuracies do not create a false over current trigger, but low enough to force the Charge FET to open before damage occurs to the pack.

OC (2nd Tier) Time Chg

See *OC(2nd Tier) Chg*. This is a buffer time allotted for a 2nd Tier Over Current condition. The timer starts every time the [OCC2] is ***Safety Alert*** is initially set. When the timer expires then, the bq20z90 forces an [OCC2] in ***Safety Status*** and opens the Charge FET. If [OCC2] in ***Safety Alert*** clears prior to the expiration of the *OC (2nd Tier) Chg Time* timer, then [OCC2] in ***Safety Alert*** is cleared and the *OC (2nd Tier) Chg Time* timer resets. Setting the *OC (2nd Tier) Chg Time* to 0 disables *OC (2nd Tier) Chg*.

Normal Setting: This is normally set to 2 seconds, but depends on the application. It must be set long enough to prevent false triggering of the [OCC2] in ***Safety Status***, but short enough to prevent damage to the battery pack. It is common for the second level over current threshold to be disabled.

OC (2nd Tier) Dsg

When current measured by ***Current*** falls down to or below this threshold during discharging, then the 2nd Tier Over Current in discharge (OCD2) protection process is triggered, initiating an [OCD2] in ***Safety Alert*** for *OC (2nd Tier) Dsg Time* in seconds. If the 2nd Tier OCD2 condition clears prior to the expiration of the *OC (2ndTier) Dsg Time* timer, then the [OCD2] is cleared in ***Safety Alert*** and no [OCD2] alarm is set in ***Safety Status***. If the 2nd Tier OCD condition does not clear, then a [OCD2] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [XDSG] and [XDSGI] in ***Operation Status*** to be set. It also causes ***Charging Current*** to be set to 0.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent. It should be set **below** the *OC (1st Tier) Dsg* threshold and must be set **below** the absolute maximum expected discharge current. It must be set **low** enough that unexpected mild discharge spikes or inaccuracies do not create a false over current trigger, but **high** enough to force the Discharge FET open before damage occurs to the pack.

OC (2nd Tier) Time Dsg

See *OC (2nd Tier) Dsg*. This is a buffer time allotted for a 2nd Tier Over Current in the discharge direction condition. The timer starts every time [OCD2] in ***Safety Alert*** is initially set. When the timer expires, then the bq20z90 forces an [OCD2] alarm in *Safety Status* and opens the Discharge FET. If [OCD2] in ***Safety Alert*** clears prior to the expiration of the *OC (2nd Tier) Time Dsg* timer, then the [OCD] in ***Safety Alert*** is cleared and the *OC (2nd Tier) Time Dsg* timer resets. Setting the *OC (2nd Tier) Time Dsg* to 0 disables *OC (2nd Tier) Dsg*.

Normal Setting: This is normally set to 2 seconds but depends on the application. It must be set long enough to prevent false triggering of the [OCD2] in ***Safety Status***, but short enough to prevent damage to the battery pack.

Current Recovery Timer

The *Current Recovery Timer* is used in the recovery process of any of the over current fault conditions. After a fault condition exists, depending on if enabled, the fault condition is cleared only after *Current Recovery Timer* time in seconds with ***AverageCurrent*** falling below the corresponding recovery threshold in the charge direction or rising above the corresponding recovery threshold in the discharge direction. The corresponding recovery does not happen immediately after the recovery condition exits. As soon as the recovery condition exists then the *Current Recovery Timer* starts and the condition clears and the corresponding FET is enabled after the *Current Recovery Timer* expires. This timer is associated with the following Fault Conditions as described in this section:

1. *OC (1st Tier) Dsg*
2. *OC (1st Tier) Chg*
3. *OC (2nd Tier) Dsg*
4. *OC (2nd Tier) Chg*
5. *AFE OC Dsg*
6. *AFE SC Dsg*
7. *AFE SC Chg*

This Recovery method is enabled if [NR] is set in *Operation Cfg B*, or if ([NR] is cleared, and the corresponding bits are set in the *Non-Removable Cfg* register:

1. *OC (1st Tier) Dsg* [OCD]
2. *OC (1st Tier) Chg* [OCC]
3. *OC (2nd Tier) Dsg* [OCD2]
4. *OC (2nd Tier) Chg* [OCC2]
5. *AFE OC Dsg* [AOCD]
6. *AFE SC Dsg* [SCD]
7. *AFE SC Chg* [SCC]

Normal Setting: The default for this register is 8 seconds. This is a recommended number to prevent heating up in the corresponding FET.

AFE OC Dsg

See the important note about all AFE fault conditions at the beginning of the **Current** section.

This is the third level Over Current protection in the discharge direction. This is a last effort protection function before using the Permanent Fail Functions in the Second Level Safety Class. This register displays in HEX using the EV Software. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If the *AFE OC DSG* condition exists for *AFE OC Dsg Time* in milliseconds, then the discharge FET opens as controlled by the bq29330. This fault condition causes [AOCD] to be set in ***Safety Status*** and [XDSG], [XDSGI] is set in *Operation Status*, and [TDA] is set in ***Battery Status***. It also causes ***Charging Current*** to be set to 0. See Table 10 for settings for this register.

Table 10. AFE OC Dsg Configuration

0X00	**0.050 V**	**0x08**	**0.090 V**	**0x10**	**0.130 V**	**0x18**	**0.170 V**
0x01	**0.055 V**	**0x09**	**0.095 V**	**0x11**	**0.135 V**	**0x19**	**0.175 V**
0x02	**0.060 V**	**0x0a**	**0.100 V**	**0x12**	**0.140 V**	**0x1a**	**0.180 V**
0x03	**0.065 V**	**0x0b**	**0.105 V**	**0x13**	**0.145 V**	**0x1b**	**0.185 V**
0x04	**0.070 V**	**0x0c**	**0.110 V**	**0x14**	**0.150 V**	**0x1c**	**0.190 V**
0x05	**0.075 V**	**0x0d**	**0.115 V**	**0x15**	**0.155 V**	**0x1d**	**0.195 V**
0x06	**0.080 V**	**0x0e**	**0.120 V**	**0x16**	**0.160 V**	**0x1e**	**0.200 V**
0x07	**0.085 V**	**0x0f**	**0.125 V**	**0x17**	**0.165 V**	**0x1f**	**0.205 V**

Normal Setting: Note that the maximum value for this register is 0x1F. Values above 0x1F cause unpredictable results. This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is **below** the *OC (2nd Tier) Dsg*.

AFE OC Dsg Time

This is the time after detection of an *AFE OC Dsg* fault before the Discharge FET attempts to open. This trigger function is completely controlled by the bq29330. The setting of this register is in HEX, and it is in milliseconds (See *AFE OC Dsg*). See Table 11 for setting for this register.

Table 11. AFE OC Dsg Time Configuration

0x00	**1 ms**	**0x04**	**9 ms**	**0x08**	**17 ms**	**0x0c**	**25 ms**
0x01	**3 ms**	**0x05**	**11 ms**	**0x09**	**19 ms**	**0x0d**	**27 ms**
0x02	**5 ms**	**0x06**	**13 ms**	**0x0a**	**21 ms**	**0x0e**	**29 ms**
0x03	**7 ms**	**0x07**	**15 ms**	**0x0b**	**23 ms**	**0x0f**	**31 ms**

Normal Setting: Note that the maximum value for this register is 0x0F. Values above 0x0F cause unpredictable results. This register is completely application specific. It should be set long enough to prevent false triggering of the [AOCD] in ***Safety Status***, but short enough to prevent damage to the battery pack.

AFE OC Dsg Recovery

See the important note about all AFE fault conditions at the beginning of the **Current** section.

AFE OC Dsg Recovery is one of several recovery methods used for *AFE OC Dsg Fault*. This value is used for either nonremovable packs ([NR] in *Operation Cfg B =1*) or for removable packs configured ([AOCD] in *Non-Removable Cfg*). With either of these settings, ***AverageCurrent*** must rise **above** this value for *Current Recovery Timer* in seconds to clear the [AOCD] in ***Safety Status*** if it is set.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent, but is normally set **high** enough that it prevents quick oscillation in the Discharge FET. If set to **low**, then the Discharge FET can oscillate with a frequency that is fast enough to still cause damage to the battery pack because the ***AverageCurrent*** moves **above** this value quickly.

AFE SC Chg Cfg

See the **NOTE** at the beginning of the Current section for an important note about all AFE fault conditions.

This register includes 2 settings. The setting are refered to as *AFE SC Chg* and *AFE SC Chg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4-7) sets the time for the AFE short circuit in the Charge direction fault detection time (*AFE SC Chg Time*). The least significant nibble (bits 0–3) set the threshold at which the bq29330 detects a AFE short circuit fault (*AFE SC Chg*). This is an extreme condition with settings for very large voltages and very short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Charge FET opens as controlled by the bq29330. This fault condition causes [SCC] to be set in ***Safety Status***, and [TCA] to be set in ***Battery Status***. It also causes ***Charging Current*** and ***Charging*** Voltage to be set to 0. See Table 13 for settings for this register.

Table 12. AFE SC Chg Cfg Bit Description

7	6	5	4	3	2	1	0
SCCT3	SCCT2	SCCT1	SCCT0	SCCV3	SCCV2	SCCV1	SCCV0
AFE SC Chg Time				*AFE SC Chg*			

Table 13. AFE SC Chg Cfg Least Significant Nibble (SCCV3-SCCV0)

0x00	**0.100 V**	**0x04**	**0.200 V**	**0x08**	**0.300 V**	**0x0c**	**0.400 V**
0x01	**0.125 V**	**0x05**	**0.225 V**	**0x09**	**0.325 V**	**0x0d**	**0.425 V**
0x02	**0.150 V**	**0x06**	**0.250 V**	**0x0a**	**0.350 V**	**0x0e**	**0.450 V**
0x03	**0.175 V**	**0x07**	**0.275 V**	**0x0b**	**0.375 V**	**0x0f**	**0.475 V**

Table 14. AFE SC Chg Cfg Most Significant Nibble (SCCT3-SCCT0)

0x00	**0 μs**	**0x04**	**244 μs**	**0x08**	**488 μs**	**0x0c**	**732 μs**
0x01	**61 μs**	**0x05**	**305 μs**	**0x09**	**549 μs**	**0x0d**	**793 μs**
0x02	**122 μs**	**0x06**	**366 μs**	**0x0a**	**610 μs**	**0x0e**	**854 μs**
0x03	**183 μs**	**0x07**	**427 μs**	**0x0b**	**671 μs**	**0x0f**	**915 μs**

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is sufficiently above *OC (2nd Tier) Chg*.

AFE SC Dsg Config

See the important note about all AFE fault conditions at the beginning of the Current section.

This register includes 2 settings. Refer to these as *AFE SC Dsg* and *AFE SC Dsg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4–7) sets the time for the AFE short circuit in the discharge direction fault detection time (*AFE SC Dsg Time*). The least significant nibble (bits 0–3) sets the threshold at which the bq29330 detects an AFE short circuit fault in the discharge direction (*AFE SC Dsg*). This is an extreme condition with settings for large voltages and short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Discharge FET opens as controlled by the bq29330. This fault condition causes [SCD] to be set in ***Safety Status***, [XDSG] and [XDSGI] to be set in ***Operation Status***, and [TDA] to be set in ***Battery Status***. See Table 16 and Table 17 for settings for this register.

Table 15. AFE SC Dsg Cfg Bit Description

7	6	5	4	3	2	1	0
SCDT3	SCDT2	SCDT1	SCDT0	SCDV3	SCDV2	SCDV1	SCDV0
AFE SC Dsg Time				*AFE SC Dsg*			

Table 16. AFE SC Dsg Cfg Least Significant Nibble (SCDV3-SCDV0)

0x00	**0.10 V**	**0x04**	**0.20 V**	**0x08**	**0.30 V**	**0x0c**	**0.40 V**
0x01	**0.125 V**	**0x05**	**0.225 V**	**0x09**	**0.325 V**	**0x0d**	**0.425 V**
0x02	**0.150 V**	**0x06**	**0.250 V**	**0x0a**	**0.350 V**	**0x0e**	**0.450 V**
0x03	**0.175 V**	**0x07**	**0.275 V**	**0x0b**	**0.375 V**	**0x0f**	**0.475 V**

Table 17. AFE SC Dsg Cfg Most Significant Nibble (SCDT3-SCDT0)

0x00	**0 μs**	**0x04**	**244 μs**	**0x08**	**488 μs**	**0x0c**	**732 μs**
0x01	**61 μs**	**0x05**	**305 μs**	**0x09**	**549 μs**	**0x0d**	**793 μs**
0x02	**122 μs**	**0x06**	**366 μs**	**0x0a**	**610 μs**	**0x0e**	**854 μs**
0x03	**183 μs**	**0x07**	**427 μs**	**0x0b**	**671 μs**	**0x0f**	**915 μs**

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required to determine the proper setting for this register. Be sure that this value is **below** AFE OC Dsg.

AFE SC Recovery

See the important note about all AFE fault conditions at the beginning of the **Current** section.

AFE SC Recovery is one of several recovery methods used for either a charge or discharge AFE short circuit fault. This value is used for either nonremovable packs ([NR] in *Operation Cfg B =1*) or for removable packs that this function is configured ([SCD] for discharge or [SCC] in charge in *Non-Removable Cfg*). With either of these settings, *AverageCurrent* must rise **above** this value (for discharge fault) or **below** this value (for charge fault) for *Current Recovery Timer* in seconds to clear the [SCD] or [SCC] in *Safety Status* if either is set.

Normal Setting: Care must be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent, but is normally set close to 0 mA to prevent quick oscillation in the Charge/Discharge FET. If it is set to far from 0 mA, then the Charge/Discharge FET oscillates with a frequency that is fast enough to cause damage to the battery pack because the ***AverageCurrent*** is within this threshold value too quickly.

Temperature

Over Temp Chg

When the pack temperature measured by ***Temperature*** rises to or above this threshold while charging (***Current***> *Chg Current Threshold*), then the Over Temperature in charge direction (OTC) protection process is triggered and [OTC] is set in ***Safety Alert*** for *OT Chg Time*. If the OTC condition clears prior to the expiration of the *OT Chg Time* timer, then the [OTC] is cleared in ***Safety Alert*** and no [OTC] is set in ***Safety Status***. If the condition does not clear, then [OTC] is set in ***Safety Status*** and if [OTFET] is set in *Operation Cfg B* the Charge FET is opened. If [OTFET] is not set in *Operation Cfg B*, then the Charge FET is not opened by this fault. This fault condition causes [TCA] and [OTA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging, and verify these setting are sufficient for the application temperature. The default is 55°C which should be sufficient for most Li-Ion applications.

OT Chg Time

See *Over Temp Chg*. This is a buffer time allotted for Over Temperature in the charge direction condition. The timer starts every time the [OTC] in ***Safety Alert*** is initially set. When the timer expires, the bq20z90 forces an [OTC] in ***Safety Status*** and opens the Charge FET if enabled with [OTFET] in *Operation Cfg B*. If [OTC] in ***Safety Alert*** clears (fault condition clears) prior to the expiration of the *OT Chg Time* timer, then [OTC] in ***Safety Alert*** is cleared and the *OT Chg Time* timer resets. Setting the *OT Chg Time* to 0 disables this function.

Normal Setting: This is normally set to 2 seconds which should be sufficient for most applications. Temperature is normally a slow acting condition that does not need high speed triggering. It must be set long enough to prevent false triggering of the [OTC] in ***Safety Status***, but short enough to prevent damage to the battery pack.

OT Chg Recovery

OT Chg Recovery is the temperature at which the battery recovers from an *OT Temp Chg* fault. This is the only recovery method for an *OT Temp Chg* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Charge FET if it was opened with the fault. The default is 50°C which is a 5 degree difference which is sufficient to protect against oscillation during the transition between conditions.

Over Temp Dsg

When the pack temperature measured by ***Temperature*** rises to or above this threshold while discharging (***Current*** <(-)(*Dsg Current Threshold*)), then the Over Temperature in discharge direction (OTD) protection process is triggered and [OTD] is set in ***Safety Alert*** for *OT Dsg Time*. If the OTD condition clears prior to the expiration of the *OT Dsg Time* timer, then the [OTD] is cleared in ***Safety Alert*** and no [OTD] is set in ***Safety Status***. If the condition does not clear, then [OTD] is set in ***Safety Status*** and if [OTFET] is set in *Operation Cfg B* the Discharge FET is opened. If [OTFET] is not set in *Operation Cfg B* then the Discharge FET is not opened by this fault. This fault condition causes [TDA] and [OTA] in ***Battery Status*** to be set. It also causes ***Charging Current*** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 60°C which is sufficient for most Li-Ion applications. The default *Over Temp Dsg* setting is higher than the default *Over Temp Chg* because Li-Ion can handle a higher temperature in the discharge direction than in the charge direction.

OT Dsg Time

See *Over Temp Dsg*. This is a buffer time allotted for Over Temperature in the discharge direction condition. The timer starts every time the [OTD] in ***Safety Alert*** is initially set. When the timer expires, then the bq20z90 forces an [OTD] in ***Safety Status*** and opens the Discharge FET if enabled with [OTFET] in Operation Cfg B. If [OTD] in ***Safety Alert*** clears (fault condition clears) prior to the expiration of the *OT Dsg Time* timer, then [OTD] in ***Safety Alert*** is cleared and the *OT Dsg Time* timer resets. Setting the *OT Chg Time* to 0 disables this function.

Normal Setting: This is normally set to 2 seconds which is sufficient for most applications. Temperature is normally a slow acting condition that does not need high speed triggering. It should be set long enough to prevent false triggering of the [OTD] in ***Safety Status***, but short enough to prevent damage to the battery pack.

OT Dsg Recovery

OT Dsg Recovery is the temperature at which the battery recovers from an *OT Temp Dsg* fault. This is the only recovery method for an *OT Temp Dsg* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Discharge FET if it was opened with the fault. The default is 55°C which is a 5 degrees difference which is sufficient to protect against this oscillation during the transition between conditions.

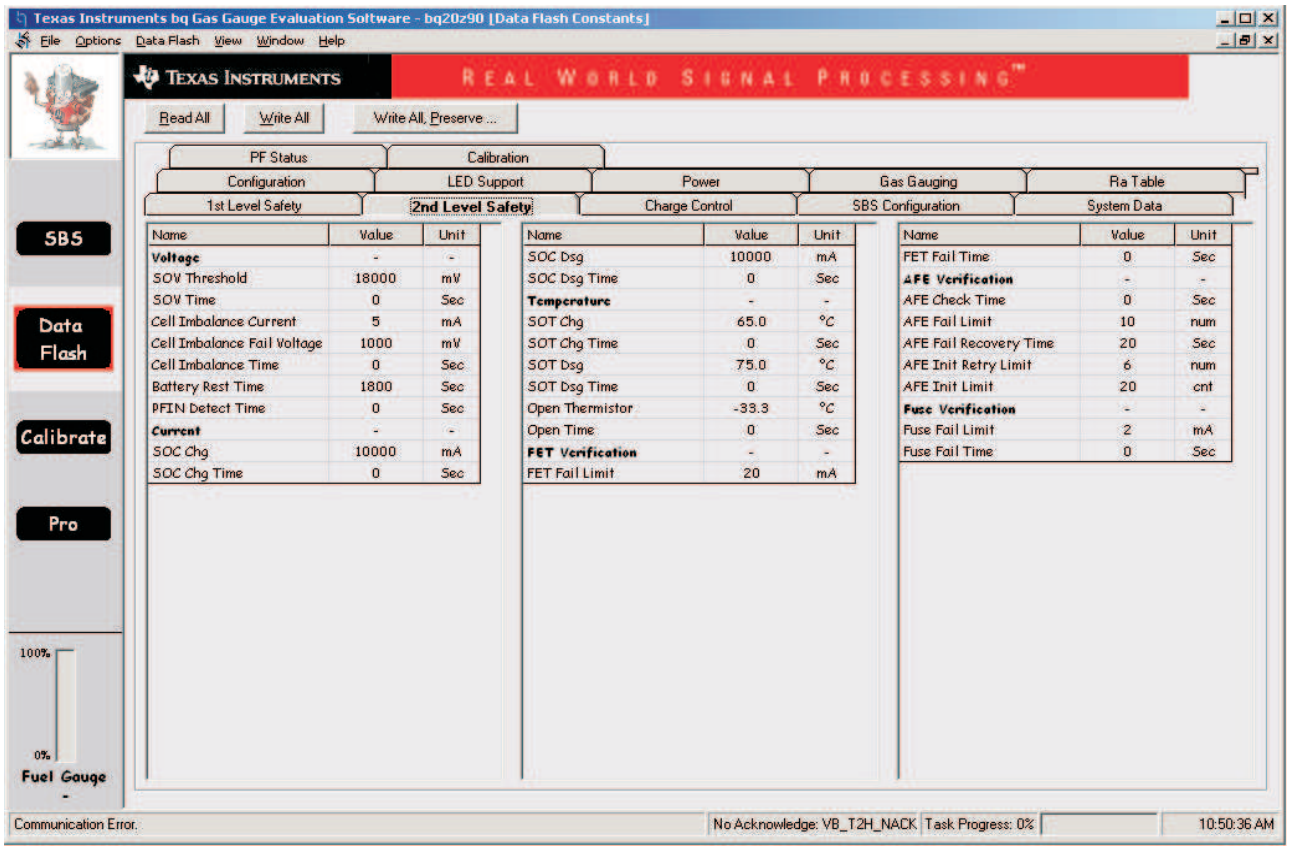
Host Comm

Host Watchdog Timeout

This function is only active when the bq20z90 is in Normal Power Mode (not asleep or in shutdown mode). It is also disabled if set to 0. If there is no communication to the bq20z90 via the SMBus for *Host Watchdog Timeout* time in seconds, then the bq20z90 reports [HWDG] set in ***Safety Status*** and opens the Charge, Discharge, and Pre-Charge FETs if enabled. This fault causes [TCA] and [TDA] in ***Battery Status*** to be set., and [XDSG] in ***Operation Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. It is difficult to monitor this function because any SMBus communication clears the fault condition. To monitor the function using SMBus, then the SMBus command that is used to clear the fault condition must be an SMBus read of ***Safety Status***. The [HWDG] flag is set on this read. Then on the next read (if its within the *Host Watchdog Timeout* window) the [HWDG] flag is cleared. The [HWDG] flag in ***Safety Alert*** as displayed in the EV Software is not used in this algorithm, and serves no purpose.

Normal Setting: This is not a common function and its default setting is 0. This provides another method for turning off the FETs, and preventing charge or discharge because the corresponding FETs are turned off when the fault occurs. It is also important to note that if the *Host Watchdog Timeout* is less than the *Bus Low Time*, then the fault condition occurs prior to the *Bus Low Timeout* which normally occurs prior to going to sleep. This function is disabled when in sleep mode, and the bq20z90 detects going to sleep mode as soon as the *Bus Low Timeout* expires. So, if the *Host Watchdog Timeout* timer expires prior to detecting bus low, then it triggers this fault.

2.3 2nd Level Safety



Voltage

SOV Threshold

This is a final level of protection. It is permanent. When the pack voltage measured by ***Voltage*** rises to this threshold, then the Safety Over Voltage (SOV) protection process is triggered. This process starts by setting [SOV] in ***PF Alert*** for *SOV Time*. If the SOV condition clears prior to the expiration of the *SOV Time* timer, then the [SOV] is cleared in ***PF Alert***, and no [SOV] is set in ***PF Status***. If the SOV condition does not clear, then [SOV] is set in ***PF Status***. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOV] in *Permanent Fail Cfg*, then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a voltage above the POV Threshold. This is meant to be a permanent condition, and it is recommended that [XSOV] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOV Time

See *SOV Threshold*. This is a buffer time allotted for an SOV condition. The timer starts after [SOV] is set in ***PF Alert***. When it expires, then the bq20z90 forces an [SOV] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOV Time* timer, then [SOV] is cleared in ***PF Alert***, and the *SOV Time* timer resets without setting [SOV] in ***PF Status***. If *SOV Time* is 0, then the *SOV Threshold* function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended . The most common values for this register are between 2–5 seconds.

Cell Imbalance Current

This is part of the safety cell imbalance detection algorithm. There are 4 registers that go together to make up this algorithm. *Cell Imbalance Current* is the value that ***Current*** must be below for the entire *Battery Rest Time* before Cell Imbalance detection is enabled. The bq20z90 does not start detecting a cell imbalance for this safety algorithm until the battery ***Current*** has been below this ***Cell Imbalance Current*** for at least the *Battery Rest Time*.

Normal Setting: This register should be set low to ensure the battery is completely relaxed when this algorithm is enabled. This Safety algorithm if triggered is permanent, and renders the battery useless. It is imperative that all data is valid prior to activation. The default setting is 5 mA which is sufficient for most applications.

Cell Imbalance Fail Voltage

This is part of the safety cell imbalance detection algorithm. For the purpose of this description:

Cell Voltage H = the highest SBS cell voltage

Cell Voltage L = the lowest SBS cell voltage

Delta Cell Voltage = ***Cell Voltage H***–***Cell Voltage L***

There are 4 registers that go together to make up this algorithm. After the *Battery Rest Time* portion of the Cell Imbalance algorithm has passed the test criteria (see *Battery Rest Time* and *Cell Imbalance Current*), then if ***Delta Cell Voltage*** is greater than the *Cell Imbalance Fail Voltage* in millivolts, then the *Cell Imbalance Fail Voltage* protection process is triggered. This process starts by setting [CIM] in ***PF Alert*** for *Cell Imbalance Time*. If the cell imbalance condition clears prior to the expiration of the *Cell Imbalance Time* timer, then the [CIM] is cleared in ***PF Alert*** with no [CIM] being set in ***PF Status***. If the cell imbalance condition does not clear, then [CIM] is set in ***PF Status***. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XCIM] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a voltage high enough to prevent any possibility of false triggering because this application is irreversible. This is meant to be a permanent condition and it is recommended that [XCIM] be set in Permanent Fail Cfg with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

Cell Imbalance Time

See *Cell Imbalance Fail Voltage*. This is a buffer time allotted for a cell imbalance safety condition. The timer starts after the *Battery Rest Time* has expired with current below the *Cell Imbalance Current* and ***Delta Cell Voltage*** (see *Cell Imbalance Fail Voltage*) is above the *Cell Imbalance Fail Voltage*. When the *Cell Imbalance Time* timer starts [CIM] is set in ***PF Alert***. When the timer expires, then the bq20z90 forces a [CIM] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Cell Imbalance Time* timer, then [CIM] is cleared in ***PF Alert***, and the *Cell Imbalance Time* timer resets without setting [CIM] in ***PF Status***. The *Cell Imbalance Fail Voltage* function is disabled with *Cell Imbalance Time* equal to 0 or *Battery Rest Time* set to 0.

Normal Setting: This register defaults to 0. This disables the function. It is recommended that this function be enabled and the [XCIM] be enabled in *Permanent Failure Cfg* to protect against a potentially dangerous condition. *Battery Rest Time* helps prevent false triggering of this condition, so a good setting for Cell imbalance Time is 5 seconds. This gives several readings to ensure that the condition does exist.

Battery Rest Time

See *Cell Imbalance Current*. *Battery Rest Time* is the time in seconds that the battery ***Current*** must be below the *Cell Imbalance Current* for before Cell Imbalance detection is enabled. The bq20z90 does not start detecting a cell imbalance for this safety algorithm until the battery ***Current*** has been below *Cell Imbalance Current* for at least the *Battery Rest Time*. The *Cell Imbalance Fail Voltage* function is disabled with *Cell Imbalance Time* equal to 0 or *Battery Rest Time* set to 0.

Normal Setting: This register should be set for a relatively long time period to ensure the battery is completely relaxed when this algorithm is enabled. This safety algorithm, if triggered, is permanent and renders the battery useless. It is imperative that all data is valid prior to activation. The default setting is 1800 seconds which is sufficient for most applications.

PFIN Detect Time

This is a buffer time allotted for an $\overline{\text{PFIN}}$ safety condition. The timer *PFIN Detect Time* timer starts after the $\overline{\text{PFIN}}$ input pin has been set logic low by some external device (normally an external protector) which forces the [PFIN] is set in ***PF Alert***. When it expires, then the bq20z90 forces an [PFIN] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *PFIN Detect Time* timer, then [PFIN] is cleared in ***PF Alert***, and the *PFIN Detect Time* timer resets without setting [PFIN] in ***PF Status***. If *PFIN Detect Time* is 0, then this function is disabled. This fault condition triggers many permanent protection features as listed here:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XPFIN] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: If this fault condition occurs then it is because an external device has already triggered a fault that should be nonrecoverable. This is meant to be a permanent condition, and it is recommended that [XPFIN] be set in *Permanent Fail Cfg*. If a fault occurs, and the external device sets the $\overline{\text{PFIN}}$ input low, the fuse will blow. If the fuse does not blow, then the bq20z90 attempts to blow the fuse (SAFE pin is set high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90). There is a clear function for this condition, but it is only intended to be used during the development process. The default for this function is 0. If the $\overline{\text{PFIN}}$ input is not used, then this function should be disabled. It is recommended that this function be used, and that [XPFIN] be set to ensure safe operation.

Current

SOC Chg

SOC Chg is a final level of current protection from the bq20z90. This is not related to the 3rd level (AFE) protection which is a fast acting protection. It is also intended to be permanent. When the charge current as measured by ***Current*** rises to or above this threshold, then the Safety Over Current in the Charge direction (SOCC) protection process is triggered. This process starts by setting [SOCC] in ***PF Alert*** for *SOC Chg Time*. If the SOCC condition clears prior to the expiration of the *SOC Chg Time* timer, then the [SOCC] is cleared in ***PF Alert*** and with no [SOCC] being set in ***PF Status***. If the SOC condition does not clear, then [SOCC] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET ware all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. If [XSOCC] in *Permanent Fail Cfg*, then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins is activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and should be set to a current above *OC(2nd Tier) Chg*. It is not necessarily required to set above *AFE OC Chg* which is a fast acting fault condition meant for high current spike detection. This function is meant to be a permanent condition, and it is recommended that [XSOCC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Chg Time

See *SOC Chg*. This is a buffer time allotted for an SOCC condition. The timer starts after [SOCC] is set in ***PF Alert***. When it expires, then the bq20z90 forces an [SOCC] in ***PF Status***, and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Chg Time* timer, then [SOCC] is cleared in ***PF Alert***, and the *SOC Chg Time* timer resets without setting [SOCC] in ***PF Status***. If *SOC Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2-5 seconds.

SOC Dsg

SOC Dsg is a final level of current protection from the bq20z90. This is not related to the 3rd level (AFE) protection which is a fast acting protection. It is also intended to be permanent. When the discharge current as measured by ***Current*** falls **down** to or **below** a negative of this threshold (–(*SOC Dsg*)), then the Safety Over Current in the discharge direction (SOCD) protection process is triggered. This process starts by setting [SOCD] in ***PF Alert*** for *SOC Dsg Time*. If the SOCC condition clears prior to the expiration of the *SOC Dsg Time* timer, then the [SOCD] is cleared in ***PF Alert*** with no [SOCC] being set in ***PF Status***. If the SOC condition does not clear, then [SOCD] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOCD] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: Care must taken when interpreting discharge descriptions in this document when

interpreting the direction and magnitude of the currents because they are in the negative direction. This is the last level of protection and must be set to a current below *OC(2nd Tier) Dsg*. It is not required to set above *AFE OC Dsg* which is a fast acting fault condition meant for high current spike detection. This is meant to be a permanent condition and it is recommended that [XSOCD] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Dsg Time

See *SOC Dsg*. This is a buffer time allotted for an SOCD condition. The timer starts after [SOCD] is set in ***PF Alert***. When it expires, then the bq20z90 forces an [SOCD] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Dsg Time* timer, then [SOCD] is cleared in ***PF Alert***, and the *SOC Dsg Time* timer resets without setting [SOCD] in ***PF Status***. If *SOC Dsg Time* is 0, then this function is disabled.
Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

Temperature

SOT Chg

SOT Chg is a final level of temperature protection from the bq20z90. This fault condition is intended to be permanent. When the temperature as measured by ***Temperature*** rises to or above this threshold while charging ([DSG] cleared in ***Battery Status***), then the Safety Over Temperature in the Charge direction (SOTC) protection process is triggered. This process starts by setting [SOTC] in ***PF Alert*** for *SOT Chg Time*. If the SOTC condition clears prior to the expiration of the *SOT Chg Time* timer, then the [SOTC] is cleared in ***PF Alert*** and with no [SOTC] being set in ***PF Status***. If the SOT condition does not clear, then [SOTC] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET ware all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOTC] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a temperature above *Over Temp Chg*. This is meant to be a permanent condition and it is recommended that [XSOTC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOT Chg Time

See *SOT Chg*. This is a buffer time allotted for a Safety Over Temperature Condition. The timer starts after [SOTC] is set in ***PF Alert***. When it expires, then the bq20z90 forces an [SOTC] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOT Chg Time* timer, then [SOTC] is cleared in ***PF Alert***, and the *SOT Chg Time* timer resets without setting [SOTC] in **PF Status**. If *SOT Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

SOT Dsg

SOT Dsg is a final level of temperature protection from the bq20z90. This fault condition is intended to be permanent. When the temperature as measured by ***Temperature*** rises to or above this threshold while discharging ([DSG] set in ***Battery Status***), then the Safety Over Temperature in the discharge direction (SOTD) protection process is triggered. This process starts by setting [SOTD] in ***PF Alert*** for SOT Dsg Time. If the SOTD condition clears prior to the expiration of the *SOT Dsg Time* timer, then the [SOTD] is cleared in ***PF Alert*** and with no [SOTD] being set in ***PF Status***. If the SOT condition does not clear, then [SOTD] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all be opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOTD] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a temperature above *Over Temp Chg*. This is meant to be a permanent condition, and it is recommended that [XSOTC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOT Dsg Time

See *SOT Dsg*. This is a buffer time allotted for a Safety Over Temperature Condition. The timer starts after [SOTD] is set in ***PF Alert***. When it expires, then the bq20z90 forces an [SOTD] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOT Dsg Time* timer, then [SOTD] is cleared in ***PF Alert***, and the *SOT Dsg Time* timer resets without setting [SOTD] in ***PF Status***. If *SOT Dsg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

Open Thermistor

Setting *Open Thermistor Time* to 0 disables this function. The *Open Thermistor* register is part of a thermistor circuit fault protection algorithm in the bq20z90 that detects an open circuit in the thermistor circuit because ***Temperature*** reaches impossible values due to open circuit ADC readings. This fault condition is intended to be permanent. When the temperature as measured by ***Temperature*** falls to or below this threshold, then the Open Thermistor protection process is triggered. This process starts by setting [OTS] in ***PF Alert*** for *Open Thermistor Time*. If the OTS condition clears prior to the expiration of the Open Thermistor Time timer, then the [OTS] is cleared in ***PF Alert*** and with no [SOTS] being set in ***PF Status***. If the OTS condition does not clear, then [OTS] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XOTS] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This function is a good safety feature that is particularly useful in detecting

thermistors that have come loose from the Gas Gauge PCB during the assembly process or if the wire of a thermistor comes lose from vibration. The value in this register does not need to be changed. This is meant to be a permanent condition, and it is recommended that [XOTS] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

Open Thermistor Time

See *Open Thermistor*. This is a buffer time allotted for an Open Thermistor Condition. The timer starts after [OTS] is set in ***PF Alert***. When it expires, then the bq20z90 forces [OTS] set in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Open Thermistor Time* timer, then [OTS] is cleared in ***PF Alert***, and the *Open Thermistor Time* timer resets without setting [OTS] in **PF Status**. If *Open Thermistor Time* is 0 then the *Open Thermistor* function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

FET Verification

FET Fail Limit

FET Fail Limit register is part of a FET circuit fault protection algorithm in the bq20z90 that detects potentially hazardous FET circuit damage. This fault condition is intended to be permanent, and has 2 possible trigger functions to help prevent confusion. The functions are listed separately.

1. If the Charge and Pre-Charge FET (if enabled) have been commanded to be off for any reason by either the bq20z90 or the bq29330 (any AFE fault condition) and charge current as measured by ***Current*** still exists which is greater than *FET Fail Limit* in milliamps, then the *FET Fail Limit* protection process is triggered. This process starts by setting [CFETF] in ***PF Alert*** for *FET Fail Time*. If the [CFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then the [CFETF] is cleared in ***PF Alert*** and no [CFETF] is set in ***PF Status***. If the [CFETF] condition does not clear, then [CFETF] is set in ***PF Status***. This triggers many permanent protection features as listed below:
2. If the discharge FET has been commanded to be off for any reason by either the bq20z90 or the bq29330 (any AFE fault condition) and discharge current as measured by ***Current*** still exists which is less than or equal to (–) *FET Fail Limit* in milliamps, then the *FET Fail Limit* protection process is triggered. This process starts by setting [DFETF] in ***PF Alert*** for *FET Fail Time*. If the [DFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then the [DFETF] is cleared in ***PF Alert*** and no [DFETF] is set in ***PF Status***. If the [DFETF] condition does not clear, then [DFETF] is set in ***PF Status***. This triggers many permanent protection features as listed below:

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if A and [XCFETF] or B and [XDFETF] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins is activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: The Charge and Discharge FETs arguably have more stress than any other component on the gas gauge PCB. This function is an excellent safety feature to help protect against the possibility of a shorted FET that is potentially hazardous. The default value in this register must be sufficient for most applications. This is meant to be a permanent condition, and it is recommended that [XCFETF] and [XDFETF] both be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

FET Fail Time

See *FET Fail Limit*. This is a buffer time allotted for the *FET Fail Limit* condition. The timer starts after either [CFETF] or [DFETF] set in ***PF Alert***. When the timer expires, then the bq20z90 forces the associated flag (either [CFETF] or [DFETF]) in ***PF Status*** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *FET Fail Time* timer, then the associated flag (either [CFETF] or [DFETF]) is cleared in ***PF Alert***, and the *FET Fail Time* timer resets without setting the associated flag (either [CFETF] or [DFETF]) in ***PF Status***. If *FET Fail Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

AFE Verification

AFE Check Time

Every *AFE Check Time* in seconds, the bq20z90 reads all the bq29330 registers through the I^2C port that is shared between the 2 parts and compares the static register read results to the AFE data in the bq20z90's Data Flash. If they do not match, then the bq20z90 attempts to repair the corruption. Then increment an internal counter (referred to in this document as AFE_P Fail Counter) which triggers the periodic AFE_P Fail protection process. This process starts by setting [AFE_P] in ***PF Alert***. As long as the AFE_P Fail Counter stays below the *AFE Fail Limit* and above 0, [AFE_P] stays set in ***PF Alert***. See *AFE Recovery Time* for a recovery description. If *AFE Check Time* is set to 0, then the periodic AFE verification (AFE_P) is completely disabled.

Normal Setting: Setting **AFE Check Time** to 0 only disables the AFE_P verification function. It does not disable the AFE_C verification function as described in *AFE Fail Limit*. *AFE Check Time* set to 0 is acceptable because there is still the AFE_C verification process. If, however, AFE Check Time is used, set it above 20 seconds since the periodic test does not need to be done often to ensure the correct function.

AFE Fail Limit

There are 2 AFE safety features that use this register. They is separated here to help prevent confusion.

1. The first safety feature is a continuation of *AFE Check Time*. If the AFE_P Fail Counter (as described above) reaches the *AFE Fail Limit* then [AFE_P] is cleared in ***PF Alert***, and then set in ***PF Status***. Setting *AFE Fail Limit* to 0 does not disable the periodic AFE verification (AFE_P). (See *AFE Check Time*)
2. The second safety feature is not associated with *AFE Check Time*. Anytime a communication with the bq29330 is performed over the I^2C bus that is not part of the periodic check described in *AFE Check Time*, then a different internal counter (referred to in this document as AFE_C Fail Counter) increments. When the AFE_C Fail Counter increments, the AFE_C Fail protection process is triggered. This process starts by setting [AFE_C] in ***PF Alert***. As long as the AFE_C Fail Counter stays below the *AFE Fail Limit* and above 0, then [AFE_C] stays set in ***PF Alert***. See *AFE Recovery Time* for a recovery description. If the AFE_C Fail Counter reaches the *AFE Fail Limit*, then [AFE_C] is cleared in ***PF Alert***, and then set in ***PF Status***. Setting *AFE Fail Limit* to 0 disables the AFE_C Fail protection process.

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if A. [XAFE_P] set or if B and [XAFE_C] set in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the PF Status class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting:*AFE Fail Limit* defaults to 10. It is very important to note that setting *AFE Fail Limit* to 0 only disables the AFE_C functions. AFE_P functions are not disabled with the *AFE Fail Limit* set to 0. This results in [AFE_P] flag getting set in ***PF Status*** on the first failure which is not recommended. The default of 10 is appropriate for most applications. This gives sufficient buffer for ESD, resets and other unknown failures that should be recoverable.

AFE Fail Recovery Time

See *AFE Check Time* and *AFE Fail Limit*. *AFE Fail Recovery Time* function works independently with each of the AFE counters described above (AFE_C Fail Counter and AFE_P Fail Counter). While [AFE_C] or [AFE_P] is set in ***PF_Alert***, every *AFE Fail Recover Time* period in seconds AFE_C Fail Counter and/or AFE_P Fail Counter is decremented by 1 until each reaches 0. As soon as they are decremented back to 0, their associated flags ([AFE_C] or [AFE_P]) are cleared in ***PF Alert***, and the fault process is reversed.

Normal Setting: It is recommended that this register be set less than *AFE Check Time*, so that at least one recovery process can occur between periodic checks.

AFE Init Retry Limit

This description is for reference only. The bq20z90 uses its internal ADC to measure initial AFE (bq29330) offsets and gain values on every reset. The quality of these readings are critical to the accuracy of the voltage as displayed by ***Voltage*** and ***Cell Voltage(All)***. Poor initial offset and gain readings can alter the voltage displayed, and it can take several minutes to reacquire accurate readings due to an internal slow responding digital filter in the bq20z90 firmware. With the importance of the quality of these initial readings, the bq20z90 takes 2 successive readings of these offsets and gain values, and compare them. If the comparison fails to meet the criteria as set by *AFE Init Limit* (see below), then the bq20z90 retries this procedure *AFE Init Retry Limit* times before it forces an AFE_C permanent failure. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOV] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: Modifying this register is not recommended; however, if unexplained AFE_C failures occur after resets, then this might be the function that caused the failure. Increasing this value can help, but the problem is normally a noisy environment due to switching from radio frequencies or PCB layout.

AFE Init Limit

This description is only for reference. This data flash location should never be modified. The bq20z90 uses its internal ADC to measure initial AFE (bq29330) offsets and gain values on every reset. The quality of these readings are critical to the accuracy of the voltage as displayed by ***Voltage*** and ***Cell Voltage(All)***. Poor initial offset and gain readings can alter the voltage displayed, and it can take several minutes to reacquire accurate readings due to an internal slow responding digital filter in the bq20z90 firmware. With the importance of the quality of these initial readings, the bq20z90 takes multiple readings (see *AFE Init Retry Limit* above) of these offsets and gain values, and compare them. The *AFE Init Limit* is the maximum difference in successive respective offset and gain value comparisons allowed for the values to be declared accurate. (Gain reading 2–Gain reading 1) must be below *AFE Init Limit*, (Offset reading 2–Offset reading 1) must be below *AFE Init Limit* etc.

Normal Setting: This register is in a reserved unit format; therefore, it is recommended that this value not be modified. It should be acceptable for most applications except for poor PCB layouts and noisy environments which affect voltage measurements. If this occurs, contact Texas Instruments for the value to put in this register.

Fuse Verification

Fuse Fail Limit register is part of a Fuse circuit fault protection algorithm in the bq20z90 that detects potentially hazardous conditions. The *Fuse Fail Limit* is used in both the charge and the discharge direction. If the *Fuse Flag* has been set to 0x3672 (SAFE pin is set high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90) and the current as measured by ***Current*** still exists which is greater than *Fuse Fail Limit* in milliamps, or less than a (–) *Fuse Fail Limit* then the *Fuse Fail Limit* protection process is triggered. This process starts by setting [FBF] in ***PF Alert*** for *Fuse Fail Time*. If the [FBF] condition clears prior to the expiration of the *Fuse Fail Time* timer, then the [FBF] is cleared in ***PF Alert*** and no [FBF] is set in ***PF Status***. If the [FBF] condition does not clear, then [FBF] is set in ***PF Status***. This causes the normal Permanent Failure conditions except that with this function they are already set. This function only works with an existing permanent failure.

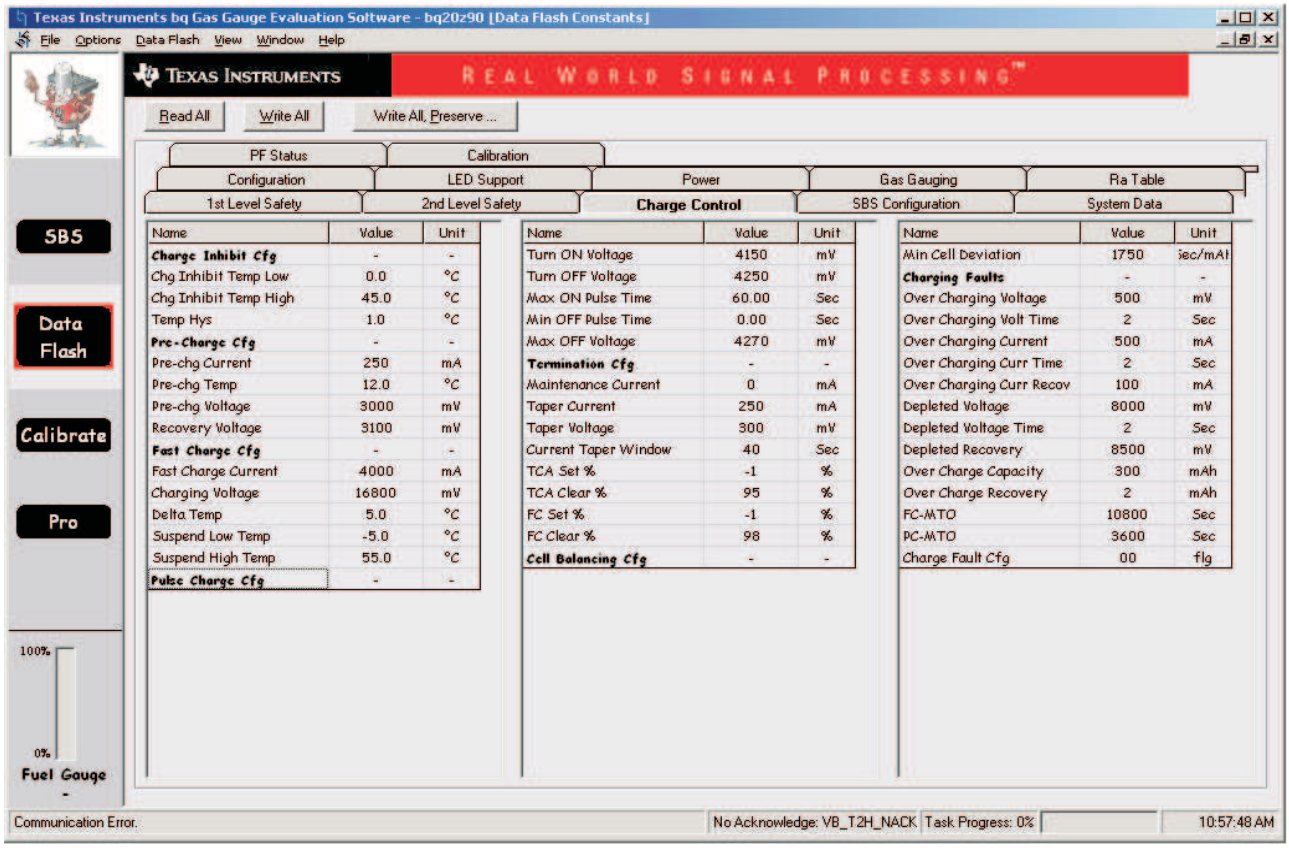
Normal Setting: The purpose of this function is for reporting and retaining the fact that the fuse was supposed to blow but did not. The fact that it causes an [FBF] flag being set in ***PF Status*** serves no purpose except for this fact being recorded for future data retrieval since the fuse was already supposed to be blown. The hope is that the bq20z90 will survive this potentially violent failure enough to be sent to the factory so that the Data Flash that this information was stored in can be read and analyzed to determine the cause of the failure. If the bq20z90 does not survive then this information is useless.

Fuse Fail Time

See *Fuse Fail Limit*. This is a buffer time allotted for the *Fuse Fail Limit* condition. The timer starts after [FBF] is set in ***PF Alert***. When the timer expires, then the bq20z90 forces [FBF] in ***PF Status***. If the condition clears prior to the expiration of the *Fuse Fail Time* timer, then [FBF] is cleared in ***PF Alert*** and the *Fuse Fail Time* timer resets without setting [FBF] in ***PF Status***. If *Fuse Fail Time* is 0, then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. The only purpose of this function is to report that a fuse was instructed to blow and did not. The bq20z90 may not survive to report this information but it is possible. It is an uncommon event unless the fuse blow circuit design is faulty. The most common values for this register are between 2–5 seconds.

2.4 Charge Control



Name	Value	Unit
Charge Inhibit Cfg	-	-
Chg Inhibit Temp Low	0.0	°C
Chg Inhibit Temp High	45.0	°C
Temp Hys	1.0	°C
Pre-Charge Cfg	-	-
Pre-chg Current	250	mA
Pre-chg Temp	12.0	°C
Pre-chg Voltage	3000	mV
Recovery Voltage	3100	mV
Fast Charge Cfg	-	-
Fast Charge Current	4000	mA
Charging Voltage	16800	mV
Delta Temp	5.0	°C
Suspend Low Temp	-5.0	°C
Suspend High Temp	55.0	°C
Pulse Charge Cfg	-	-

Name	Value	Unit
Turn ON Voltage	4150	mV
Turn OFF Voltage	4250	mV
Max ON Pulse Time	60.00	Sec
Min OFF Pulse Time	0.00	Sec
Max OFF Voltage	4270	mV
Termination Cfg	-	-
Maintenance Current	0	mA
Taper Current	250	mA
Taper Voltage	300	mV
Current Taper Window	40	Sec
TCA Set %	-1	%
TCA Clear %	95	%
FC Set %	-1	%
FC Clear %	98	%
Cell Balancing Cfg	-	-

Name	Value	Unit
Min Cell Deviation	1750	sec/mA
Charging Faults	-	-
Over Charging Voltage	500	mV
Over Charging Volt Time	2	Sec
Over Charging Current	500	mA
Over Charging Curr Time	2	Sec
Over Charging Curr Recov	100	mA
Depleted Voltage	8000	mV
Depleted Voltage Time	2	Sec
Depleted Recovery	8500	mV
Over Charge Capacity	300	mAh
Over Charge Recovery	2	mAh
FC-MTO	10800	Sec
PC-MTO	3600	Sec
Charge Fault Cfg	00	flg

Charge Inhibit Config

Chg Inhibit Temp Low

When the pack temperature measured by ***Temperature*** falls to or below this threshold while discharging ([DSG] flag set in ***Battery Status***), the Charge Inhibit Mode is triggered. This causes ***Charging Current*** and ***Charging Voltage*** to be set to 0, [XCHG] is set in ***Charging Status***, and if [CHGIN] set in *Operation Cfg B*, then Charge FET is turned off and/or the Pre-Charge FET is turned off. There are 2 primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** rises above (*Charge Inhibit Temp Low* + *Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated with [DSG] flag set in ***Battery Status***.

With either of these recoveries, [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.

Normal Setting: The purpose of this low inhibit temperature is not to suspend charging, but to prevent it from starting when the conditions are not acceptable, This prevents damage to the pack. The default for this is 0 degrees, and can be modified to fit the application.

Chg Inhibit Temp High

When the pack temperature measured by ***Temperature*** rises to or above this threshold while discharging ([DSG] flag set in ***Battery Status***) the Charge Inhibit Mode is triggered. This causes Charging Current and Charging Voltage to be set to 0, [XCHG] is set in ***Charging Status***, and if [CHGIN] set in *Operation Cfg B* then Charge FET is turned off and/or the Pre-Charge FET is turned off. There are two primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** falls below (*Charge Inhibit Temp Low* – *Temp Hys*).

2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists then, the inhibit mode is reactivated with [DSG] flag set in ***Battery Status***.

With either of these recoveries, [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.

Normal Setting: The purpose of this high inhibit temperature is not to suspend charging but to prevent it from starting when the conditions are not acceptable. This prevents damage to the pack. The default for this is 45°. Notice that this is less than the default charge suspend mode (see *Suspend High Temp*).

Temp Hys

This register works with both *Chg Inhibit High* and *Chg Inhibit Low* in the recovery process.

1. With charge inhibited resulting from a high temperature and if ***Temperature*** falls below (*Charge Inhibit Temp High – Temp Hys*), then the [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.
2. With charge inhibited resulting from low temperature and if ***Temperature*** rises above (*Charge Inhibit Temp Low + Temp Hys*), then the [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.

Normal Setting: this register defaults to 1°C. For most applications, this is considered low for a hysteresis value. This register should be set to at least 2°C to 3°C to prevent oscillation of this condition.

Pre-Charge Config

Pre-Charge Current

This is the current that the bq20z90 reports in the ***Charging Current*** register when the bq20z90 is in Pre-Charge mode (see *Pre-Chg Temperature* and *Pre-Chg Voltage*). This current is broadcast to a smart charger when bq20z90 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Pre-Charge Mode (***Charging Current*** = *Pre-Charge Current*), [PCHG] is set in ***Charging Status***, then the appropriate charging FET is enabled as set with [ZVCHG1] and [ZVCHG0] in *Operation Cfg A*.

Table 9. FET Control Bits in Operation Cfg A

ZVCHG1	ZVCHG0	FET Used
0	0	ZVCHG
0	1	CHG
1	0	OD
1	1	No Action

There are 3 primary recoveries from Pre-Charge mode:

1. Independent of the method (*Pre-Chg Voltage* or *Pre-Chg Temperature*) that caused the Pre-Charge Mode:
   a. ***Cell Voltage (All)*** must be above *Recovery Voltage*
   b. ***Temperature*** must be above (*Pre Chg Temperature + Temp Hys*)

   Either of these conditions cause the bq20z90 to enter Fast Charge Mode (See *Fast Charge Current*)
2. Pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated with any of the Pre-Charge criteria.
3. This is considered a recovery, but it is really a transition from one mode to another. A charge suspend condition (see *Suspend High Temp* and *Suspend Low Temp*) which forces the bq20z90 to transition from Pre-Charge Mode to Charge Suspend Mode.

Normal Setting: This register is application dependent. If a Pre-Charge FET and a current limiting resistor is used to control the current allowed into the battery during Pre-Charge Mode ([ZVCHG1] and [ZVCHG1] both equal 0), then this register accuracy is not as important as if it were used for a smart charger which initiate a current equal to the requested Pre-Charge current. It is important to note that use of the OD pin is not recommended because it does not have limiting circuitry to ensure "hard" on control for a Zero Volt charging condition. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is always recommended.

Pre-Chg Temperature

See *Pre-Charge Current*. With either the *Pre-Chg Voltage* or the *Pre-Chg Temperature* criteria being met, then the bq20z90 triggers Pre-Charge Mode. With ***Temperature*** falling to or below *Pre-Chg Temperature*, but above Charge Inhibit Temp Low, then the bq20z90 enters the Pre-Charge Mode (see *Pre-Charge Current*).

Normal Setting: Ensure that this register is above the *Charge Inhibit Temp Low* . This ensures that *Pre-Chg Temperature* is above the charge suspend temperature because the charge suspend is below the charge inhibit. (See *Charge Inhibit Temp Low* and *Charge Suspend Temp Low*). At cold temperatures, lower currents are better for the battery cells. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Pre-Chg Voltage

See *Pre-Charge Current*. With either the *Pre-Chg Voltage* or the *Pre-Chg Temperature* criteria being met, then the bq20z90 triggers Pre-Charge Mode. With ***Cell Voltage (Any)*** falling to or below *Pre-Chg Voltage*, then the bq20z90 enters Pre-Charge Mode (see *Pre-Charge Current*).

Normal Setting: Ensure that this voltage is set per the battery cell specifications. Setting this value too high is not harmful (except for slower charging from empty), but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage which brings them up to a normal charging voltage before hitting them with a fast current. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Recovery Voltage

If the battery pack is in Pre-Charge mode due to ***Cell Voltage (Any)*** falling to or below *Pre-Chg Voltage*, then it exits the Pre-Charge mode and enter the Fast Charge Mode (see *Fast Charge Current*) when ***Cell Voltage (All)*** rises above *Recovery Voltage*. This is one of three primary recovery methods for a battery pack in Pre-Charge mode.

Normal Setting: This is battery cell dependent. Ensure that it is set per the battery cell specifications. Setting this value too high is not harmful (except for slower charging from empty), but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage which brings them up to normal charging voltage before hitting them with a fast current. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Fast Charge Config

Fast Charge Current

This is the current that the bq20z90 reports in the ***Charging Current*** register when the bq20z90 is in Fast Charge mode (see *Pre-Chg Temperature*, *Pre-Chg Voltage*, and *Pre-Chg Current*). This current is also broadcast to a smart charger when bq20z90 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Fast Charge Mode (***Charging Current*** = *Fast Charge Current*), [FCHG] is set in ***Charging Status*** and the Charge FET is enabled. There are 3 primary criteria that must be met to be in Fast Charge Mode:

1. Assuming all temperature faults are configured correctly (*Pre-Chg Temperature* configured in Data Flash as the highest low temperature mode), ***Temperature*** is above *Pre-Chg Temperature* with [PCHG] clear in ***Charging Status***
2. ***Temperature*** is below *Suspend High Temp* and no [CHGSUSP] in ***Charging Status***
3. ***Voltage*** must be above *Pre-Chg Voltage* with [PCHG] clear in ***Charging Status***
4. ***Voltage*** must be below ***Charging Voltage*** + *Over Charging Voltage*

While in Fast Charge Mode, there is an option called Charge Throttling that is enabled/disabled by *Delta Temperature* as described below (See *Delta Temperature*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

Charging Voltage

When in any charging mode without a fault condition present, the *Charging Voltage* is the voltage that is put in ***Charging Voltage***. With most fault conditions ***Charging Voltage*** is set to 0. This is also used in bq20z90 charge qualification and termination algorithms.

Normal Setting: This register is normally set based on the charger specifications. Charger tolerances are considered when setting this register.

Delta Temp

Delta Temp is used in a "throttling" algorithm for maximizing the charging algorithm. This description starts in Fast Charge Mode with Temperature in the normal range and ***Charging Current*** = *Fast Charge Current*. The value that is in ***Charging Current*** is broadcast to smart chargers if master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*)

1. When the ***Temperature*** rises to (*Suspend High Temp – (Delta Temp* $\times$ *2)*) then the bq20z90 initiates stage 2 throttling. In this mode, the ***Charging Current*** register is changed from *Fast Charge Current* to (*Fast Charge Current –Pre-Chg Current)* / 2. Also, [TCHG2] is set in ***Charging Status***. The purpose of this stage is to request a slower ***Charging Current*** to prevent overheating of the battery. If ***Temperature*** continues to climb then see step B).
2. If the ***Temperature*** continues to rise even though the ***Charging Current*** was decreased, then when the ***Temperature*** rises to (*Suspend High Temp – Delta Temp*), the bq20z90 initiates stage 1 throttling. In this mode, the ***Charging Current*** register is changed from [(*Fast Charge Current – Pre-Chg Current*) / 2] to *Pre-Chg Current*. Also [TCHG1] is set in ***Charging Status*** and [TCHG2] is cleared.
3. If the ***Temperature*** continues to climb, then it reaches the *Suspend High Temp* which halts charging completely. (see *Suspend High Temp*).

The battery returns to Fast Charge Mode when the temperature falls back below (*Suspend High Temp – (Delta Temp*$\times$ 2)) which clears [TCHG1] and [TCHG2] in ***Charging Status***. If *Delta Temp* is set to 0, then this function is disabled.

Normal Setting: Ensure that this value is large enough to keep the battery from switching modes rapidly; however, setting it to high increases the charging time and reduces the algorithms effectiveness. This register is only required in either high temperature environments, or with extreme charge currents.

Suspend Low Temp

When the pack temperature measured by ***Temperature*** falls to or below *Suspend Low Temp* while charging ([DSG] flag clear in ***Battery Status***), then the Charge Suspend Mode is triggered. This causes ***Charging Current*** to be set to 0, [CHGSUSP] is set in ***Charging Status***, and if [CHGSUSP] set in *Operation Cfg B*, then the Charge FET and Pre-Charge FET are both opened regardless of their prior open/close state. There are two primary possible recoveries to this mode

1. The primary recovery is if ***Temperature*** rises above (*Suspend Low Temp* + *Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the suspend mode is reactivated with [DSG] flag cleared in ***Battery Status***.

With either of these recoveries, [CHGSUSP] is cleared in ***Charging Status***. This enables the charging process to resume.

Normal Setting: Notice that default *Suspend Low Temp* is lower than *Chg Inhibit Low Temp*. This value is application and battery cell dependent.

Suspend High Temp

When the pack temperature measured by ***Temperature*** rises to or above *Suspend High Temp* while charging the ([DSG] flag in ***Battery Status***), then the Charge Suspend Mode is triggered. This causes ***Charging Current*** to be set to 0, [CHGSUSP] is set in ***Charging Status***, and if [CHGSUSP] set in *Operation Cfg B*, then the Charge FET and Pre-Charge FET are both opened regardless of their prior open/close state. There are two primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** falls below (*Suspend High Temp – Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the suspend mode is reactivated with [DSG] flag cleared in ***Battery Status***.

With either of these recoveries, [CHGSUSP] is cleared in ***Charging Status***. This enables the charging process to resume.

Normal Setting: Notice that default *Suspend High Temp* is higher than *Chg Inhibit High Temp*. This value is application and battery cell dependent.

Pulse Charge Config

Pulse Charge Config is one of the most confusing setups in the bq20z90. In application, however, it is a relatively simple function. When charging, these settings can be used to turn ON and OFF the Charge FET to provide a pulse charging function. Figure 6 shows an example of a pulse charging voltage vs time wave form with all the Pulse Charge Config registers explained graphically.

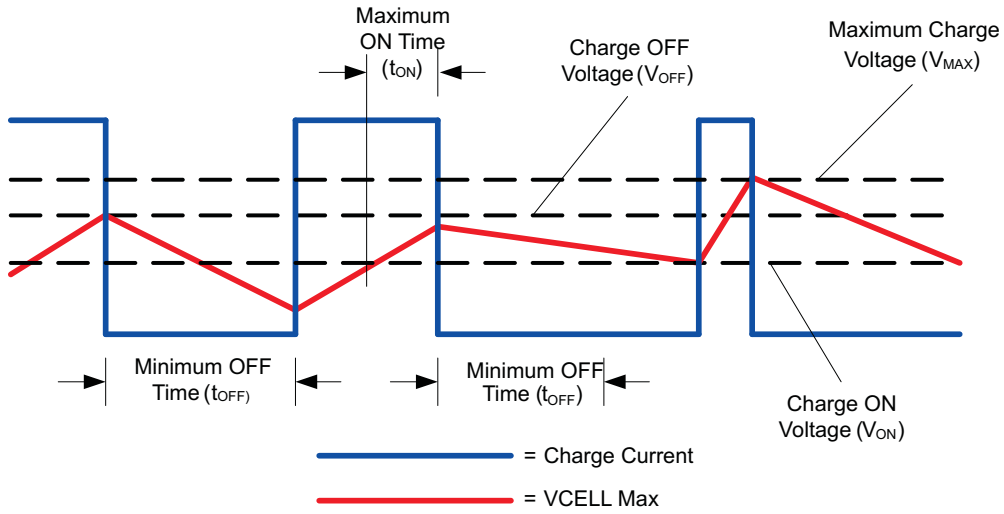


Figure 6. Pulse Charging Voltage vs Time

Turn Off Voltage

While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode ([FCHG] set in ***Charging Status***), when ***Cell Voltage (MAX)*** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates (see *Max On Pulse Time* for the rest of this process). If *Max On Pulse Time* is set to 0, then the process acts as if the *Max On Pulse Time* timer expired immediately (see *Max On Pulse Time* for the rest of this process).

Normal Setting: This is application dependent, if Pulse Charging is required, then *Turn Off Voltage* should be set below *Max Off Voltage* so that *Max On Pulse Time* is given time to expire throughout most of each charge cycle. This maximizes charge efficiency.

Turn On Voltage

This explanation is continued from *Min Off Pulse Time* (see *Min Off Pulse Time*). While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode ([FCHG] set in ***Charging Status***), the *Min Off Pulse Time* timer is initiated as soon as the Charge FET opens. Regardless of whether or not the ***Cell Voltage (MAX)*** falls below the *Turn On Voltage*, the *Min Off Pulse Time* timer must expire before the bq20z90 allows the Charge FET to be closed, and allows charge current to flow. If *Min Off Pulse*

Time timer expires prior to ***Cell Voltage (MAX)*** falling below *Turn On Voltage*, the Charge FET is not closed until ***Cell Voltage (MAX)*** reaches *Turn On Voltage*. When the Charge FET is closed, then [PLSOFF] is cleared in ***Charging Status***.

Normal Setting: This is battery cell specification specific. See the Cell manufacturer data sheet for maximum voltage allowed. Note that the cell voltage readings for this algorithm are updated every 250 ms when in pulse charging mode instead of 1 second updates with ***Cell Voltage (ALL)***.

Max On Pulse Time

This explanation is continued from *Turn Off Voltage* above (see *Turn Off Voltage*). While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode ([FCHG] set in ***Charging Status***), when ***Cell Voltage (MAX)*** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates. If *Max On Pulse Time* is set to 0, then the process acts as if the *Max On Pulse Time* timer expired immediately. The expiration of the *Max On Pulse Time* timer forces the Charge FET to open, [PLSOFF] and [PULSE] to be set in ***Charging Status***, and the *Min Off Pulse Time* timer to be initiated (See *Min Off Pulse Time*). If *Max On Pulse Time* timer does not expire prior to ***Cell Voltage (MAX)*** reaching *Max Off Voltage*, then *Max Off Voltage* forces the Charge FET to open (See *Max Off Voltage*).

Normal Setting:

This register should be set to such a time that the Charge FET will shut off by this timer most of the time and not by the *Max Off Voltage*. It is not uncommon for this register to be 0 which would only use the *Max Off Voltage* for turning off the Charge FET. Care should be taken when setting it to 0 to ensure that the voltage does not overrun enough to produce a COV condition. The default for this register is 60 and is in units of Seconds.

Min Off Pulse Time

This explanation is continued from one of the following condition descriptions.

1. *Max On Pulse Time*
2. *Max Off Voltage*
3. *Turn Off Voltage*

While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode ([FCHG] set in ***Charging Status***), the *Min Off Pulse Time* timer is initiated as soon the Charge FET opens from one of these listed conditions (1–3 above). Regardless of whether or not the ***Cell Voltage (MAX)*** falls below the *Turn On Voltage*, the *Min Off Pulse Time* timer must expire before the bq20z90 allows the Charge FET to be closed, and allows charge current to flow. If *Min Off Pulse Time* timer expires prior to ***Cell Voltage (MAX)*** falling below *Turn On Voltage*, the Charge FET is not closed until ***Cell Voltage (MAX)*** reaches *Turn On Voltage* (see *Turn On Voltage*).

Normal Setting: This register defaults to 0. This is a buffer to prevent fast oscillation of the Charge FET.

Max Off Voltage

This explanation is continued from *Max On Pulse Time* above (see *Max On Pulse Time*). While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode, when ***Cell Voltage (MAX)*** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates. If *Max On Pulse Time* timer does not expire prior to ***Cell Voltage (MAX)*** reaching *Max Off Voltage* then *Max Off Voltage* forces the Charge FET to open, [PLSOFF] and [PULSE] to be set in ***Charging Status***, and the *Min Off Pulse Time* timer to be initiated (See *Min Off Pulse Time*).

Normal Setting: This is battery cell specification specific. See the Cell manufacturer data sheet for maximum voltage allowed. Note that the cell voltage readings of this algorithm are updated every 250 ms when in pulse charging mode instead of 1 second updates with ***Cell Voltage (ALL)***.

Termination Config

Maintenance Current

Maintenance Current is only put into the ***Charging Current*** register when [TCA] is set in ***Battery Status*** by a primary charge termination (See *Taper Current*), or *TCA Set%* condition (see *TCA Set%*), or many of the fault conditions from the **1st Level Safety** and **2nd Level Safety** classes. Even with [TCA] set, if configured for Charge FET to be turned off ([CHGFET] set in *Operation Cfg B*) then ***Charging Current*** is set to 0, and [MCHG] is cleared in *Charging Status*.

Normal Setting: This register should be 0 for most if not all Li-Ion chemistries.

Taper Current

Taper Current is used in the Primary Charge Termination algorithm. ***Current*** is integrated over each of the two *Current Taper Window* periods separately, and then they are averaged separately to give two averages. Both of these averages must be below the *Taper Current* to qualify for a Primary Charge Termination. In total, a primary charge termination has the following requirements:

1. ***Voltage*** must be above (*Charging Voltage – Termination Voltage*) for the bq20z90 to start trying to qualify a termination. It must be above this voltage before bq20z90 starts trying to detect a primary charge termination.
2. An average of all ***Current*** measurements must be below *Taper Current* for two consecutive periods of *Current Taper Window* from beginning to end of each window.
3. An average of all ***Current*** measurements during each of two consecutive periods of *Current Taper Window* from beginning to end of each window must be above 0.25 mAh as integrated, and averaged over the two *Current Taper Windows*.

When these conditions are met, the primary charge termination has occurred and the following happens:

1. 1. if *TCA Set %* = –1 (disabled) then [TCA] is set in ***Battery Status*** and either of the following happens:
   a. if [CHGFET] set in *Operation Cfg B* then and ***Charging Current*** is set to 0, and the Charge FET is opened.
   b. if [CHGFET] is cleared in *Operation Cfg B* then and ***Charging Current*** is set to *Maintenance Current*.
2. If *FC_Set %* = –1 (disabled), then [FC] is set in ***Battery Status***
3. If [CSYNC] is set in *Operation Cfg B*, then ***Remaining Capacity*** is written to ***Full Charge Capacity***.

The primary charge termination mode has two clearing methods:

1. It is cleared when ***RSOC*** falls below *FC Clear %*
2. if [CHGTERM] in *Operation Cfg B* set, and ***Current*** is less than *Chg Current Threshold* for two consecutive periods of *Current Taper Window.*

Normal Settings: This register is dependent on battery cell characteristics and charger specifications. ***Average Current*** is not used for this qualification because its time constant is not the same as the *Current Taper Window*. The reason for making two Current Taper qualifications is to prevent false current taper qualifications. False primary terminations happens with pulse charging and with random starting and stopping of the charge current. This is particularly critical at the beginning or end of the qualification period. It is important to note that as the *Current Taper Window* value is increased, the current range in the 3rd requirement for primary charge termination is lowered. If you increase the *Current Taper Window*, then the current used to integrate to the 0.25 mAh is decreased, so this threshold becomes more sensitive. Therefore, care should be taken when modifying the *Current Taper Window*.

Termination Voltage

During Primary Charge Termination detection, one of the 3 requirements is that ***Voltage*** must be above (*Charging Voltage – Termination Voltage*) for the bq20z90 to start trying to qualify a termination. It must be above this voltage before bq20z90 starts trying to detect a primary charge termination.

Normal Setting: This value is dependent on charger characteristics. It needs to be set so that ripple voltage, noise, and charger tolerances are taken into account. A low value selected can cause early termination. If the value selected is too high, then it can cause no or late termination detection. An example value is 200 mV (see *Taper Current*).

Current Taper Window

During Primary Charge Termination detection, all three requirements as described in *Maintenance Current* must be valid for two periods of this *Current Taper Window* for the bq20z90 to detect a primary charge termination (see *Taper Current*).

Normal Setting: This register does not need to be modified for most applications. It is important to note that as the *Current Taper Window* value Is increased, the current range in the 3rd requirement for primary charge termination is lowered as the value increases. If the user increases the *Current Taper Window*, then the current used to integrate to the 0.25 mAh is decreased, so this threshold becomes more sensitive. Therefore, care should be taken when modifying the *Current Taper Window*.

TCA Set %

This is an alternative method to setting [TCA] in ***Battery Status***. If this is set to anything but (–)1, then this is the only normal (nonfault condition) function that sets [TCA]. This means that a Primary Charge Termination is not set [TCA] with *TCA Set %* set between 0 and 100%. IF set to (–)1, then the Primary Charge Termination algorithm is the only normal mode algorithms used to set [TCA]. If set between and including 0 and 100%, then whenever charging ([DSG] not set in ***Battery Status***) and ***RSOC*** rises above this value then [TCA] is set in ***Battery Status***. Regardless of this setting or any Primary Charge Termination setting, any fault condition that has [TCA] as part of its fault process works completely independent of these functions.

Normal Setting: This is a user preference. TCA Set % may be used if it is mandatory that [TCA] be set during the Charge process. It is a good process to use if the Primary Charge Termination is not assured every charge cycle (see *Maintenance Charge*). If the [CSYNC] bit is set in *Operation Cfg B*, then a Primary Charge Termination writes ***Remaining Capacity*** up to ***Full Charge Capacity*** and writes ***RSOC*** to 100% so [TCA] is set with this method even if *TCA Set %* is set between 0 and 100%

TCA Clear %

If during discharge ([DSG] set in ***Battery Status***), RSOC falls below this value then [TCA] is cleared.

Normal Setting: Must be set below *TCA Set %* if used.

FC Set %

This is an alternative method to setting [FC] in ***Battery Status***. If this is set to anything but (–)1, then this is the only normal function that sets [FC]. IF set to (–)1, then the Primary Charge Termination algorithm is used to set [FC]. If set between and including 0 and 100%, then whenever charging ([DSG] not set in ***Battery Status***) and ***RSOC*** rises above this value, then [FC] is set in ***Battery Status***. Regardless of this setting, any fault condition that has [FC] as part of its fault process works completely independent of this function.

Normal Setting: This is user preference. *FC Set %* may be used if it is mandatory that [FC] be set during the Charge process. It is a good process to use if the Primary Charge Termination is NOT assured ever charge period (see *Taper Current*).

FC Clear %

If during discharge ([DSG] set in ***Battery Status***), ***RSOC*** falls below this value, then [FC] is cleared.

Normal Setting: Must be set below *FC Set %* if used.

Cell Balancing Config

Min Cell Deviation

The cell balancing algorithm with be active only during charging ([DSG] cleared in ***Battery Status***). The function is disabled completely if *Min Cell Deviation* is set to 0. With impedance track, the bq20z90 knows the Full Charge Capacity for each cell independently. Each cell input in the bq29330 has an internal FET that shorts the cell filtering resistors, and an internal 500-Ω resistor across the cells that need reduced charging to help balance the cells. The bq20z90 use impedance track information along with the value for *Min Cell Deviation* to know how long to turn on the shorting FET. The algorithm works based on the formula:

Min Cell Deviation = dQ × R / (V × duty cycle)

Where:

dQ = correction factor = 3600 seconds/hour

V = nominal cell voltage = 3600 mV

duty cycle = 40% = 0.4

R = Total resistance from cell top to cell bottom (2 filter resistors and internal 500-Ω resistor), so for the bq20z90 EVM, the filter resistors are 100 Ω;

therefore,

$R = 100 \times 2 + 500 = 700\ \Omega$

So for 700 Ω in resistance Min Cell Deviation = 1750 sec/mAh

Normal Setting: The bq20z90 default value for this register is 1750 s/mAH. The only values that is needed to be changed in the formula are R (Resistance), and V (nominal cell voltage). (See SLUA340.pdf for more information)

Charging Faults

Over Charging Voltage

When the pack voltage measured by ***Voltage*** rises to or above (*Charging Voltage* + *Over Charging Voltage*), then Over Charging Voltage fault process is triggered which initiates the *Over Charging Volt Time* timer. If ***Voltage*** falls below (*Charging Voltage* + *Over Charging Voltage*) prior to the expiration of the *Over Charging Volt Time* timer, then the Over Charging Voltage fault process halts and the *Over Charging Volt Time* timer resets. If the ***Voltage*** continues to be above (*Charging Voltage* + *Over Charging Voltage*) until the *Over Charging Volt Time* timer expires, then the bq20z90 sets the [OCHGV] in ***Charging Status*** and if [OCHGV] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. The bq20z90 clears the Over Voltage fault condition when ***Voltage*** falls to or below Charging .

Voltage.**Normal Setting:** This value should be high enough that ripple on the charger voltage does not cause a false Over Charging Voltage fault, but low enough to allow for a normal fault condition.

Over Charge Voltage Time

When the *Over Charging Voltage* criteria are met then Over Charging Voltage fault process is triggered which initiates the *Over Charging Volt Time* timer. If the Over Charging Voltage criteria continue to be met until the *Over Charging Volt Time* timer expires, then the bq20z90 sets [OCHGV] in ***Charging Status***, and if [XCHGV] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. If ***Voltage*** falls below *Over Charging Voltage* criteria any time prior to the expiration of the *Over Charging Volt Time* timer, then the Over Charging Voltage fault process halts and the *Over Charging Volt Time* timer resets. The bq20z90 clears the Over Voltage fault condition when ***Voltage*** falls to or below *Charging Voltage*. (See *Over Charging Voltage*)

Normal Setting: The default for this register is 2 seconds. This should be sufficient for most applications. This function is not disabled if set to 0. Instead it triggers immediately.

Over Charging Current

When the current as measured by ***Current*** rises up to or above (***Charging Current*** + *Over Charging Current*) then Over Charging Current fault process is triggered which initiates the *Over Charging Current Time* timer. If ***Current*** falls below (***Charging Current*** + *Over Charging Current*) prior to the expiration of the *Over Charging Current Time* timer, then the Over Charging Current fault process halts and the *Over Charging Current Time* timer resets. If the ***Current*** continues to be above (***Charging Current*** + *Over Charging Current*) until the *Over Charging Current Time* timer expires, then the bq20z90 sets [OCHGI] in ***Charging Status*** and if [XCHGI] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes Charging Current and Charging Voltage to be set to 0. The bq20z90 clears the Over Current fault condition when ***Average Current*** falls to or below *Over Charging Recovery Current*.

Normal Setting: This setting should be set high enough to prevent false triggering, but low enough to prevent battery cell damage. The default setting is 500 mA which is sufficient for most applications.

Over Charging Current Time

When the *Over Charging Current* criteria are met, then Over Charging Current fault process is triggered which initiates the *Over Charging Current Time* timer. If the *Over Charging Current* criteria continue to be met until the *Over Charging Current Time* timer expires, then the bq20z90 set the [OCHGI] in ***Charging Status*** and if [XCHGV] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition

causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. If ***Current*** falls below *Over Charging Current* criteria any time prior to the expiration of the *Over Charging Current Time* timer, then the Over Charging Current fault process halts and the *Over Charging Current Time* timer resets. The bq20z90 clears the Over Current fault condition when ***Average Current*** falls to or below *Over Charging Recovery Current*.

Normal Setting: The default for this register is 2 seconds. This is sufficient for most applications. This function is not disabled if set to 0. Instead it triggers immediately.

Over Charging Recov Curr

When the *Over Charging Current* criteria are met to the point of forcing an Over Charging Condition Fault, then the bq20z90 clears the Over Current fault condition when ***Average Current*** falls to or below *Over Charging Recovery Current*.

Normal Setting: The default for this register is 100 mA. This is sufficient for most applications.

Depleted Voltage

When the voltage measured by ***Voltage*** falls to *Depleted Voltage* threshold and stays at or below this level for more than *Depleted Voltage Time* seconds, then the bq20z90 sets the [XCHGLV] in ***Charging Status*** and the [TDA] in ***Battery Status***. If [CS_XCHGLV] bit is set in *Charge Fault Cfg*, then the discharge FET is turned off. A charger must be detected as present for a *Depleted Voltage* fault to occur. See *Charger Present* for a description on how to detect a charger.

Normal Setting: This function is not recommended if there is any external voltage source that could interfere with *Charger Present*. Set *Depleted Voltage Timer* to 0 to disable this function. This register is variable depending on the lowest possible system voltage. Set this value just above what the system requires for the lowest possible voltage.

Depleted Voltage Time

See *Depleted Voltage*. The ***Voltage*** must be equal to or below the Depleted Voltage for at least this time (*Depleted Voltage Time*) for the bq20z90 to register a [XCHGLV] fault in ***Charging Status***. If set to 0, then *Depleted Voltage* function is completely disabled.

Normal Setting: The default value for this register is 2 seconds. Ensure that this register is set to prevent false readings or spiked load currents from triggering a premature fault. With high current loads, be sure that this register is set short enough to prevent the system from detecting a low voltage since voltage is normally dropping very rapidly at this level.

Depleted Recovery

When the voltage as measured by ***Voltage***, rises to or above this value while charging then the [OCHGLV] flag is cleared in *Charging Status*. If the discharge FET was turned off, it returns to the on state.

Normal Setting: This register should be set at least several hundred millivolts higher than the *Depleted Voltage* to ensure hysteresis through this transition.

Over Charge Capacity

Over Charge Capacity is detected in a two-step process. First the battery must be charged to the point where Remaining Capacity reaches ***FCC*** (***Full Charge Capacity***). Then any charge applied after this point is still measured but not displayed by the bq20z90. When this charge as measured by the bq20z90 reaches a threshold as defined by ***FCC*** + *Over Charge Capacity*, then the bq20z90 goes into a charging fault condition. The [OC] in ***Charging Status*** is set. ***Charging Voltage*** and ***Charging Current*** are both set to 0. If [OC] set in *Charge Fault Cfg*, then the Charge FET is turned off.

Normal Setting: This register is application dependent but a good example is 100 to 300 mAh for each cell in parallel. To small of a value could force false detections, and to large a value could damage the cells if normal charge termination methods fail.

Over Charge Recovery

There are three recovery methods for the bq20z90.

1. The first involves *Over Charge Recover* and only happens if [NR] in *Operation Cfg B* is set. With this setting, the bq20z90 recovers from an overcharged condition with a continuous discharge of *Over Charge Recovery* mAHs.
2. With [NR] cleared in *Operation Cfg B*, the bq20z90 recovers from the overcharge fault with a pack removal and reinsertion ($\overline{\text{PRES}}$ transition).
3. The third recovery happens when ***RSOC*** falls below the *FC Clear %*. This recovery also is the only one that returns ***Charging Voltage*** and ***Charging Current*** to normal.

Normal Setting: This value is normally small. Typically around 2 mAh. Its only purpose is to ensure small discharge spikes or false discharge detections do not clear the condition prematurely.

FC-MTO

If charging current is greater than *Chg Current Threshold* and [FCHG] is set in ***Charging Status*** for *FC-MTO* time in seconds, then the bq20z90 sets [FC-MTO] (fast time mode timeout) in ***Charging Status***, ***Charging Voltage*** and ***Charging Current*** are set to 0, [TCA] is set in ***Battery Status***, and if [FCMTO] is set in *Charge Fault Cfg* then the Charge FET is turned off. If charging is interrupted ([DSG] in ***Battery Status*** sets) and an *Over Charging Curr Recov* amount of discharge is detected anytime during the charging process prior to *FC-MTO* timer expiring, then the *FC-MTO* timer is reset and starts counting from 0. The bq20z90 recovers from an *FC-MTO* fault with the following conditions:

1. The fault condition is cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*.
2. If ***Current*** falls below *Dsg Current Threshold*

If *FC-MTO* is 0, then this function is disabled.

Normal Settings: The purpose of this register is another form of charge protection. If this timer has timed out, then something has gone wrong and the battery is taking to long to charge. The default setting for this register is 10800 seconds. This may be short for some applications. Be sure and give plenty of time for all possible scenarios. Smaller charge currents may require longer settings. It is also important to note that as a battery ages, the charge time increases due to increased impedance. Setting this value short limits the capacity of aged cells.

PC-MTO

If charging current is greater than *Chg Current Threshold*, and [PCHG] is set in ***Charging Status*** for *PC-MTO* time in seconds, then the bq20z90 sets [PC-MTO] (precharge time mode timeout) in ***Charging Status***, ***Charging Voltage*** and ***Charging Current*** are set to 0, [TCA] is set in ***Charging Status***, and if [PCMTO] is set in *Charge Fault Cfg* then the Charge FET/Pre-Charge FET is turned off. If charging is interrupted ([DSG] in ***Charging Status*** sets) and an *Over Charging Curr Recov* amount of discharge is detected anytime during the charging process prior to *FC-MTO* timer expiring, then the *FC-MTO* timer is reset and starts counting from 0. The bq20z90 recovers from a *PC-MTO* fault with the following conditions:

1. The fault condition is cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*.
2. If ***Current*** falls below *Dsg Current Threshold*

If *PC-MTO* is 0 then this function is disabled.

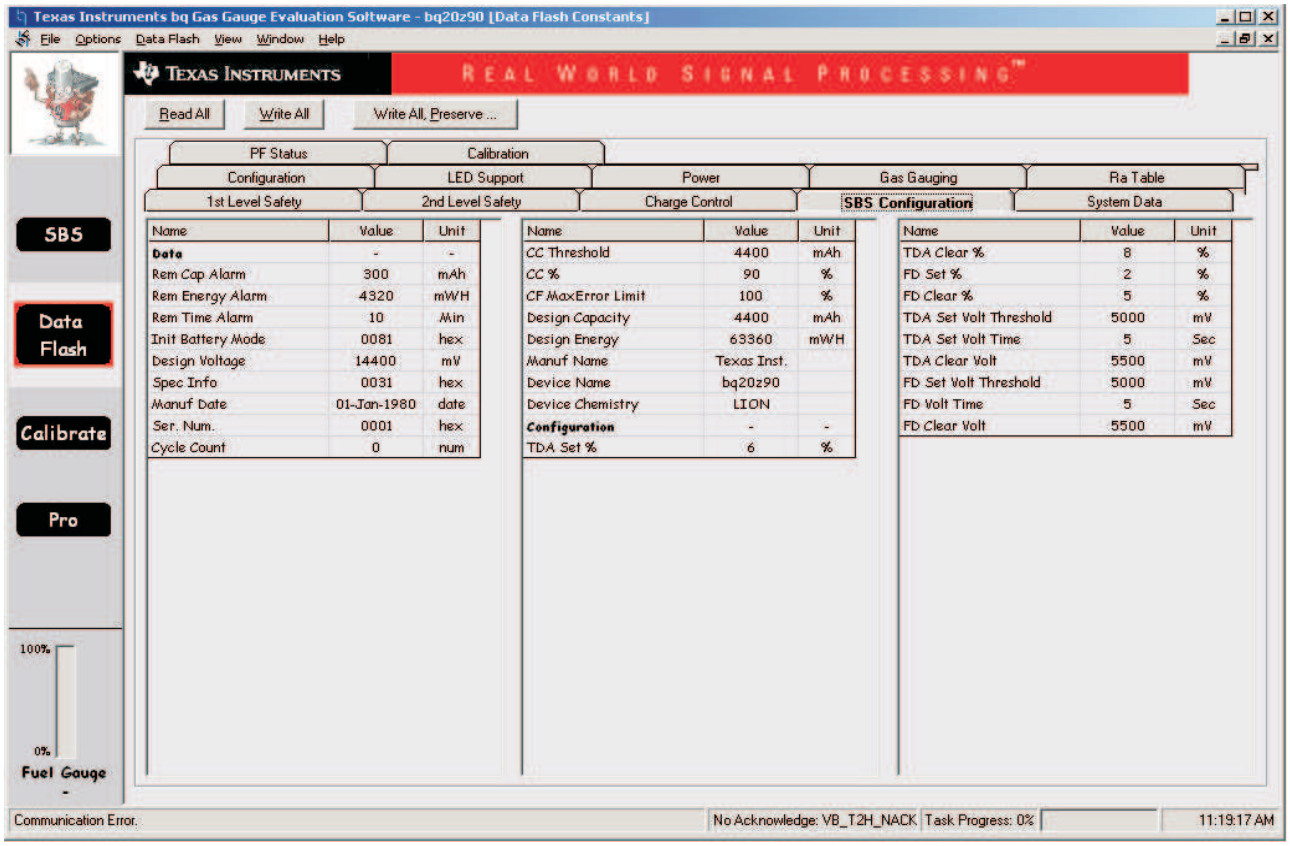
Normal Settings: The purpose of this register is another form of charge protection. If this timer has timed out, then something has gone wrong and the battery is taking to long to charge. The default setting for this register is 3600 seconds. This is good for most applications. Smaller charge currents may require longer settings.

Charge Fault Configuration

—	—	PCMTO	FCMTO	OCHGV	OCHGI	OC	CS_XCHGLV

- PCMTO: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *PC-MTO* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- FCMTO: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *FC-MTO* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- OCHGV: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charging Voltage* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- OCHGI: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charging Current* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- OC: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charge* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- CS_XCHGLV: If set, then the discharge FET is turned off when a Depleted Voltage fault condition occurs.
  Normal Setting: Default is 0 (disabled)

2.5 SBS Configuration



SBS Data

Rem Cap Alarm

When the ***Remaining Capacity*** falls below this value, [RTA] is set in ***Battery Status***.

Normal Setting: About 10% of the *Full Charge Capacity*. This value is programmed into ***RemainingCapacityAlarm*** on device initialization

Rem Energy Alarm

When the bq20z90 is in milliwatt mode ([CapM] set in ***Battery Mode***), the value in *Rem Energy Alarm* is written to the ***Rem Cap Alarm***. Once this value is written to ***Rem Cap Alarm*** then the function will act the same as *Rem Cap Alarm* except units are in milliwatts. (See *Rem Cap Alarm*)

Normal Setting: About 10% of the *Full Charge Capacity* but units have to be converted to milliwatts. This data flash value is only used when in milliwatt mode. This value is programmed into ***RemainingCapacityAlarm*** on device initialization if in milliwatt mode.

Rem Time Alarm

When the average time to empty falls below this value, then the [RTA] flag is set in ***Battery Status***.

Normal Setting: Approximately 10 minutes. This value is programmed into ***RemainingTimeAlarm*** on device initialization.

Init Battery Mode

This is the default value loaded into ***Battery Mode*** on all resets, and when the bq20z90 wakes from sleep. The primary purpose of having an initial value for this register is to enable milliwatt mode whenever the bq20z90 resets or wakes up from sleep.

Normal Setting: In most applications, this register should be 0x0081. If the application requires the bq20z90 to wake in mW mode, then this value can be set to 0x8081. Care should be taken with this setting; however, because the ***Battery Mode*** register is writable even when the bq20z90 is sealed. The mW mode bit can be accidentally written to a 0.

Design Voltage

This is the theoretical nominal voltage of the battery pack. This value is used in ***ATRATE*** calculations and milliWatt mode (***Battery Mode*** MSByte bit 7).

Normal Setting: This varies by cell manufacturer, but Li-Ion is normally about 3.6-V per cell. See the cell manufacturer data sheet for the exact numbers. This value is programmed into ***DesignVoltage*** on device initialization.

Spec Info

This performs two purposes. The high byte has the current and voltage multipliers. The bq20z90 does not require any multiplier, so use 0x00. The low byte is the SBS specification revision. See the SBS Implementers Forum web page for more information (http://www.sbs-forum.org/specs/index.html).

Normal Setting: 0x0031 for SBS specification v1.1 with PEC error checking, or 0x0021 for SBS specification V1.1 without PEC error checking.

Mfg Date

This is the date of manufacture. It is stored in the Data Flash in packed format. All bqEV Software and bqMTester both accept input of this date in standard date format so the packed format does not need to be used input. It is then translated by the software to packed format. This data does not affect the operation, nor is it used by the part in any way.

Ser Num

This is a 16 bit serial number that does not affect the operation nor is it used by the part in any way. It is normally used for battery identification.

Cycle Count(CC)

There are two methods to increment *Cycle Count*:

1. If [CCT] is set in *Operation Cfg B*, then this CC% is used to increment *Cycle Count*. When the bq20z90 accumulates enough discharge capacity equal to (*CC%* × ***Full Charge Capacity***), then it increments *Cycle Count* by 1. If at any time (*CC%* × ***Full Charge Capacity***) is less than *Cycle Count Threshold*, then the *Cycle Count Threshold* is used to increment *Cycle Count*.
2. If [CCT] is cleared in Operation Cfg B, then *Cycle Count Threshold* is always be used to increment Cycle Count. When the bq20z90 accumulates enough discharge capacity equal to the *Cycle Count Threshold*, then it increments Cycle Count by 1.

This discharge capacity used by either of these methods does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *Cycle Count Threshold* or *CC %* depending on [CCT]. Then *Cycle Count* is incremented. Every increment of *Cycle Count* between QMAX updates increments ***MaxErr*** by 0.05%. It takes 20 increments of *Cycle Count* to increment ***MaxErr*** by 1%, so that it is visible in the SBS register.

Normal Setting: This should be set to 0.

Cycle Count Threshold

If [CCT] is cleared in *Operation Cfg B*, then this value is always used to increment *Cycle Count*. When the bq20z90 accumulates enough discharge capacity equal to the *Cycle Count Threshold*, then it increments *Cycle Count* by 1. This discharge capacity does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *Cycle Count Threshold*, and increments *Cycle Count*. If [CCT]is set, then see *CC%.*

Normal Setting: This is normally set to about 80% of the *Design Capacity*.

CC%

If [CCT] is set in *Operation Cfg B*, then this value is used to increment *Cycle Count*. When the bq20z90 accumulates enough discharge capacity equal to (*CC%* × *FCC*), then it increments *Cycle Count* by 1. If at any time (*CC%* × ***Full Charge Capacity***) is less than *Cycle Count Threshold*, then the *Cycle Count Threshold* is used to increment *Cycle Count*. This discharge capacity does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the (*CC%* × *FCC*), and increments *Cycle Count*. If [CCT] is clear, then see *Cycle Count Threshold*.

Normal Setting: This is normally set to 80–90%. This can be set closer to *FCC* than the *Cycle Count Threshold* method because it tracks with *FCC* as it decreases with age. This keeps cycle count tracking closely with each discharge cycle as the battery ages. Ensure that *Cycle Count Threshold* has a meaningful value even if *CC%* is used because the *Cycle Count Threshold* is used if (*CC%*×***Full Charge Capacity***) is less than *Cycle Count Threshold*.

CF Max Error Limit

The bq20z90 forces [CF] to be set in ***Battery Mode*** if ***MaxErr*** goes above the value stored in this register. This value is used to give an alternate method for setting the [CF] flag in ***Battery Mode***, other than the impedance track algorithm. The [CF] flag is a condition request flag indicating the battery would like a full charge/discharge cycle, and rarely is set by impedance track because accurate capacity measurements are always updated.

Normal Setting: This register is normally set to 100 and is in units of %.

Design Capacity

Design Capacity is the data flash location that is reported in the ***Design Capacity*** register when [CapM] is clear in ***Battery Mode***. If [CapM] is set in ***Battery Mode***, then *Design Energy* is reported in ***Design Capacity***. This value is used also for the ***ASOC*** calculation by the bq20z90 if [CapM] is cleared in ***Battery Mode***.

Normal Setting: This value should be set based on the application battery specification. See the battery manufacturer data sheet.

Design Energy

Design Energy is the data flash location that is reported in the ***Design Capacity*** register if [CapM] is set in ***Battery Mode***. If [CapM] is clear in ***Battery Mode***, then *Design Capacity* is reported in ***Design Capacity***. This value is used also for the ***ASOC*** calculation by the bq20z90 if [CapM] is set in ***Battery Mode***.

Normal Setting: This value is be set based on the application battery specification. See the battery manufacturer data sheet. At higher rates of discharge, energy is less, so referring to discharge data similar to the typical rate of the user's application is important to obtain a meaningful value.

Manuf Name

String data that can be a maximum of 11 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x20.

Device Name

String data that can be a maximum of 7 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x21.

Device Chemistry

String data that can be a maximum of 4 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x22 .

Configuration

These are alternative methods for setting and clearing [TDA] and [FD] in ***Battery Status***. They are in addition to traditional methods or fault conditions explained in this document.

TDA Set %

If set to a value between 0 and 100 then when ***RSOC*** falls to or below this value, then [TDA] in ***Battery Status*** is set. If set to (–)1, then this function is disabled. *TDA Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference. This is the threshold that the bq20z90 requests that discharge be halted because the battery is nearing depletion. If used, it is normally set around 6%. Be sure that if *TDA Clear %* is used, then this should be used as well. They only work together.

TDA Clear %

If set to a value between 0 and 100 then when ***RSOC*** rises to or above this value after being set by *TDA Set %*, then [TDA] in ***Battery Status*** is cleared. This register can only be used to clear [TDA] if it was set by TDA Set %. If set to (–)1 then this function is disabled. *TDA Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 8%. Be sure that if *TDA Set %* is used then this should be used as well. They only work together.

FD Set %

If set to a value between 0 and 100 then when ***RSOC*** falls to or below this value then [FD] in ***Battery Status*** is set. If set to (–)1 then this function is disabled. *FD Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [FD] is completely unaffected by this register.

Normal Setting: This is user preference. This is a stronger request than TDA. The battery is presumed dead at this point. If used it is normally set around 2%. Be sure that if FD *Clear %* is used then this should be used as well.

FD Clear %

If set to a value between 0 and 100 then when ***RSOC*** rises to or above this value after being set by *FD Set %*, then [FD] in ***Battery Status*** is cleared. If set to (–)1 then this function is disabled. *FD Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 5%. If FD *Set %* is used, then this should be used as well. They only work together.

TDA Set Volt Threshold

When battery voltage as measured by ***Voltage*** falls to or below the *TDA Set Volt Threshold* value for *TDA Set Volt Time* seconds, then [TDA] in ***Battery Status*** is set. This works completely independent of *TDA Set %*. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 6% ***RSOC***.

TDA Set Volt Time

See *TDA Set Volt*. This is the time that the battery voltage must be equal to or below *TDA Set Volt Threshold* before [TDA] is set in ***Battery Status***.

Normal Setting: This is normally set to 5 seconds but depends on the application.

TDA Clear Volt Threshold

When battery voltage (as measured by ***Voltage***) rises to or above this value, then [TDA] in ***Battery Status*** is cleared. [TDA] is only cleared with this threshold if it was set by *TDA Set Volt* criteria, and it is not cleared if it was set by any other methods.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 8% ***RSOC***.

FD Set Volt Threshold

When battery voltage as measured by ***Voltage*** falls to or below the *FD Set Volt Threshold* value for *FD Set Volt Time* seconds, then [FD] in ***Battery Status*** is set. This register works completely independent of *FD Set %*. Any fault condition that specifies setting [FD] is completely unaffected by this register.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 2% ***RSOC***.

FD Set Volt Time

See *FD Set Volt*. This is the time that the battery voltage must be equal to or below *FD Set Volt Threshold* before [FD] is set in ***Battery Status***.

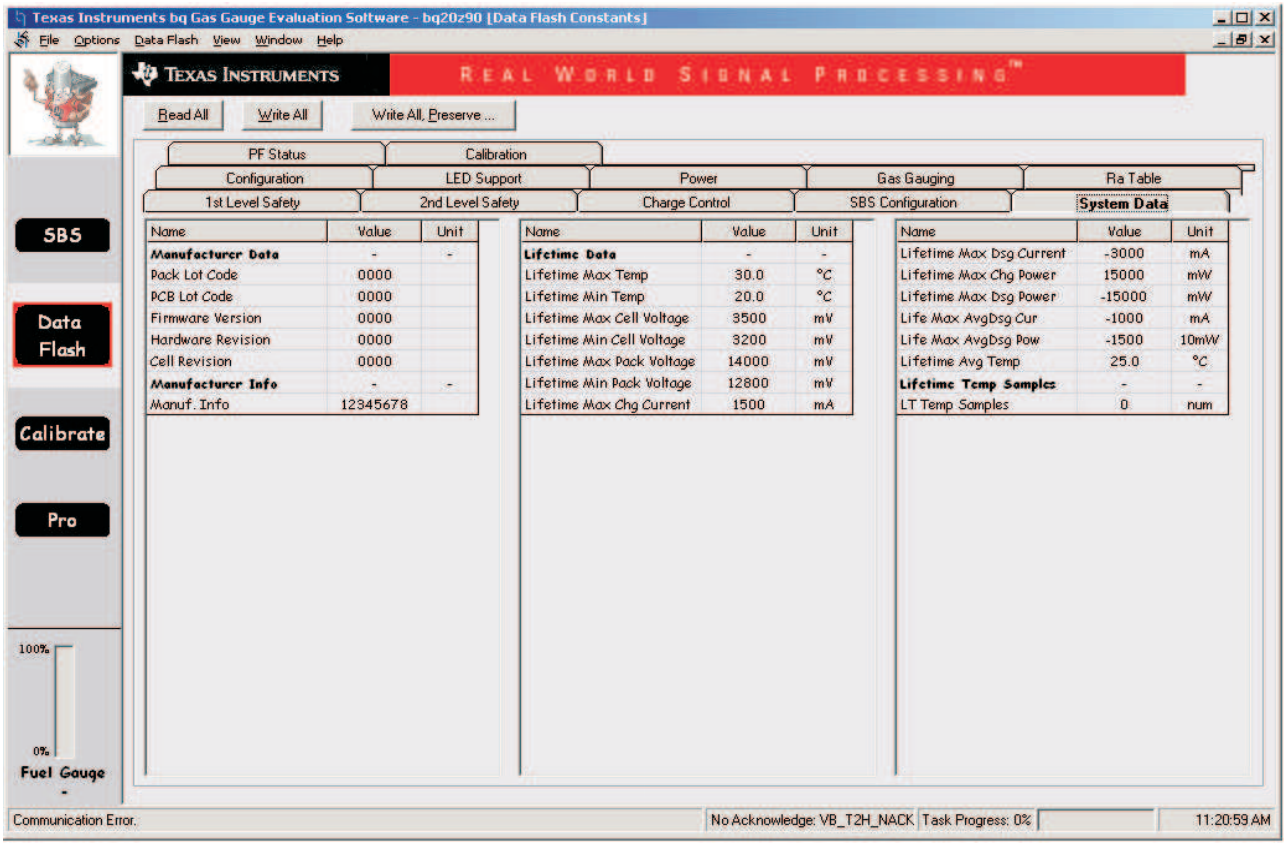
Normal Setting: This is normally set to 5 seconds but depends on the application.

FD Clear Volt Threshold

When battery voltage as measured by ***Voltage*** rises to or above this value, then [FD] in ***Battery Status*** is cleared. [FD] is cleared from this threshold only if it was set by *FD Set Volt* criteria.

Normal Setting: This is user preference, but it must be a voltage that the battery is at under normal loads at around 5% ***RSOC***.

2.6 System Data



Manufacturer Data

Pack Lot Code

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: The most common use of this register is as an extension to the *Serial Number* as a form of pack identification. It is only readable via ***Manufacturer Data*** (0x23) string read.

PCB Lot Code

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: The most common use of this register is as an extension to the *Serial Number* as a form of pack identification. It is only readable via ***Manufacturer Data*** (0x23) string read.

Firmware Version

This is a 16 bit value that does not affect operation nor is it used by the part in any way. It is intended as a firmware revision however it is not protected so it is not reliable. Use ***Manufacturing Access Commands*** to get a reliable firmware version of the bq20z90.

Normal Setting: This can be used for any user data. It is only readable via ***Manufacturer Data*** (0x23) string read.

Hardware Revision

This is a 16 bit value that does not affect operation nor is it used by the part in any way. It is intended as a IC hardware revision; however, it is not protected so it is not reliable. Use ***Manufacturing Access Commands*** to get a reliable firmware version of the bq20z90.

Normal Setting: This can be used for any user data. It is only readable via ***Manufacturer Data*** (0x23) string read.

Cell Revision

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: This can be used for any user data. It is only readable via ***Manufacturer Data*** (0x23) string read.

Manufacturer Info

Manuf. Info

This is string data that can be any user data. It can be a maximum of 8 characters.

Normal Setting: Can be used for any user data.

Lifetime Data

Lifetime Max Temp

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum temperature as measured by ***Temperature*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Temp* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Temp* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Temp* by at least 1°C
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Temp

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum temperature as measured by ***Temperature*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Temp* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Temp* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Temp* by at least 1°C
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Cell Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum cell voltage as measured by ***Cell Voltage (Max)*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Cell Voltage* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Cell Voltage* for 60 seconds

2. If the internal RAM location is greater than *Lifetime Max Cell Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Cell Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum cell voltage as measured by ***Cell Voltage (Min)*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Cell Voltage* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Cell Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Cell Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Pack Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum pack voltage as measured by ***Voltage*** is updated continuously in a reserved RAM location. To prevent flash wear out, this RAM only updates with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Pack Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Pack Voltage* by at least 100 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Pack Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum cell voltage as measured by ***Voltage*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Pack Voltage* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Pack Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Pack Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Chg Current

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum current in the charge direction as measured by ***Average Current*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Chg Current* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Chg Current* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Chg Current* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Dsg Current

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum current in the discharge direction as measured by ***Average Current*** is updated continuously in a reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Dsg Current* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is less than (–)*Lifetime Max Chg Current* for 60 seconds
2. If the internal RAM location is less than (–) *Lifetime Max Chg Current* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Chg Pwr

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum power in the charge direction as measured by a reserved continually updated average power register (uses ***Voltage***×***Current*** in an internal averaging algorithm) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Chg Pwr* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Chg Power* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Chg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Dsg Pwr

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum power in the discharge direction as measured by a reserved continually updated average power register (uses ***Voltage***×***Current*** in an internal averaging algorithm) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Dsg Power* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is less than (–)*Lifetime Max Chg Current* for 60 seconds.
2. If the internal RAM location is less than (–) *Lifetime Max Chg Current* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Life Max Avg Dsg Pwr

Power is averaged over every discharge cycle. Every discharge cycle an internal unaccessible RAM Register (LastAveragePower) is updated with this average power. The maximum power in the discharge direction as measured by this last average discharge power register (uses ***Voltage***×***Current*** in an internal averaging algorithm) is updated continuously in a lifetime data reserved RAM location. When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), the *Life Max Avg Dsg Pwr* data flash register is updated from this RAM location but only with any one of the following 3 conditions:

1. Whenever the internal RAM location is **less** than (–) *Lifetime Max Avg Dsg Power* for 60 seconds.
2. If the internal RAM location is **less** than (–) *Lifetime Max Avg Dsg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Life Min Avg Dsg Pwr

Power is averaged over every discharge cycle. Every discharge cycle an internal unaccessible RAM Register (LastAveragePower) is updated with this average power. The minimum power in the discharge direction as measured by this last average discharge power register (uses ***Voltage***×***Current*** in an internal averaging algorithm) is updated continuously in a lifetime data reserved RAM location. When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), the *Life Min Avg Dsg Pwr* data flash register is updated from this RAM location but only with any one of the following 3 conditions:

1. Whenever the internal RAM location is **greater** than (–) *Lifetime Min Avg Dsg Power* for 60 seconds.
2. If the internal RAM location is **greater** than (–) *Lifetime Min Avg Dsg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Avg Temp

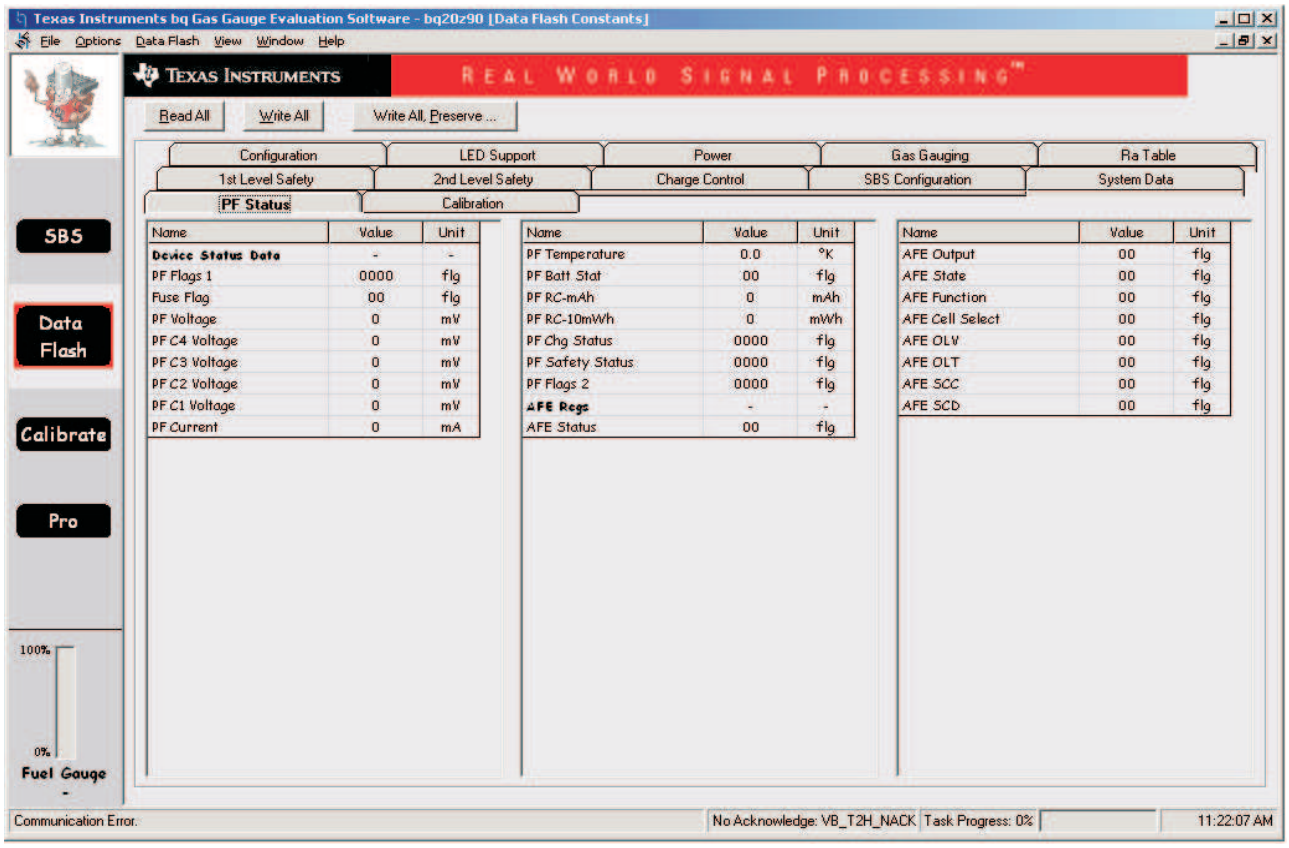
Temperature is averaged over the entire life of the battery. The temperature is sampled from the ***Temperature*** register every 1/16th of an hour. Then summed given the last Temperature Sum (***Temperature*** + Previous ***Temperature*** Sum) as updated the previous 1/16th of an hour sample and then divided by *LT Temp Samples*. This is then updated continuously in a lifetime data reserved RAM location. To prevent flash wear out, this RAM only updates to data flash when any other Lifetime Data locations update to data flash after meeting their update criteria. Impedance Track must be enabled ([QEN] set in Operation Status) for this data flash update to occur.

Lifetime Temp Samples

LT Temp Samples

LT Temp Samples are used to compute the *Lifetime Avg Temp*. Temperature is averaged over the entire life of the battery. The temperature is sampled from the ***Temperature*** register every 1/16th of an hour, then summed given the last Temperature Sum (***Temperature*** + Previous ***Temperature*** Sum)as updated the previous 1/16th of an hour sample and then divided by *LT Temp Samples*. *LT Temp Samples* is then incremented by 1. *LT Temp Samples* is updated continuously in a lifetime data reserved RAM location. To prevent flash wear out, this RAM location only updates when any other Lifetime Data location updates to data flash after meeting their update criteria. Impedance Track™ must be enabled ([QEN] set in Operation Status) for this data flash update to occur.

2.7 PF Status



There is no configuration or settings required for the PF Status Class. The entire PF Status class should all be zeros for every register. This class is intended only for reporting failure information to the factory and Texas Instruments. In fact, it only reports any information with catastrophic failures or during development time as a tool to help with configuration or layout issues.

Device Status Data

PF Flags 1

This location indicates all the causes of permanent failures that have occurred from the time the bq20z90 was last programmed with new firmware or the last time this register was cleared. It is important to understand that more than one fault can be recorded here if multiple faults have occurred. *PF Flags 1* bit locations and definitions correspond to ***PF Status***. If the corresponding bit in PF Flags 1 is enabled in the *Permanent Fail Cfg* register then the bq20z90 attempts to blow the fuse in addition to record the permanent failure in the *PF Flags 1 register*. This register is cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z90 (See the bq20z90 data sheet). This is the only register in the data flash which ignores the disabled data flash writing setting when a permanent failure occurs. (See *Permanent Fail Cfg*)

FBF	–	–	SOPT	SOCD	SOCC	AFE_P	AFE_C
DFF	DFETF	CFETF	CIM	SOTD	SOTC	SOV	PFIN

- FBF: Set if *Fuse Fail Limit* fault has occurred and the function is enabled. If the *Fuse Flag* has been set to 0x3672 (SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90) and the current as measured by ***Current*** still exists which is greater than *Fuse Fail Limit* in milliamps, or less than a (–) *Fuse Fail Limit* for *Fuse Fail Time*, then the this flag is set. See *Fuse Fail Limit*.
- SOPT: Set if a Safety Open Thermistor Fault has occurred and the function is enabled. If *Open Thermistor Time* is set to 0, then this function is disabled. If [XSOPT] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse* Flag. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *SOC Dsg*).
- SOCD: Set if a Safety Over Current Discharge Fault has occurred and the function is enabled. If *SOC Dsg Time* is set to 0, then this function is disabled. If [XSOCD] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse* Flag. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *SOC Dsg*).
- SOCC: Set if a Safety Over Current Charge Fault has occurred and the function is enabled. If *SOC Chg Time* is set to 0, then this function is disabled. If [XSOCC] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *SOC Chg*).
- AFE_P: Set if a Periodic AFE Check Fault has occurred and the function is enabled. If *AFE Check Time* is set to 0, then this function is disabled. If [XAFE_P] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *AFE Check Time*).
- AFE_C: Set if an AFE Communication Fault has occurred. If *AFE Fail Limit* is set to 0, then this function is disabled. If [XAFE_C] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *AFE Fail Limit*).
- DFF: The bq20z90 verifies all data flash writes and will set [DFF] if a Data Flash Verify Fault has occurred Only the setting of [DFF] can be disabled. If [XDFF] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90.
- DFETF: Set if a Discharge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XDFETF] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *FET Fail Time*).
- CFETF: Set if a Charge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XCFETF] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *FET Fail Time*).
- CIM: Set if a Cell Imbalance Fault has occurred and the function is enabled. If *Battery Rest Time* is set to 0, then that function is disabled. If [XCIM] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *Battery Rest Time*).
- SOTD: Set if a Safety Over Temperature Discharge Fault has occurred and the function is enabled. If *SOT Dsg Time* is set to 0, then this function is disabled. if [XSOTD] is set in *Permanent Fail Cfg,* then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *SOT Dsg*).

- SOTC: Set if a Safety Over Temperature Charge Fault has occurred and the function is enabled. If *SOT Chg Time* is set to 0, then this function is disabled. If [XSOTC] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag.* The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *SOT Chg*).
- SOV: Set if a Safety Over Voltage Threshold Fault has occurred and the function is enabled. If *SOV Time* is set to 0, then this function is disabled. if [XSOV] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *SOV Threshold*).
- PFIN: The bq20z90 monitors the PFIN line. When the PFIN line goes low for *PFIN Detect Time*, then the bq20z90 attempts to report a PFIN Fault if the function is enabled. If *PFIN Detect Time* is set to 0 then this function is disabled. if [XPFIN] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90 (See *PFIN Detect Time*)

Fuse Flag

This is set to 0x3672 when the bq20z90 sets any permanent failure flags in ***PF Status***. Otherwise this register is 0x0000. This register is cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z90. See the bq20z90 Technical Reference Manual (SLUU241) for more information on clearing permanent failures.

PF Voltage

The ***Voltage*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C1 Voltage

The ***Cell Voltage 1*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C2 Voltage

The ***Cell Voltage 2*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C3 Voltage

The ***Cell Voltage 3*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C4 Voltage

The ***Cell Voltage 4*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Current

The ***Current*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Temperature

The ***Temperature*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Batt Stat

The ***Battery Status*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF RC (mAh)

The ***Remaining Capacity*** register in mAh is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF RC (10mWh)

The ***Remaining Capacity*** register in mWh is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Charging Status

The ***Charging Status*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Safety Status

The ***Safety Status*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Flags 2

This register reports the first permanent failure that occurred from the time the bq20z90 was last programmed with new firmware. The difference between this register and PF Flags 1 is that this register only records one failure and it is the first one in a possible series of failures. This method gives a better chance to learn what could have caused a whole series of failures by knowing what the first failure was.

AFE Regs

All AFE registers are captured at the time that the most recent permanent failure occurred. This subclass should always be 0 unless a permanent failure has occurred.

AFE Status

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Output

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE State

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Function

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Cell Select

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE OLV

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE OLT

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

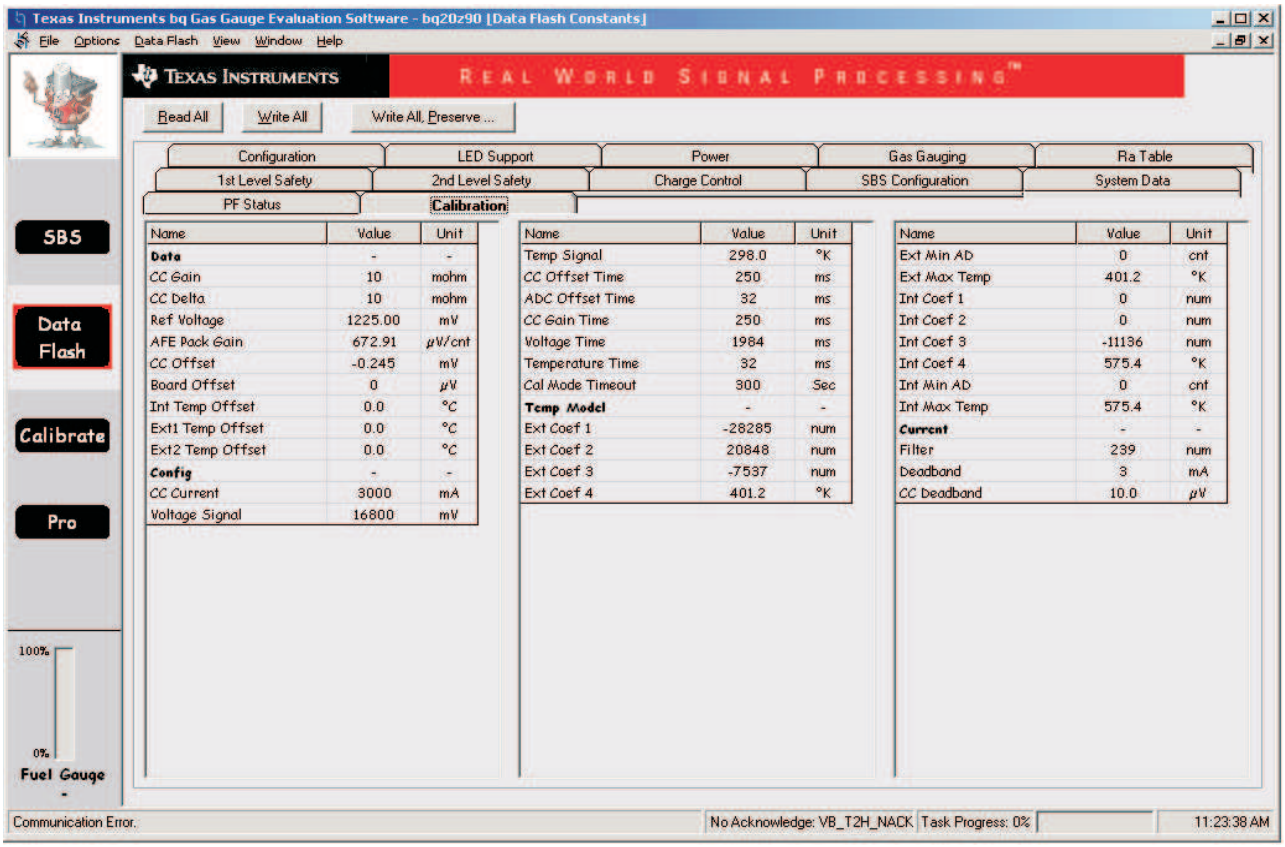
AFE SCC

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE SCD

The internal RAM copy in the AFE Status register in the bq20z90 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

2.8 Calibration



Data

Most of these values should never need to be modified by the user. They should only be modified by the Calibration commands in Calibration mode as explained in the *Calibration* application note SLUA379.

CC Gain

This is the gain factor for calibrating out Sense Resistor, Trace, and internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports ***Current***. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports Current cancels out the time base since ***Current*** does not have a time component (it reports in mA) and *CC Delta* requires a time base for reporting ***Remaining Capacity*** (it reports in mAh).

Normal Setting:*CC Gain* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of Gas Gauges* application note SLUA379 for more information.

CC Delta

This is the gain factor for calibrating out Sense Resistor, Trace, and internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports charge and discharge in and out of the battery through the ***Remaining Capacity*** register. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports ***Current*** cancels out the time base since ***Current*** does not have a time component (it reports in mA) and *CC Delta* requires a time base for reporting ***Remaining Capacity*** (it reports in mAh).

Normal Setting:*CC Delta* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of gas Gauges* application note SLUA379 for more information.

Ref Voltage

The *Ref Voltage* is based on the actual reference voltage that the bq29330 uses for reference when sending voltage readings to the bq20z90. Therefore this is a required constant in all the bq20z90 voltage computation formulas for displaying individual cell voltages (***Cell Voltage 1-4***) and the computed battery voltage (***Voltage***) in millivolts. By tweaking this value before it is used in the voltage computation formulas, then the errors introduced by the bq20z90 ADC and bq29330 reference are canceled out before they affect the reported voltages.

Normal Setting:*Ref Voltage* should never need to be modified by the user. It is modified by the voltage calibration command in Calibration mode. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of gas Gauges* application note SLUA379 for more information

AFE Corr

The AFE gain varies slightly as a function of in the input voltage. This variation is relatively constant and predictable so *AFE Corr* is used to correct for this common mode gain error of the input voltage.

Normal Setting: This register will only need to be changed under special circumstances. Its default setting is 1288. It is not modified by calibration commands.

AFE Pack Gain

The *AFE Pack Gain* is used for calibrating out errors in the bq29330 reference and bq20z90 ADC. It is used for reporting the ***Pack Voltage*** as measured on the PACK pin of the bq29330. Therefore, this is a required constant in all the bq20z90 voltage computation formulas for displaying ***Pack Voltage*** in millivolts. By tweaking this value before it is used in the voltage computation formulas, then it changes the gain of the reported voltage which gives a method for calibrating this reported voltage.

Normal Setting: AFE Pack Gain may not need to be calibrated depending on the application. Unless ***Pack Voltage*** is used for display by the application then it will only be used for charger detection, and it does not need to be accurate for function. *AFE Pack Gain* should never need to be modified by the user. It is modified by the pack voltage calibration command in Calibration mode. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of gas Gauges* application note SLUA379 for more information.

CC Offset

There are 2 offsets for calibrating the offset of the internal Coulomb Counter, board layout, sense resistor, copper traces and other offsets from the Coulomb Counter readings. *CC Offset* is the calibration value that primarily corrects for the offset error of the bq20z90 Coulomb Counter circuitry. The other offset calibration is *Board Offset* described below. To minimize external influences when doing *CC Offset* calibration either by either automatic *CC Offset* calibration or by the *CC Offset* calibration function in Calibration Mode an internal short is places across the SR1 and SR2 pins inside the bq20z90. *CC Offset* is a correction for very small noise/errors; therefore, to maximize accuracy it takes about 20 seconds to calibrate out the offset. Since it is not practical to do a 20 second offset during production, 2 different methods for calibrating CC Offset were developed.

1. The first method is to calibrate CC Offset by the putting the bq20z90 in Calibration Mode and initiating the CC Offset function as part of the entire bq20z90 calibration suite. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of gas Gauges* application note SLUA379 for more information on the Calibration Mode. This is a short calibration that is not as accurate as the second method described below. Its primary purpose is to calibrate CC Offset enough so it will not affect any other Coulomb Counter calibrations. This is only intended as a temporary calibration because the automatic calibration described below is done the first time SMBus is low for more than 20 seconds which is a much more accurate calibration.
2. During normal Gas Gauge Operation (***Temperature*** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*) when the SMBus clock and data lines are low for more than *Bus Low Time* seconds and ***Current*** is less than *Sleep Current* in milliAmps then an automatic *CC Offset* calibration is performed. This takes around 16 seconds and is much more accurate than the method in Calibration mode.

Normal Setting: *CC Offset* should never be modified directly by the user. It is modified by the current calibration function from Calibration Mode or by Automatic Calibration. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of gas Gauges* application note SLUA379 for more information for more information on calibration.

Board Offset

Board Offset is the second offset register. Its primary purpose is to calibrate all that the *CC Offset* does not calibrate out. This includes board layout, sense resistor and copper trace and other offsets that are external to the bq20z90 IC. The simplified ground circuit design in the bq20z90 requires a separate board offset for each tested device. The bq20z90 board offset calibration is explained in the SLUA379.pdf application note.

Normal Setting: This value needs to be modified for each device being tested unlike the bq20z90. Refer to the latest calibration application note for the bq20z90 (SLUA379: *Data Flash Programming and Calibrating the bq20z70 and bq20z90 Family of Gas Gauges*) for more information on calibration.

Int Temp Offset

The bq20z90 has a temperature sensor built into the IC. The *Int Temp Offset* is used for calibrating out offset errors in the measurement of the reported ***Temperature*** if the internal temperature sensor is used. The gain of the internal temperature sensor is accurate enough that a calibration for Gain is not required.

Normal Setting:*Int Temp Offset* should never need to be modified by the user. It is modified by the internal temperature sensor calibration command in Calibration mode. *Int Temp Offset* should only be calibrated if the internal temperature sensor is used. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of Gas Gauges* application note SLUA379 for more information on calibration.

Ext1 Temp Offset

Ext1 Temp Offset is for calibrating the offset of the thermistor connected to the TS1 pin of the bq20z90 as reported by ***Temperature***. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting:*Ext1 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext1 Temp Offset* should only be calibrated if a thermistor is connected to the TS1 pin of the bq20z90. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of Gas Gauges* application note SLUA379 for more information on calibration.

Ext2 Temp Offset

Ext2 Temp Offset is for calibrating the offset of the thermistor connected to the TS2 pin of the bq20z90 as reported by ***Temperature***. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting: *Ext2 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext2 Temp Offset* should only be calibrated if the a thermistor is connected to the TS1 pin of the bq20z90. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of Gas Gauges* application note SLUA379 for more information on calibration.

Config

These are all setting for adjusting Calibration Mode applied voltage, current, and temperature as well as the times associated with these calibrations. The Times should not need to be modified with normal applications. The values in Data Flash for these registers are defaults for Calibration Mode. If no other values are assigned to the calibration commands associated with each of these registers when in Calibration Mode then these default values is used. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of Gas Gauges* application note SLUA379 for more information on calibration.

CC Current

This register holds the default current that is applied during the calibration process while in Calibration mode. If, while in calibration mode, the *CC Current* is not modified by calibration command then this value is what is used to calibrate *CC Gain* and *CC Delta*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z90.
Normal Setting: This depends on the sense resistor used. Higher currents increase the voltage across the SR1 and SR2 pins which decreases noise and offset errors. It also increases the calibration accuracy because the granularity has less effect on the measurements. Good numbers for a 10 milliohm sense resistor are 2 to 3 amps.

Voltage Signal

This register holds the default voltage that is applied during the calibration process while in Calibration Mode. If, while in calibration mode, the *Voltage Signal* is not modified by calibration command then this value is what is used to calibrate *Reference Voltage* and *AFE Pack Gain*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z90. This value is a pack voltage, not a cell voltage.
Normal Setting: This depends on the number of cells, but it is good idea to use a voltage that is within the normal operating voltages of the cells used in the application times the number of cells.

Temperature Signal

This register holds the default Temperature that is applied during the calibration process while in Calibration Mode. If, while in calibration mode, the *Temperature Signal* is not modified by calibration command then this value is what is used to calibrate all the Temperature inputs that are used in this application. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z90.
Normal Setting: This value more than any of the others must be modified using the calibration commands in Calibration Mode instead of using this Data Flash location because temperature is continually changing.

CC Offset Time

CC Offset Time is the time that the calibration command for initiating a *CC Offset* calibration will take to do a *CC Offset* calibration. This is also used in Board Offset calibration in the bq20z90 EV software.
Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function rounds the *CC Offset Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Remember that this is only a temporary calibration to minimize offset effects on other CC calibrations. The Automatic Offset calibration that happens during normal Gas Gauging mode does a more accurate calibration. It is important to note that this is also used by the bq20z90 EV software to do Board Offset calibration. It is a good idea to increase this number to 20,000 to get a very accurate board offset measurement for production testing (see *Board Offset*) .

ADC Offset Time

ADC Offset Time is the time that the calibration command for initiating an ADC Offset calibration takes for an ADC Offset calibration. *ADC Offset* is not associated with a Data Flash location, but it is done every time Automatic *ADC Offset* is done in Gas Gauging mode and should be initiated at the same time as *ADC Offset* when in Calibration Mode.
Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the *ADC Offset Time* down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It reports a calibration error if a value less than 32 is used. Remember that this is only a temporary calibration. The Automatic Offset calibration that happens during normal Gas Gauging mode keeps this value accurate.

CC Gain Time

CC Gain Time is the time that the calibration command for initiating a CC Gain calibration takes for a *CC Gain Time* calibration. It uses the value in *CC Current* over *CC Gain Time* to do the calibration.
Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function will round the *CC Gain Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Depending on the current used, it is possible that 250 ms not enough time for a good calibration . It is recommended that 500 ms to 1000 ms be used for best results.

Voltage Time

Voltage Time is the time that the calibration commands for initiating a Reference Voltage or *AFE Pack Gain* calibration takes for a *Reference Voltage* or *AFE Pack Gain* calibration. These commands use the value in *Voltage Signal* over *Voltage Time* to do the calibration.
Normal Setting: The default is 1984 and the units are in milliseconds. Only use values in multiples of 1984 ms. The calibration function will round the *Voltage Time* down to the next lower multiple of 1984 ms if an exact multiple of 1984 is not used. It will report a calibration error if a value less than 1984 is used.

Temperature Time

Temperature Time is the time that the calibration commands for initiating any of the 3 temperature calibrations takes for the respective calibrations. These commands uses the value in *Temperature Signal* over *Temperature Time* to do the calibration.
Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the *Temperature Time* down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It will report a calibration error if a value less than 32 is used.

Cal Mode Timeout

Cal Mode Timeout is the maximum amount of time allowed for all calibrations to complete before the bq20z90 reverts to Gas Gauge mode automatically. The timer for this function starts when the ***Call Mode*** command is initiated.
Normal Setting: The purpose of this function is ensure that the bq20z90 has the ability to get out of Calibration Mode on its own if it was accidentally put into Calibration Mode for any unknown reason. The default for this register is 300 which is in units of seconds. This translates to 5 minutes. It is unlikely that this register will need to be modified.

Temp Model

None of these registers must not be changed for any reason. The only reason these values are listed is for the purpose of using a different thermistor; however, this is not recommended, and has not been tested with the bq20z90 at the time this was written.

Ext Coef 1, Ext Coef 2, Ext Coef 3, Ext Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Ext Min AD

This is the minimum ADC value allowed for the Temperature conversion formula.
Normal Setting: This value is 0 and should not be changed.

Ext Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.
Normal Setting: This value is 4012 and should not be changed.

Int Coef 1, Int Coef 2, Int Coef 3, Int Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Int Min AD

This is the minimum ADC value allowed for the Temperature conversion formula. Normal Setting: This value is 0 and should not be changed.

Int Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.
Normal Setting: This value is 4012 and should not be changed.

Current

Filter

This constant defines the filter constant used in the ***Average Current*** formula. This is a very common question how this is calculated. The formula used to compute ***Average Current*** is :

New (***Average Current***) = A $\times$ *Old* (***Average Current***) + (1-A) $\times$ ***Current***

A = *Filter*/256. Default value is 239

The time constant = 1 sec/ln(1/a) (default 14.5 sec)
Normal Setting: It is unlikely that this value should ever need to be changed.

Deadband

The purpose of the *Deadband* is to create a filter window to the reported ***Current*** register where the current is reported as 0. Any negative current above this value or any positive current below this value is displayed as 0.
Normal Setting: This defaults to 3 mA. There are not many reasons to change this value. Here are a few.

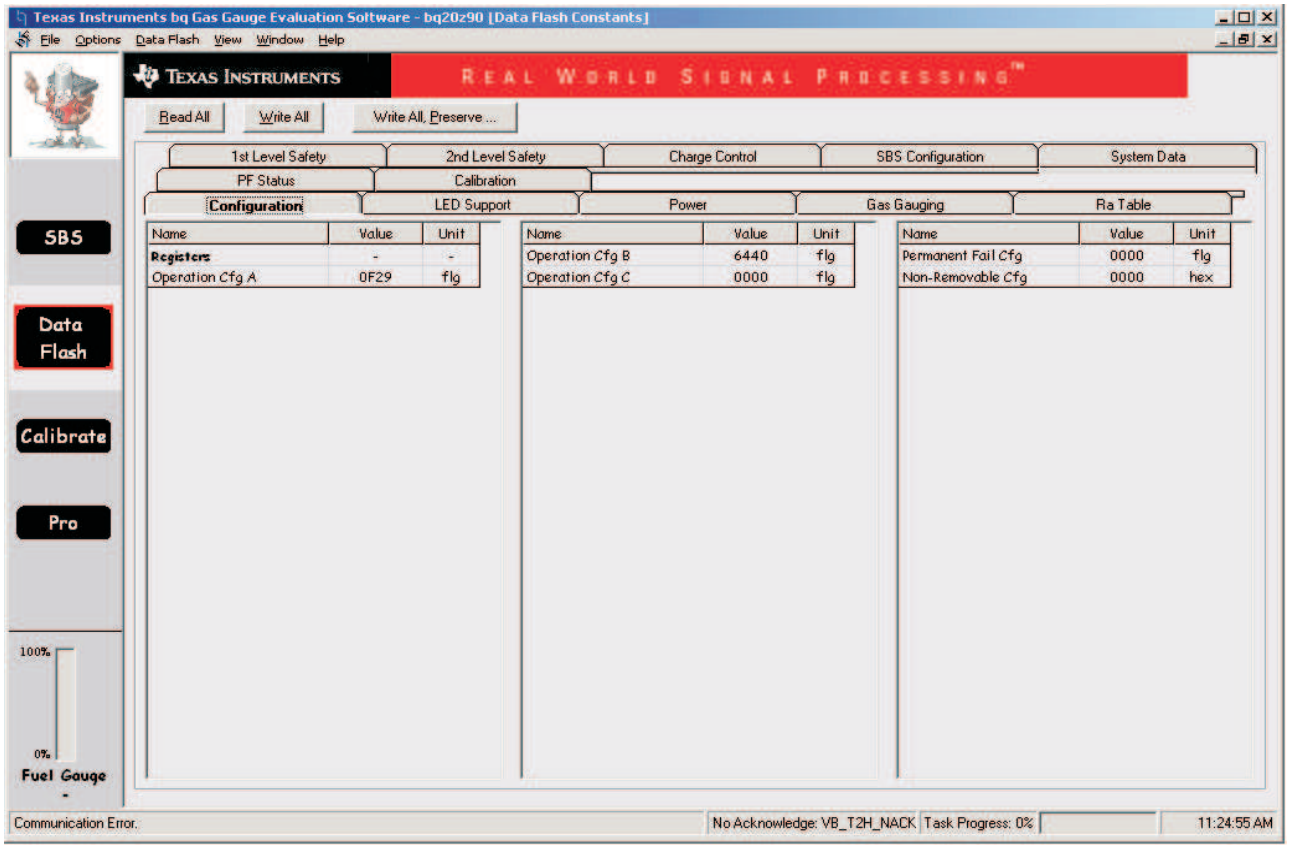
1. If the bq20z90 is not calibrated.
2. *Board Offset* has not been characterized.
3. If the PCB layout has issues that cause inconsistent board offsets from board to board.
4. An extra noisy environment in conjunction with number 3.

If this value must be modified be sure and verify the CC Deadband as well.

CC Deadband

This is also referred to as Digital Filter. This works much in the same way as the *Deadband* except it works for capacity counting on the ***Remaining Capacity*** register. Any absolute voltage between SR1 and SR2 below this value does not contribute to capacity measurement. The purpose of this is to minimize the possibility of unwanted noise from being counted towards capacity.
Normal Setting: The default for this register is 10 microvolts. This value is too small for noisy applications. For noisy applications, a better value would be more like 2 or 3 times this default. Unlike *Deadband* this value is not influenced by what value of sense resistor is used since this value is stored in microvolts and not milliamps.

2.9 Configuration



Registers

Operation Cfg A

This register is used to enable or disable various functions on the bq20z90. These bits are continued in *Operation Cfg B*.

LEDR	LEDRCA	CHGLED	DMODE	LED1	LED0	CC1	CC0
—	—	SLEEP	TEMP1	TEMP0	SLED	ZVCHG1	ZVCHG0

- LEDR [15]: This bit is useful to watch for device resets. If enabled, it activates the LED display with the present ***RSOC*** state after a reset has occurred. LEDs operates exactly the same as a DISP button transition function (See **LED Support** class).
  - 0: LEDs do not illuminate on reset
  - 1: LEDs illuminate in the same manner as a DISP button press after a reset has occurred.

  Normal Setting: This bit defaults to a 0 which should be used in production. This bit should normally only be set during development.
- LEDRCA [14]: If enabled, this bit forces the bq20z90 to force the LEDs to flash with a period of (2 ×*LED Flash Rate*) whenever [RCA] is set in ***Battery Status*** and the LEDs are activated. In Discharge Mode ([DSG] flag clear in ***Battery Status***), a transition from high to low on the DISP pin of the bq2z80 (DISP button transition) is required to activate the LEDs. During Charge ([DSG] flag clear in ***Battery Status***), if [CHGLED] set in *Operation Cfg A*, then DISP button transition is not required because the LEDs are activated (See **LED Support** class).
  - 0: LEDs do not flash at the *LED Flash Rate* period with [RCA] set in ***Battery Status***.
  - 1: LEDs do flash at (2 ×*LED Flash Rate*) period with [RCA] set in ***Battery Status*** if activated.

  Normal Setting: This bit defaults to a 0. It is set based on user preference.
- CHGLED [13]: If enabled, this bit forces the bq20z90 to activate the LED display whenever charging (***Current*** greater than *CHG Current Threshold*). LEDs operate exactly the same as a DISP button transition function except they do not time out and deactivate until ***Current*** is less than *CHG Current Threshold*. (See **LED Support** class)
  - 0: LEDs do not illuminate on reset
  - 1: LEDs illuminate in the same manner as a DISP button press.

  Normal Setting: This bit defaults to a 0. It is set based on user preference.
- DMODE [12]: This is the Display Mode bit which refers to LED configuration. If the Display mode bit is 0, then the display is in “Relative Mode”. If it is 1, then it is in “Absolute Mode”. In relative mode, the LED display is based on a percentage of the ***Full Charge Capacity***, which is stored in the ***RSOC*** register. If it is in absolute mode, then the LED display is based on a percentage of ***Design Capacity***, which is stored in the ***ASOC*** register.
  - 0: Number of LEDs that illuminated when activated are based on ***RSOC***.
  - 1: Number of LEDs that illuminated when activated are based on ***ASOC***.

  Normal Setting: This bit defaults to a 0 which is Relative Mode. This is the most common mode that customers use. It is important to note that ***ASOC*** can be greater than 100%. The LEDs treat any ***ASOC*** greater than 100% as 100%
- LED1, 0 [11, 10]: These bits are used to inform the bq20z90 of the number of LEDs that are being used in the application.
  - 1,1 = 5 LEDs
  - 1,0 = 4 LEDs
  - 0,1 = 3 LEDs
  - 0,0 = This is for a user defined setting as set in the **LED Support** class.

  Normal Setting: The default setting for these bits is both bits set. This is based on user preference and application.
- CC1,0 [9,8]: These bits are used to inform the bq20z90 of the number of Li-Ion battery cells in a series for the application. This setting is critical for every aspect of the Data Flash configuration with regards to voltage based functions.
  - 1,1 = 4 series cell application

– 1,0 = 3 series cell application
– 0,1 = 2 series cell application
– 0,0 = Reserved (Not Valid)

Normal Setting: The default value for these bits are both set for a 4-series cell application. These bits are application and user dependant.

- RESERVED [7,6]: These bits are reserved
- SLEEP [5]: This bit enables or disables the ability to go to sleep when SMBus Clock and Data lines go low for *Bus Low Time* and ***Current*** is below *Sleep Current* (See *Sleep Current* and *Bus Low Time*)
  – 0: bq20z90 do not go to sleep with the above criteria
  – 1: bq20z90 do go to sleep when the sleep criteria is set

  Normal Setting: This bit defaults to a 1 which should be used in most applications. There are few reasons for this bit to be set to 0.
- Temp1,0 [4,3]: These bits are used to tell the bq20z90 the temperature sensor configuration. The bq20z90 can use up to 2 external sensors and there is also an internal sensor available if needed. All of these sensors are able to use various configurations to report temperature in the ***Temperature*** register.
  – 1,1 = The Average of TS1 and TS2 external inputs are used to generate ***Temperature***.
  – 1,0 = Greater Value of TS1 and TS2 external inputs are used to generate ***Temperature***.
  – 0,1 = Only Temperature sensor TS1 is used to generate ***Temperature***.
  – 0,0 = Only internal temperature sensor is used to generate ***Temperature***.

  Normal Setting: The default setting for these bits is [Temp1] cleared and [Temp0] set. This requires one external temperature sensor on TS1. The bq20z90 default configuration is for a Semitec 103AT thermistor as briefly described in the **Temp Model** subclass (See **Temp Model**). The internal temperature sensor is slightly less accurate than using a Semitc 103AT and is not recommended. It also is not as accurate because it cannot be put as close to the battery cells in the application as can be done with an external thermistor.
- SLED [2]: The serial LED option can be used to implement a much brighter display at the expense of additional hardware components. With the parallel connection, the 3.3 V output from the bq29330. is used to power the LEDs. Using that approach, current in each LED should be limited to 3 mA. With the serial option, all LEDs can be powered from the battery voltage and driven in series through a simple constant current regulator. The current is then diverted to ground at the various nodes between the series LEDs in order to program the desired pattern. If this function is enabled, then the Permanent Failure display mode using the LEDs is disabled. (See *Operation Cfg B*). The 2 options for this bit are:
  – 0: Parallel LED configuration
  – 1: Serial LED Configuration

  Normal Setting: This bit defaults to a 0 which should be used in production for most applications. Given that serial LEDs require more components and 3 mA is usually sufficient for most applications then 0 is the most common setting for this bit.
- ZVCHG1,0 [1,0]: These bits are also known as Pre-Charge 1,0. These bits are used to tell the bq20z90 how the Pre-Charge circuit is configured in the application. It tells the bq20z90 what pin on the bq29330 to use for Pre-Charge functions when required.
  – 1,1 = No action is taken in Pre-Charge functions with this setting.
  – 1,0 = OD pin is used for Pre-Charge functions.
  – 0,1 = Charge FET is used for Pre-Charge functions.
  – 0,0 = ZVCHG FET is being used for Pre-Charge functions.

  Normal Setting: If using a separate Pre-Charge FET it is recommended not to use the OD pin for this function because it does not have good “zero volt charging” capabilities when a battery is completely dead. Therefore, the ZVCHG pin should be used because it has excellent clamping abilities. The default is for using the Charge FET pin on the bq29330.

Operation Cfg B

This register is used to enable or disable various functions on the bq20z90. This is a continuation of *Operation Cfg A*.

PFD1	PFD0	RESCAP	NCSMB	NRCHG	CSYNC	CHGTERM	CCT
CHGSUP	OTFET	CHGFET	CHGIN	NR	CPE	HPE	BCAST

- PFD1,0 [15,14]: These bits are used to configure how the bq20z90 is supposed to display permanent failure data through the LEDs if enabled. If [SLED] set in *Operation Cfg A* then this function is disabled. If there is no permanent failure, then no action is taken on the LEDs even if this function is enabled.
  - 1,1 = Permanent Failure data is displayed on the LEDs after the LEDs display the state of charge data (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) when the DISP button is activated. The DISP button does not have to be activated for more than *LED Hold Time*.
  - 1,0 = Permanent Failure data is disabled with this setting
  - 0,1 = Permanent Failure data is displayed on the LEDs after the LED display indicates the SOC data (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*), but only if DISP button is activated for more than *LED Hold Time*.
  - 0,0 = Permanent Failure display is disabled with this setting

  Normal Setting: The default setting here is [PFD1] cleared and [PFD0] set. This gives the ability to get permanent failure data from a damaged battery pack even if communications are not possible as long as the bq20z90 CPU is still functioning.
- RESCAP [13]: The bq20z90 reports ***Remaining Capacity*** and ***Full Charge Capacity*** that is falsely lower than the actual capacity of the battery as defined by the *Reserve Cap-mAh* in mAh mode or *Reserve Cap-mW* in mWh mode (configured by [CAPM] in ***Battery Mode***). RESCAP sets a load compensation for this function.
  - 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
  - 1: If set to a 1, then a more normal rate of load compensation as defined by Load Select is applied to this reserve capacity. (See **IT Cfg** class)

  Normal Setting: This bit defaults to a 1. For most applications, this along with *Load Select* should be left at the default values.
- NCSMB [12]: This bit is used to enable a special mode for the SMBus engine in the bq20z90 where it allows for unlimited timeouts for SMBus communications more like I^2C. This mode was made for customers that were using older legacy parts that had longer timeouts and were not SMBus compliant.
  - 0: Timeout extension is disabled.
  - 1: Unlimited Timeout extension enabled.

  Normal Setting: The default for this register is 0. It is recommended that this always be set to 0. There have been many complications with customers using this function in the past. When set to a 1, it is important to note that if clocking in data with a SMBus read command and the communication gets interrupted with data low then data can be stuck low until more clocks are sent to finish the communication.
- NRCHG [11]: This bit is used to configure whether or not the bq20z90 turns off the Charge FET when it goes to Sleep if [NR] bit is set in Operation Cfg B. If [NR] cleared then this bit is not used.
  - 0: Charge FET turns off in sleep mode as long as the bq20z90 is setup with [NR] set.
  - 1: Charge FET remains on in sleep mode with the [NR} bit set.

  Normal Setting: This bit defaults to a 0 which should be used for most applications with [NR] set. This could be a problem for some applications that expect the battery to start charging immediately when charge is applied when asleep.
- CSYNC [10]: This bit is used in the Primary Charge Termination Algorithm (See *Maintenance Current*). When this bit is set, then with a Primary Charge Termination the bq20z90 writes the ***Remaining Capacity*** to ***Full Charge Capacity***
  - 0: ***Remaining Capacity*** is not written up to ***Full Charge Capacity*** on Primary Charge Termination.
  - 1: ***Remaining Capacity*** is written up to ***Full Charge Capacity*** on Primary Charge Termination.

  Normal Setting: The default setting for this bit is 1. This should be used for most applications to ensure that the Remaining Capacity starts from ***Full Charge Capacity*** when the charger terminates charging. This is a synchronization function to ensure the bq20z90 discharges from full when it has been determined that the battery is full.
- CHGTERM [9]: This bit enables the ability for the bq20z90 to turn off [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination is detected and then ***Current*** falls below the *Chg Current*

Threshold for 2 consecutive periods of *Taper Current Window*.

- 0: bq20z90 does not clear [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination.
- 1: bq20z90 does clear [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination.

Normal Setting: This bit defaults to 0. This should be acceptable for most applications.

- CCT [8]: This bit configures which method the bq20z90 will use for incrementing ***Cycle Count***.
  - 0: If set to 0, then the bq20z90 increments ***Cycle Count*** by 1 with every cumulative discharge of *Cycle Count Threshold* in mAh. This discharge does not have to be consecutive. The bq20z90 accumulates all discharge current for this calculation even when broken up by periods of charge.
  - 1: if set, then when the bq20z90 accumulates enough discharge capacity equal to (*CC%*×*FCC*) then it increments *Cycle Count* by 1.

  Normal Setting: This bit defaults to a 0. This setting is application specific.
- CHGSUSP [7]: This bit enables the ability to turn off the Charge FET and/or Pre-Charge FET in charge suspend mode (See **Charge Control** Class).
  - 0 = The Charge FET is unaffected by any type of charge suspension.
  - 1 = The Charge FET and/or Pre-Charge FET are opened with any charge suspension.

  Normal Setting: the default setting for this bit is 0. It is common for this to be set to 1 to give the bq20z90 the control for additional protection.
- OTFET [6]: This bit is used to configure how the bq20z90 controls the current FETs (Charge or Discharge) during *Over Temp Chg* or *Over Temp Dsg* faults. (See *Over Temp Chg* and *Over Temp Dsg*)
  - 0: FET control is unaffected by any *Over Temp Chg* or *Over Temp Dsg* faults.
  - 1: During a *Over Temp Chg* fault the Charge FET is opened. During a *Over Temp Dsg* fault the Discharge FET is opened.

  Normal Setting: This bit defaults to a 1 which should be used in production for most applications. Over temperature conditions can be dangerous and every level of protection possible should be used.
- CHGFET [5]: This bit is used to configure how the bq20z90 controls the Charge FETs when [TCA] gets set in ***Battery Status***. (See *TCA Set* % for an explanation for when [TCA] gets set).
  - 0: Charge FET is unaffected anytime [TCA] gets set.
  - 1: Charge FET is turned off anytime [TCA] gets set.

  Normal Setting: This bit defaults to a 0 which should be used in production for most applications. Setting it to a 1 turns the Charge FET off is only if *Maintenance Current* is set to 0.
- CHGIN [4]: This bit is used to configure how the bq20z90 controls the Charge FETs when in charge inhibit mode. (See *Chg Inhibit Temp Low* and *Chg Inhibit Temp High*).
  - 0: Charge FET is unaffected when in charge inhibit mode.
  - 1: Charge FET is turned off when in charge inhibit mode.

  Normal Setting: This bit defaults to a 0 which should be acceptable for most applications. It is important to note that this is different than charge suspend mode because this inhibits the charge cycle from occurring. This function acts while discharging.
- NR [3]: Use this bit to configure the bq20z90 for either a removable or a non removable battery pack. A removable pack uses the System Present pin (PRES) and a nonremovable pack does not. This affects many functions in the bq20z90. Primarily it affects the way it handles recovery methods of most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register is used to enable many nonremovable pack fault recovery methods for use with a removable pack. (See *NR Config* and **Current** subclass in **1st Level Safety** class)
  - 0: Configures battery for removable mode. Transition on System Present pin (PRES) triggers certain recovery functions. *NR Config* can be used to enable nonremovable functions for this mode as well
  - 1: Configures battery for nonremovable mode.

  Normal Setting: Default for this bit is application specific. Set to 0 for batteries that are removed, and use the PRES pin. Set to 1 for packs that do not use the PRES pin.
- CPE [2]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z90 broadcasts to the SMBus Device Address 0x12 (SMBus charger device address) (See SBS and SMBus specification that can be downloaded from the web).

– 0: No PEC byte is sent to SMBus Device Address 0x12.
– 1: Every broadcast from the bq20z90 to SMBus Device Address 0x12 includes a PEC byte as the last byte sent.

Normal Setting: If a smart charger (SMBus Device Address 0x12) is used that is PEC capable, then this should be set to a 1. It is always recommended to use PEC when possible.

- HPE [1]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z90 broadcasts to the SMBus Device Address 0x14 (SMBus Host device address)
  – 0: No PEC byte is set to SMBus Device Address 0x14. (See SBS and SMBus specification that can be downloaded from the web)
  – 1: Every broadcast from the bq20z90 to SMBus Device Address 0x14 includes a PEC byte as the last byte sent.

  Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.
- BCAST [0]: This bit enables or disables Master Mode Message broadcasting periodically to a smart charger or host. The bq20z90 broadcasts are completely disabled. (See SBS and SMBus specification that can be downloaded from the web).
  – 0: The bq20z90 never masters the SMBus for any reason.
  – 1: The bq20z90 is enabled to Master the bus periodically to inform a host or charger of critical information

  Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.

Operation Cfg C

This register is used to enable or disable various functions on the bq20z90. This is a continuation of *Operation Cfg B*.

–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	RSOCL

- RSOCL[0]: This bit is used to modify the functionality of RSOC at 100%
  – 1 = When set to 1 then ***RSOC*** will only be written to 100% if there is a primary charge termination (see *Taper Current* for more information on primary charge termination). At no other time will ***RSOC***
  – 0 = When set to 0 then ***RSOC*** at 100% will function like every other percentage for RSOC. When it reaches 99% then any fraction above 99% in the ***RSOC*** computation will force ***RSOC*** to be written to 100%.

  Normal Setting: This function is very application specific. Some customers have requested that they do not want ***RSOC*** to be 100% under any circumstances unless the bq20z90 detects a full condition. If this is a requirement then consider setting this to a 1.

Permanent Fail Cfg

This enables or disables the various permanent failure protection functions ability to activate the SAFE outputs ($\overline{\text{SAFE}}$ and SAFE pins) or not when the function is triggered.

–	–	–	XSOPT	XSOCD	XSOCC	XAFE_P	XAFE_C
XDFF	XDFETF	XCFETF	XCIM	XSOTD	XSOTC	XSOV	XPFIN

- RESERVED [15–13]: These bits are reserved.
- XSOPT [12]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an Open Thermistor failure condition. With this function enabled, the bq20z90 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high, and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Chg*)
  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a an Open Thermistor failure condition
  – 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for an Open Thermistor failure condition

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing

of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOPT] be set for production packs to protect against hazardous failures.

- XSOCD [11]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Current in the discharge direction condition. With this function enabled, the bq20z90 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Chg*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Current in the discharge direction Condition
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a Safety Over Current in the discharge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOCD] be set for production packs to protect against hazardous failures.
- XSOCC [10]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Current in the charge direction condition. With this function enables the bq20z90 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Dsg*).
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Current in the charge direction Condition
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a Safety Over Current in the charge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOCC] be set for production packs to protect against hazardous failures.
- XAFE_P [9]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a periodic AFE verification failure. With this function enabled, the bq20z90 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *AFE Check Time*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a periodic AFE verification failure.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a periodic AFE verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XAFE_P] be set for production packs to protect against hazardous failures.
- XAFE_C [8]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an AFE communication verification failure. With this function enabled the bq20z90 will also write 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *AFE Fail Limit*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for an AFE communication verification failure.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for an AFE communication verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XAFE_C] be set for production packs to protect against hazardous failures.

- XDFF [7]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Data Flash verification failure. With this function enabled, the bq20z90 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *PF Flags 1*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Data Flash verification failure.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a Data Flash verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFF] be set for production packs to protect against hazardous failures.
- XDFETF [6]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Discharge FET Failure condition . With this function enabled, the bq20z90 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *FET Fail Limit*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Discharge FET Failure Condition.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a Discharge FET Failure Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFETF] be set for production packs to protect against hazardous failures.
- XCFETF [5]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Charge FET Failure condition . With this function enabled, the bq20z90 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *FET Fail Limit*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Charge FET Failure Condition.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a Charge FET Failure Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCFETF] be set for production packs to protect against hazardous failures.
- XCIM [4]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a extreme Cell Imbalance condition . With this function enabled, the bq20z90 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *Cell Imbalance Fail Voltage*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a extreme Cell Imbalance Condition.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a extreme Cell Imbalance Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCIM] be set for production packs to protect against hazardous failures.
- XSOTD [3]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Temperature in the discharge direction condition. With this function enabled, the bq20z90 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOT Chg*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over

Temperature in the discharge direction Condition.

– 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a Safety Over Temperature in the discharge direction Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOTD] be set for production packs to protect against hazardous failures.

- XSOTC [2]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Temperature in the charge direction condition . With this function enabled, the bq20z90 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOT Chg*)
  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Temperature in the charge direction Condition.
  – 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a Safety Over Temperature in the charge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOTC] be set for production packs to protect against hazardous failures.
- XSOV [1]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Voltage condition . With this function enabled, the bq20z90 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOV Threshold*).
  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Voltage Condition.
  – 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a Safety Over Voltage Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOV] be set for production packs to protect against hazardous failures.
- XPFIN [0]: This bit enables the ability for the bq20z90 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a PFIN input low condition . With this function enabled, the bq20z90 writes 0x3672 in the Fuse Flag to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *PFIN Detect Time*)
  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a PF input low Condition.
  – 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z90. The *Fuse Flag* is written to 0x3672 for a PF input low Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XPFIN] be set for production packs to protect against hazardous failures.

Non-Removable Cfg

This register affects the way the bq20z90 handles recovery methods for most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register can be used to enable many nonremovable pack fault recovery methods for use with a removable pack. NR Config can be used to enable nonremovable fault recovery functions for a battery pack that is configured as removable.

–	–	OCD	OCC	OCD2	OCC2	–	–
–	–	OC	–	–	AOCD	SCC	SCD

- RESERVED [15, 14]: These bits are reserved
- OCD [13]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z90. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the discharge direction fault (See (OC*1st Tier) Dsg*).
  - 0: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is not enabled.
  - 1: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- OCC [12]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z90. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the charge direction fault (See *OC (1st Tier) Chg*).
  - 0: The nonremovable recovery option associated with *OC (1st Tier) Chg* is not enabled
  - 1: The nonremovable recovery option associated with *OC (1st Tier) Chg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- OCD2 [11]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z90. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with a second level Over Current in the discharge direction fault (See *OC (2nd Tier) Dsg*).
  - 0: The nonremovable recovery option associated with *OC (2nd Tier) Dsg* is not enabled.
  - 1: The nonremovable recovery option associated with *OC (2nd Tier) Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- OCC2 [10]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z90. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with a second level Over Current in the charge direction fault (See *OC (2nd Tier) Dsg*).
  - 0: The nonremovable recovery option associated with *OC (2nd Tier) Chg* is not enabled.
  - 1: The nonremovable recovery option associated with *OC (2nd Tier) Chg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- RESERVED [9-3]: These bits are reserved.
- AOCD [2]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z90. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE Over Current in the discharge direction fault (*AFE OC Dsg*).
  - 0: The nonremovable recovery option associated with *AFE OC Dsg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE OC Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- SCC [1]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z90. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the charge direction fault (*AFE SC Chg*).
  - 0: The non removable recovery option associated with *AFE SC Chg* is disabled.
  - 1: The non removable recovery option associated with *AFE SC Chg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- SCD [0]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z90. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the discharge direction fault (*AFE SC Dsg*).
  - 0: The nonremovable recovery option associated with *AFE SC Dsg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE SC Dsg* is enabled.

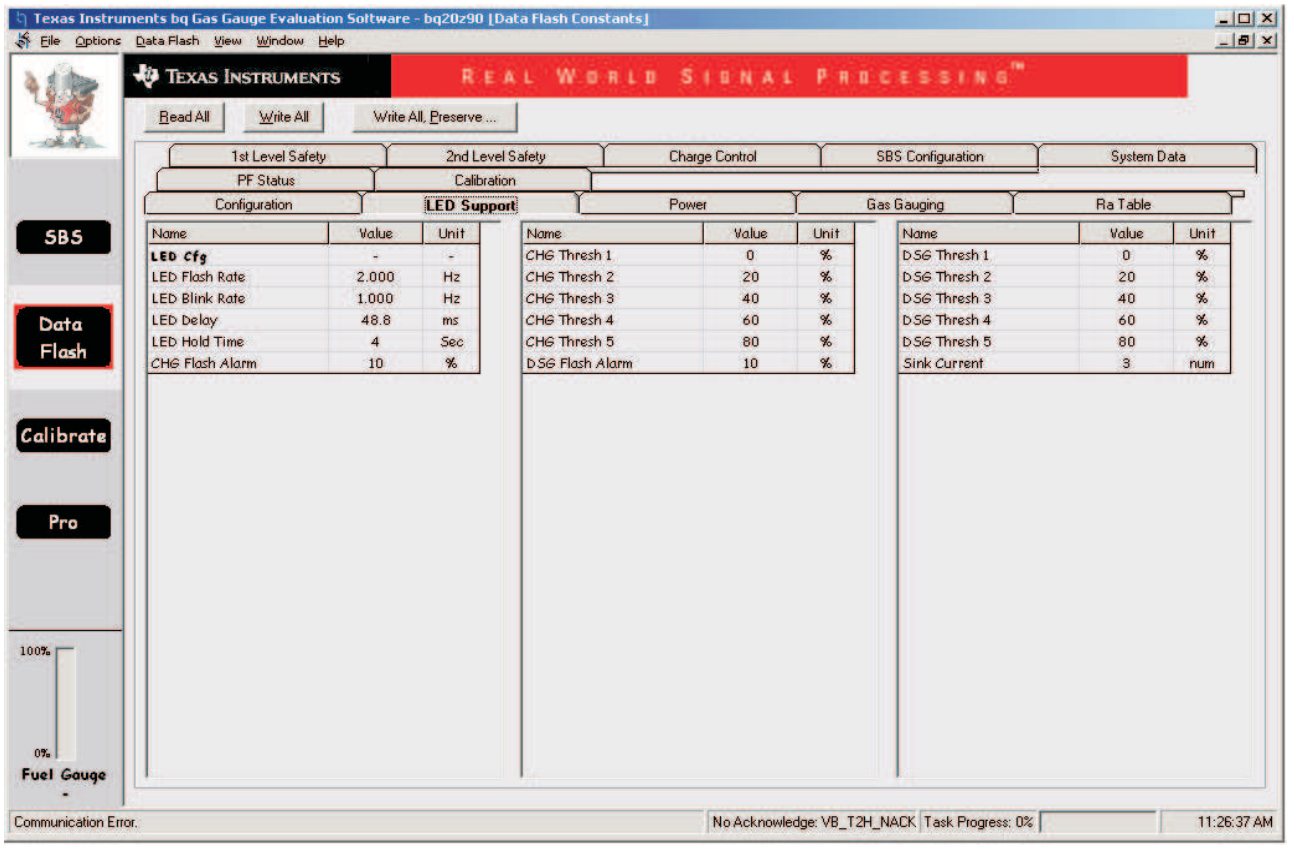
  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR]

cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

2.10 LED Support

There are 3 different display modes for the LEDs that need clarification to help understand the **LED Support** class.

- Blinking: When the display is said to be blinking, then the word “blinking” is used to refer to the LED located closest to the LED used to indicate 100% that is illuminated and “blinking” when the LED display is activated and displaying SOC (state of charge). Only this “topmost” activated LED in the display blinks. All other LEDs that are activated is steady state when activated. (see *LED Blink Rate*)
- Flashing: When the display is said to be flashing then the word “flashing” means all LEDs that are activated to indicate the SOC will flash with a period of (2 ×*LED Flash Rate*).
- Delay: When the display is activate, all LEDs that are required to indicate the SOC may not illuminate at the same time. Starting from the LED that represents the lowest SOC, there can be a delay (*LED Delay*) between each LED illuminating from the LED that represents the lowest possible SOC up to the LED that represents the present SOC.



LED Cfg

LED Flash Rate

LED Flash Rate is used to configure the periodic rate at which the activated LEDs flashes with a (2 ×*LED Flash Rate*) period and a 50% duty cycle when the LEDs are required to flash. Only the LEDs that are requested to illuminate based on SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) will flash. LEDs are Required to flash with the following conditions:

1. When Charging ([DSG] cleared in ***Battery Status***) with the following conditions:
   a. When [CHGLED] set in *Operation Cfg A*
      a. [LEDRCA] set in *Operation Cfg A*
      b. [RCA] set in ***Battery Status***
   b. High to low transition on the DISP pin (button press) with the following requirements:
      a. LEDRCA] set in *Operation Cfg A*
      b. [[RCA] set in ***Battery Status***
2. When Discharging ([DSG] set in ***Battery Status***) with a high to low transition on the DISP pin (button press) and the following conditions:
   a. LEDRCA] set in *Operation Cfg A*
   b. [RCA] set in ***Battery Status***

   Normal Setting: This setting depends on user preference however for most applications the default is acceptable. *LED Flash Rate* does not affect the operation of the part in any way except the display. The default is 2 and it is converted to units of Hertz by the EV Software.

LED Blink Rate

The bq20z90 can be configured to blink the topmost LED in the LED display at a rate stored in *LED Blink Rate* . When the LED display is activated, the topmost LED is the illuminated LED closest to the LED that is used to indicate 100% SOC. The topmost LED in the LED string will blink at a frequency denoted by *LED Blink Rate* period and a 50% duty cycle when charging ([DSG] cleared in ***Battery Status***) with the following conditions:

1. Charging (***Current*** > *Chg Current Threshold*) and [CHGLED] set in *Operation Cfg A*.
2. High to low transition on the DISP pin (button press)

This function is disabled (no blinking of topmost LED) if *LED Blink Rate* = 0.
Normal Setting: This setting depends on user preference however for most applications the default is acceptable. *LED Blink Rate* does not affect the operation of the part in any way except the display. The default is 1024 and is 1 and it is converted to units of Hertz by the EV Software.

LED Delay

The bq20z90 can be configured to put a delay in between the illumination of each LED segment during the display activation sequence. Upon request for activation of the LED display either by button press or charging, the LEDs ramps up to the topmost LED with a delay in between each LED illuminating in the sequence. The topmost LED is the illuminated LED that is closest to the LED that illuminates with 100% SOC when the LEDs are requested. If *LED Delay* = 0 then this function is disabled (no delay between LEDs illuminating).
Normal Setting: This setting depends on user preference however for most applications the default is acceptable. *LED Delay* does not affect the operation of the part in any way except the display. The default for this register is 100 in units of 500 micro seconds. So this would mean the default is 50 ms.

LED Hold Time

LED Hold Time defines the time that the LEDs remain active once all LEDs required to indicate the current SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) are active. When the request is registered, either by high to low transition on the DISP pin (button press) or charging, then the LED activation sequence is initiated then the LEDs must ramp up (see *LED Delay*) to all LEDs illuminating that are requested. When the ramp up completes, then an internal *LED Hold Time* timer is initiated. When the *LED Hold Time* timer expires, the LED display is deactivated.
Normal Setting: This setting depends on user preference however for most applications the default is acceptable. *LED Delay* does not affect the operation of the part in any way except the display. The default for this register is 4 seconds.

CHG Flash Alarm

The value in *CHG Flash Alarm* is only enabled if bits [LED1] and [LED0] in Operation Cfg A are set to "User" defined (both bits clear), otherwise this register is ignored. *CHG Flash Alarm* is used in an alternative method for alerting user to a low capacity condition. This function is completely independent of [LEDRCA] set in *Operation Cfg A*. This register is set as a function of SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*). This function only operates when charging. If SOC% is at or below the *CHG Flash Alarm* then the LEDs indicating the SOC% flashes at the *LED Flash Rate* with the following conditions:

1. When Charging ([DSG] cleared in ***Battery Status***) and [CHGLED] set in *Operation Cfg A* .
2. High to low transition on the DISP pin (button press)

Normal Setting: The default setting for this register is 10%. This should be acceptable for most applications.

CHG Thresh 1

The value in *CHG Thresh 1* is only enabled if bits [LED1] and [LED0] in Operation Cfg A are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in Battery Status) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 (The LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st LED segment is active with SOC% within 0% to *CHG Thresh 1*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 2*.

CHG Thresh 2

The value in *CHG Thresh 2* is only enabled if bits [LED1] and [LED0] in Operation Cfg A are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in ***Battery Status***) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1-5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 and LED 2 (The LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st and 2nd LED segments is active with SOC% above *CHG Thresh 1* and equal to or below *CHG Thresh 2*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 3*.

CHG Thresh 3

The value in *CHG Thresh 3* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in ***Battery Status***) for *CHG Thresh 1–5* to be available for LED requests, otherwise DSG Thresh 1-5 are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED2, and LED 3 (The 3rd LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st , 2nd, and 3rd LED segments is active with SOC% above *CHG Thresh 2* and equal to or below *CHG Thresh 3*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 4*.

CHG Thresh 4

The value in *CHG Thresh 4* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in ***Battery Status***) for CHG Thresh 1–5 to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED 2, LED 3 and LED 4 (The

4 LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, 3rd, and 4th LED segments is active with SOC% above *CHG Thresh 3* and equal to or below *CHG Thresh 4*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 5*.

CHG Thresh 5

The value in *CHG Thresh 5* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in ***Battery Status***) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 through LED 5 (The last LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then LED segments 1–5 is active with SOC% above *CHG Thresh 4*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers.

DSG Flash Alarm

The value in *DSG Flash Alarm* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. *Dsg Flash Alarm* is used in an alternative method for alerting user to a low capacity condition. This function is completely independent of [LEDRCA] set in *Operation Cfg A*. This register is set as a function of SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*). This function only operates when discharging ([DSG] set in ***Battery Status***). If SOC% is at or below the *Dsg Flash Alarm*, then the LEDs indicating the SOC% flashes at the *LED Flash Rate* with a high to low transition on the DISP pin (button press).
Normal Setting: The default setting for this register is 10%. This should be acceptable for most applications.

DSG Thresh 1

The value in *DSG Thresh 1* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 (The LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st LED segment is active with SOC% within 0% to *DSG Thresh 1*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 2*.

DSG Thresh 2

The value in *DSG Thresh 2* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 and LED 2 (The LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st and 2nd LED segments is active with SOC% above *CHG Thresh 1* and equal to or below *DSG Thresh 2*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 3*.

DSG Thresh 3

The value in *DSG Thresh 3* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED2, and LED 3 (The 3rd LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, and 3rd LED segments is active with SOC% above *CHG Thresh 2* and equal to or below *DSG Thresh 3*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 4*.

DSG Thresh 4

The value in *DSG Thresh 4* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED 2, LED 3 and LED 4 (The 4 LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, 3rd, and 4th LED segments is active with SOC% above *CHG Thresh 3* and equal to or below *DSG Thresh 4*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 5*.

DSG Thresh 5

The value in *DSG Thresh 5* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 through LED 5 (The last LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then LED segments 1–5 is active with SOC% above *DSG Thresh 4*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in Operation Cfg A are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers.

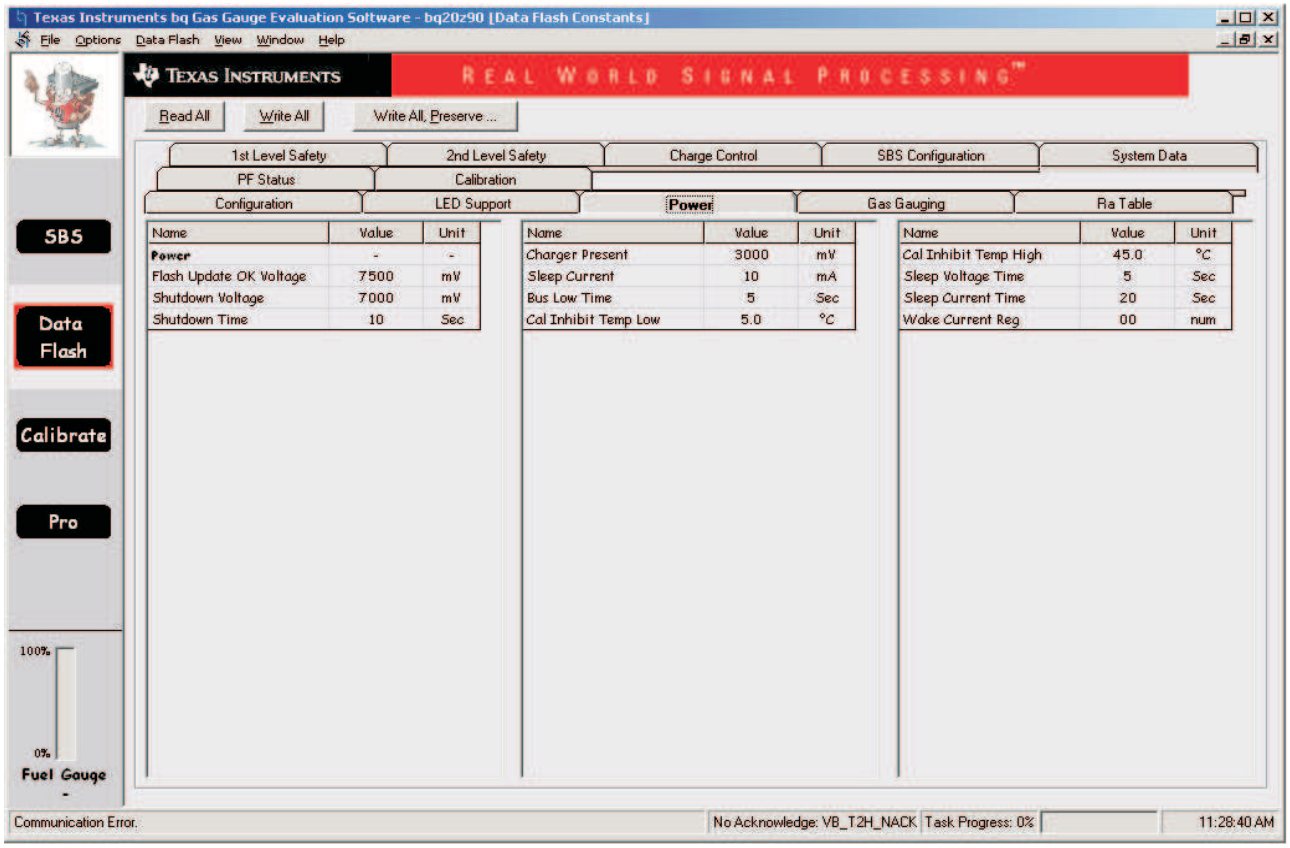
Sink Current

Sink Current is used to set the amount of current that is used to drive each LED segment. There are only 4 options.

SETTING	SINK CURRENT
0x00	0 mA
0x01	3 mA
0x02	4 mA
0x03	5 mA

Normal Setting: The Default setting for this register is 0x03 which is 5 milliamps. For most LEDs this should be acceptable.

2.11 Power



Power

Flash Update OK Voltage

This register controls one of several data flash protection features. It is very critical that data flash is not updated when the battery voltage is too low. Data Flash programming takes much more current than normal operation of the bq20z90/bq29330 chipset and with a depleted battery this current can cause the battery voltage to crater (drop dramatically) forcing the bq20z90 into reset before completing a data flash write. The effects of an incomplete Data Flash write can corrupt the memory resulting in unpredictable and extremely undesirable results. The voltage setting in *Flash Update OK Voltage* is used to prevent any writes to the data flash below this value. If a charger is detected then this register is ignored.

Normal Setting: The default for this register is 7500 millivolts. For 2-cell applications, this can cause production issues with writing to the data flash because at nominal cell voltages, 2-cell applications can easily be below 7500 millivolts. The way to solve this problem is to connect a charger voltage to the battery which overrides this register while connected. Ensure that this register is set to a voltage where the battery has plenty of capacity to support data flash writes but below any normal battery operation conditions.

Shutdown Voltage

The bq20z90 goes into shutdown mode when ***Voltage*** falls below the *Shutdown Voltage* for at least Shutdown Time seconds. Also ***Current*** must be less than 0 and the ***Pack Voltage*** must be less than *Charger Present* for the entire time. (See *Shutdown Time*)

Normal Setting: This voltage should be far below any normal operating voltage but above any threshold that can cause damage to the cells. This threshold is met after the Charge and Discharge FETs are turned off from an under voltage fault condition.

Shutdown Time

When the following conditions are met:

1. ***Voltage*** is below *Shutdown Voltage*.
2. ***Current*** is less than 0.
3. ***Pack Voltage*** less than *Charger Present*

Then the *Shutdown Time* timer is initiated. If the above conditions remain until the *Shutdown Time* timer expires, then the bq20z90 goes into shutdown mode. Every time the bq20z90 wakes up from shutdown mode, then the *Shutdown Time* timer is reset meaning it is not possible for the bq20z90 to go back into shutdown mode for *Shutdown Time* seconds after waking. When in shutdown mode, VCC is completely removed from the bq20z90 by the bq29330. (See *Shutdown Voltage*)
Normal Setting: The default for this register is 10 seconds. Between 10–20 seconds is acceptable for most applications. It is recommended not to go below 10 seconds to prevent an oscillation going into and out of shutdown mode.

Charger Present

A charger is deemed present when ***Pack Voltage*** is at or above this level.
Normal Setting: It is important to note that a charger detection because this function prevents shutdown by either a ***Manufacture Access*** command or *Shutdown Voltage*. Some applications with external voltage sources can confuse the shutdown detection which prevents the bq20z90 shutdown mode from functioning properly. The bq29330 wakes up with a voltage above the “Start-up” voltage which is a wake up feature built into the bq29330 (see the bq29330 data sheet (SLUS629A). If there is an external voltage source that has a voltage above the “Start-up” voltage threshold, but below the *Charger Present* threshold, then the bq20z90 oscillates between awake and shutdown. This causes abnormal operational side effects. Therefore, it is recommended that *Charger Present* be set to 3500 mV if there are any external voltage sources. Otherwise, this voltage can be set to between (3000–4000 mV per cell) × (number of cells) .

Sleep Current

When ***Current*** is less than *Sleep Current* or greater than (–)*Sleep Current* in milliAmps and the following conditions are met:

1. ***Temperature*** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*
2. SMBus clock and data lines are low for more than *Bus Low Time seconds*.
3. [Sleep] is set in *Operation Cfg A*.

Then the bq20z90 does a *CC Offset* calibration, and then goes to sleep.
Normal Setting: This setting should be below any normal application currents. The default is 10 mA which should be sufficient for most applications.

Bus Low Time

When SMBus clock and data lines are low for more than *Bus Low Time* seconds and the following conditions are met:

1. ***Current*** is less than Sleep Current or greater than (-)Sleep Current in milliAmps
2. ***Temperature*** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*.

Then the bq20z90 does a *CC Offset* calibration and then goes to sleep. [Sleep] in *Operation Cfg A* does not affect the calibration portion of this detection.
Normal Setting: This setting should be below any normal application currents. The default is 5 seconds which should be sufficient for most applications. Do not go below 2 seconds to protect against false triggering.

Cal Inhibit Temp Low

For the bq20z90 to perform a *CC Offset* and ADC offset calibration prior to entering sleep mode, ***Temperature*** must be between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High* along with the following conditions:

1. ***Current*** is less than *Sleep Current* or greater than (–)*Sleep Current* in milliAmps.
2. SMBus clock and data lines are low for more than *Bus Low Time seconds*.

Normal Setting: The default for this application is 5° or 50 in 0.1°C units. This should not need to be changed. The bq20z90 does not need to do a *CC Offset* calibration every time the bq20z90 goes to sleep and it definitely does not need to do it at extreme temperatures to prevent temperature drift from decreasing the offset calibration accuracy.

Cal Inhibit Temp High

For the bq20z90 to perform a *CC Offset* and internal ADC offset calibration prior to entering sleep mode, ***Temperature*** must be between *Cal Inhibit Temp High* and *Cal Inhibit Temp High* along with the following conditions:

1. ***Current*** is less than *Sleep Current* or greater than (–)*Sleep Current* in milliAmps
2. SMBus clock and data lines are low for more than *Bus Low Time* seconds

Normal Setting: The default for this application is 45° or 450 in 0.1°C units. This should not need to be changed. The bq20z90 does not need to do a *CC Offset* calibration every time the bq20z90 goes to sleep and it definitely does not need to do it at extreme temperatures to prevent temperature drift from decreasing the offset calibration accuracy.

Sleep Voltage Time

While in sleep mode, the bq20z90 wakes up to measure and updates ***Voltage***, ***Cell Voltage(All)*** and ***Temperature*** every *Sleep Voltage Time* in seconds.
Normal Setting: The default for this register is 5 seconds. It is important to note for the settings of this register that it takes time to measure and update the voltage and temperature registers and the bq20z90 is awake and consuming power during this process. The more the bq20z90 is awake, the more it consumes. There is a trade off between voltage detection and power consumption. It is also important to note that the bq29330 (AFE) protection is still active and not affected by sleep.

Sleep Current Time

While in sleep mode, the bq20z90 wakes up to measure and update ***Current*** and ***Average Current*** every *Sleep Current Time* in seconds. Immediately after this update the bq20z90 goes back to sleep unless ***Current*** is above *Sleep Current* during one of these wake up periods. If it is above *Sleep Current*, then the part stays awake until the sleep conditions are met again (See *Sleep Current*).
Normal Setting: The default for this register is 20 seconds. It is important to note for the settings of this register that it takes about 1 second to measure and update the current registers and the bq20z90 is awake and consuming power during this process. The more the bq20z90 is awake, the more it consumes. There is a trade off between current detection and power consumption. It is also important to note that the bq29330 (AFE) protection is still active and not affected by sleep.

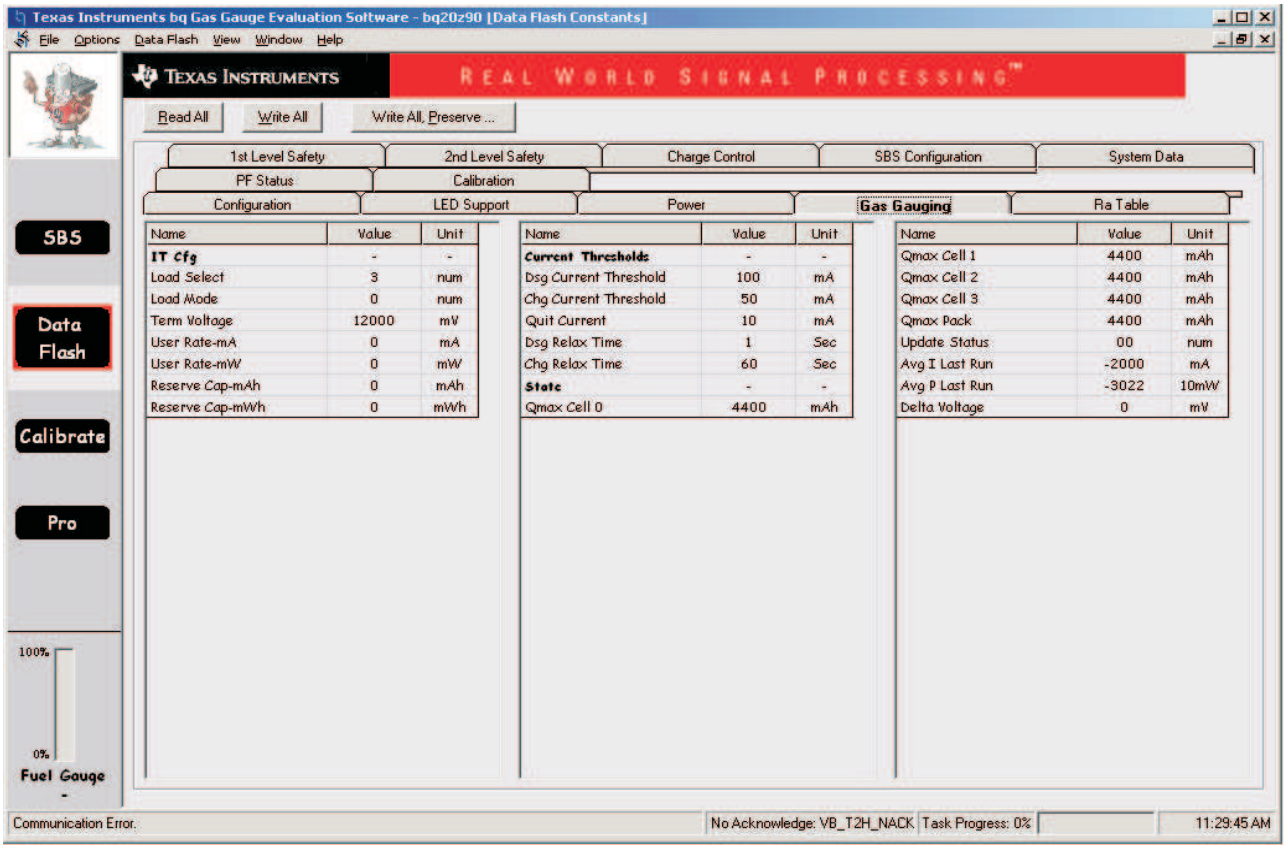
Wake Current Reg

This is one option for waking the bq20z90 from sleep. When the ***Current*** becomes more than what is set in *Wake Current Reg*, then the bq20z90 wakes from sleep.
Normal Setting: The default for this register is 0x00. This means that the function is disabled. The function is based on current, therefore, a sense resistor value must be selected as part of the option in (RSNS1, RSNS0).

–	–	–	–	–	–	–	–
–	–	–	–	–	IWAKE	RSNS1	RSNS0

IWAKE	RSNS1	RSNS0	Current	Sense Resistor Value
0	0	0	Disabled	Disabled
0	0	1	0.5A	2.5 mΩ
0	1	0	0.5A	5 mΩ
0	1	1	0.5A	10 mΩ
1	0	0	Disabled	Disabled
1	0	1	1 A	2.5 mΩ
1	1	0	1 A	5 mΩ
1	1	1	1 A	10 mΩ

2.12 Gas Gauging



IT Config

Load Select

Load Select defines the type of power or current model to be used for Remaining Capacity computation in the Impedance Track™ algorithm. If *Load Mode* = Constant Current then the following options are available:

0 = Average discharge current from previous cycle: There is an internal register that records the average discharge current through each entire discharge cycle. The previous average is stored in this register.

1 = Present average discharge current: This is the average discharge current from the beginning of this discharge cycle till present time.

2 = *Current*: based off of *Current*

3 = *Average Current* (default): based off the *Average Current*

4 = *Design Capacity* / 5: C Rate based off of *Design Capacity* /5 or a C / 5 rate in mA.

5 = *AtRate* (mA): Use whatever current is in *AtRate*

6 = *User_Rate-mA*: Use the value in *User_Rate-mA*. This gives a completely user configurable method.

If *Load Mode* = Constant Power then the following options are available:

0 = Average discharge power from previous cycle: There is an internal register that records the average discharge power through each entire discharge cycle. The previous average is stored in this register.

1 = Present average discharge power: This is the average discharge power from the beginning of this discharge cycle till present time.

2 = *Current* × *Voltage*: based off of *Current* and *Voltage*

3 = *Average Current*×*Voltage* (default): based off the *Average Current* and *Voltage*

4 = *Design Energy* / 5: C Rate based off of *Design Energy* /5 or a C / 5 rate in mA

5 = *AtRate* (10 mW): Use whatever value is in *AtRate*.

6 = *User_Rate-10mW*: Use the value in *User_Rate-mW*. This gives a completely user configurable method.

Normal Setting: The default for this register is 3 which should be acceptable for most applications. This is application dependent.

Load Mode

Load Mode is used to select either the constant current or constant power model for the Impedance Track™ algorithm as used in *Load Select*. (See *Load Select*)

- 0: Constant Current Model
- 1: Constant Power Model

Normal Setting: This is normally set to Current Model but It is application specific. If the application load profile more closely matches a constant power model, then set to 1.

Term Voltage

Term Voltage is used in the Impedance Track™ algorithm to help compute ***Remaining Capacity***. This is the absolute minimum voltage for end of discharge, where the remaining chemical capacity is assumed as zero.
Normal Setting: This register is application dependent. It should be set based on battery cell specifications to prevent damage to the cells or the absolute minimum system input voltage taking into account impedance drop from the PCB traces, FETs, and wires.

User Rate-mAh

User Rate-mAh is only used if *Load Select* is set to 6 and *Load Mode* = 0. If these criteria are met then the current stored in this register is used for the ***Remaining Capacity*** computation in the Impedance Track™ algorithm. This is the only function that uses this register.
Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined current at the end of discharge. With this type of discharge, it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment *Term Voltage* is reached.

User Rate-10mWh

User Rate-10mWh is only used if Load Select is set to 6 and *Load Mode* = 1. If these criteria are met then the power stored in this register is used for the ***Remaining Capacity*** computation in the Impedance Track™ algorithm. This is the only function that uses this register.
Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined power at the end of discharge. With this application. it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment Term Voltage is reached.

Reserve Cap-mAh

Reserve Cap-mAh determines how much actual remaining capacity exists after reaching SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 0. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- [RESCAP]=0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
- [RESCAP]=1: If set to a 1, then a higher rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mA mode (configured by [CAPM] in ***Battery Mode***).
Normal Setting: This register defaults to 0 which disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarm* or *Remaining Capacity Alarm*.

Reserve Cap-10mWh

Reserve Cap-10mWh determines how much actual remaining capacity exists after reaching SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 1. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
- 1: If set to a 1, then a more normal rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mW mode (configured by [CAPM] in ***Battery Mode***).
Normal Setting: This register defaults to 0 which basically disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarm* or *Remaining Capacity Alarm*.

Current Thresholds

Dsg Current Threshold

This register is used as a threshold by many functions in the bq20z90 to determine if actual discharge current is flowing into and out of the part. This is independent from [DSG] in ***Battery Status*** which indicates whether the bq20z90 is in discharge mode or charge mode.
Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. If the bq20z90 is charging, then [DSG] is 0 and any other time (***Current*** less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z90 require more definitive information about whether current is flowing in either the charge or discharge direction. *Dsg Current Threshold* is used for this purpose. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Chg Current Threshold

This register is used as a threshold by many functions in the bq20z90 to determine if actual charge current is flowing into and out of the part. This is independent from [DSG] in ***Battery Status*** which indicates whether the bq20z90 is in discharge mode or charge mode.
Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. Basically, if the bq20z90 is charging then [DSG] is 0 and any other time (***Current*** less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z90 require more definitive information about whether current is flowing in either the charge or discharge direction. This is what *Dsg Current Threshold* is used for. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Quit Current

The *Quit Current* is used as part of the Impedance Track™ algorithm to determine when the bq20z90 goes into relaxation mode from a current flowing mode in either the charge direction or the discharge direction. Either of the following criteria must be met to enter relaxation mode:

1. ***Current*** is **less than** (–)*Quit Current* and then goes within (±)*Quit Current* for *Dsg Relax Time*.
2. ***Current*** is **greater than***Quit Current* and then goes within (±)*Quit Current* for *Chg Relax Time*.

After about 30 minutes in relaxation mode, the bq20z90 attempts to take accurate OCV and Qmax updates which are used in the Impedance Track™ algorithms.
Normal Setting: It is critical that the battery voltage be relaxed during OCV readings to get the most accurate results. This current must not be higher than C/20 when attempting to go into relaxation mode; however, it should not be so low as to prevent going into relaxation mode due to noise. This should always be less than *Chg Current Threshold* or *Dsg Current Threshold*.

Dsg Relax Time

The *Dsg Relax Time* is used in the function to determine when to go into relaxation mode. When ***Current*** is **less than** (–)*Quit Current* and then goes within (±)*Quit Current* the *Dsg Relax Time*, timer is initiated. If the current stays within (±)*Quit Current* until the *Dsg Relax Time* timer expires, then the bq20z90 goes into relaxation mode. After about 30 minutes in relaxation mode, the bq20z90 attempts to take accurate OCV and Qmax updates which are used in the Impedance Track™ algorithms.
Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This is application specific.

Chg Relax Time

The *Chg Relax Time* is used in the function to determine when to go into relaxation mode. When ***Current*** is greater than *Quit Current* and then goes within (±)*Quit Current* the *Chg Relax Time*, timer is initiated. If the current stays within (±)*Quit Current* until the Chg Relax Time timer expires, then the bq20z90 goes into relaxation mode. After about 30 minutes in relaxation mode, the bq20z90 attempts to take accurate OCV and Qmax updates which are used in the Impedance Track™ algorithms.
Normal Setting: This is application specific.

State

Qmax Cell 0

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z90 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Cell 1

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z90 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Cell 2

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z90 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 3

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z90 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Pack

This is the maximum capacity of the entire battery pack. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated to the lowest chemical capacity of all the cells (*Qmax Cell 0 – Qmax Cell 3*) by the bq20z90 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity. It is updated with the capacity of the lowest cell during use. This is because the capacity of the entire battery is only as much as the capacity of the lowest cell. When that cell is empty, it does not matter if any other cells have capacity.

Update Status

There are 2 bits in this register that are important.

- Bit 1 (0x02) indicates that the bq20z90 has learned new Qmax parameters and is accurate.
- Bit 2 (0x04) indicates whether Impedance Track™ algorithm is enabled.

The remaining bits are reserved.
Normal Setting: These bits are user configurable; however, bit 1 is also a status flag that can be set by the bq20z90. These bits should never be modified except when creating a golden image file as explained in the application note *Preparing Optimized Default Flash Constants for specific Battery Types* (see SLUA334.pdf). Bit 1 is updated as needed by the bq20z90 and Bit 2 is set with ***Manufacturers Access*** command 0x0021.

Avg I Last Run

The bq20z90 logs the ***Current*** averaged from the beginning to the end of each discharge cycle. It stores this average current from the previous discharge cycle in this register.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z90 when required.

Avg P Last Run

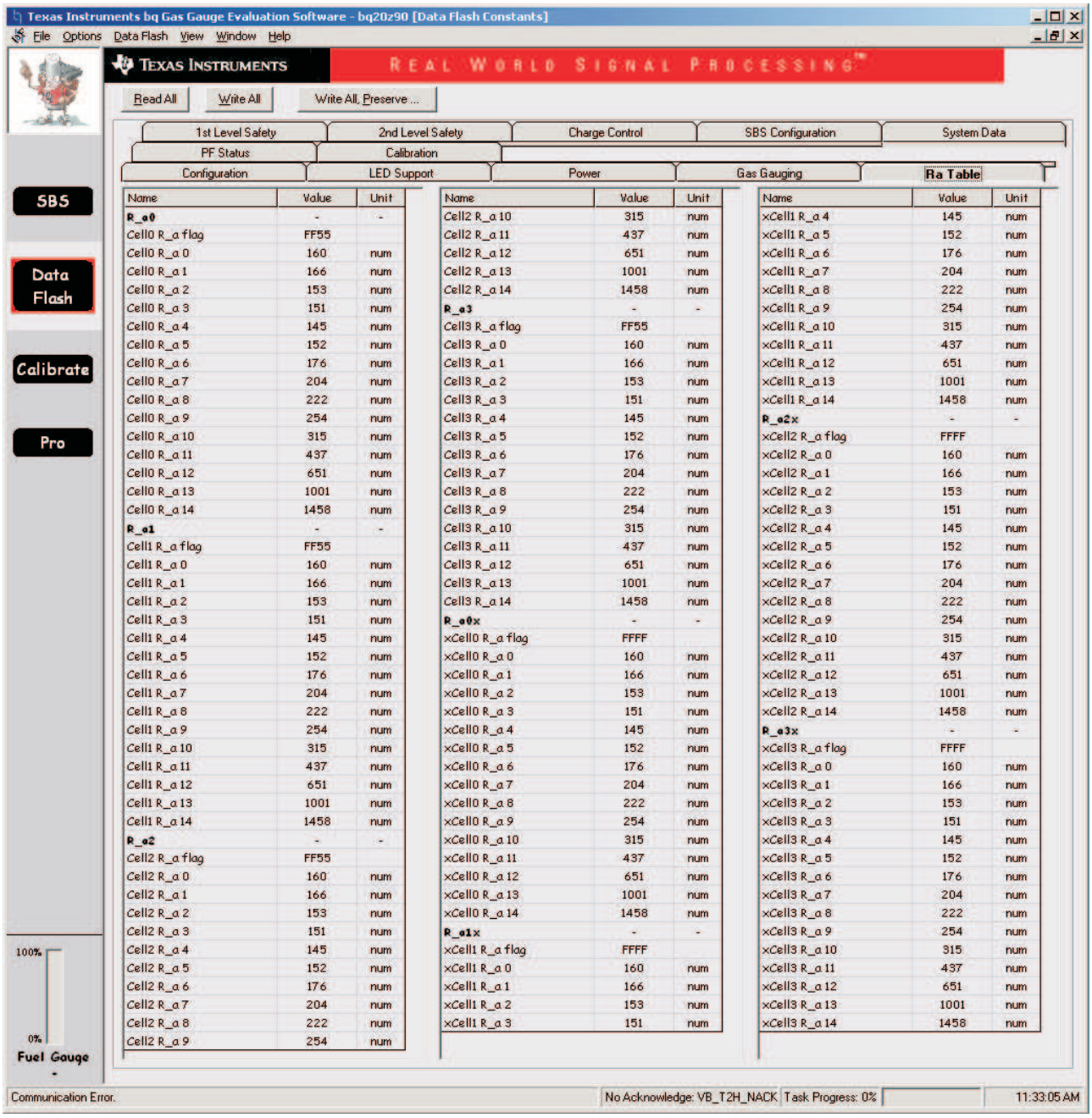
The bq20z90 logs the power averaged from the beginning to the end of each discharge cycle. It stores this average power from the previous discharge cycle in this register. To get a correct average power reading the bq20z90 continuously multiplies ***Current*** times ***Voltage*** to get power. It then logs this data to derive the average power.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z90 when the required.

Delta Voltage

The exact computation of this register is very complex so this description, while not exact, gives the general formula. *Delta Voltage* is derived as a function average ***Voltage*** versus immediate ***Voltage***. The average ***Voltage*** is a localized average over the most recent few seconds. The *Delta Voltage* is the maximum (average ***Voltage***–***Voltage***) at any given time. This register is only updated whenever the algorithm computes a value greater than the previous. Every SOC gridpoint (see *Cell0 R_a0*) causes a sort of reset of this computation. To prevent a 0 value in this register and to give more meaning, the reset algorithm uses a percentage of the previous SOC gridpoint *Delta Voltage* to compute a reset value and then starts the process of computing maximum *Delta Voltage* values again.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z90 when required.

2.13 Ra Table

This data is automatically updated during device operation. No user changes should be made except for reading the values from another pre-learned pack for creating “Golden Image Files”. See application note “Preparation of optimized default flash constants for specific type of battery” (SLUA334). Profiles have format CellN R_a M where N is the cell serial number (from ground up), and M is the number indicating state of charge to which the value corresponds.



Name	Value	Unit
R_a0	-	-
Cell0 R_a flag	FF55	
Cell0 R_a 0	160	num
Cell0 R_a 1	166	num
Cell0 R_a 2	153	num
Cell0 R_a 3	151	num
Cell0 R_a 4	145	num
Cell0 R_a 5	152	num
Cell0 R_a 6	176	num
Cell0 R_a 7	204	num
Cell0 R_a 8	222	num
Cell0 R_a 9	254	num
Cell0 R_a 10	315	num
Cell0 R_a 11	437	num
Cell0 R_a 12	651	num
Cell0 R_a 13	1001	num
Cell0 R_a 14	1458	num
R_a1	-	-
Cell1 R_a flag	FF55	
Cell1 R_a 0	160	num
Cell1 R_a 1	166	num
Cell1 R_a 2	153	num
Cell1 R_a 3	151	num
Cell1 R_a 4	145	num
Cell1 R_a 5	152	num
Cell1 R_a 6	176	num
Cell1 R_a 7	204	num
Cell1 R_a 8	222	num
Cell1 R_a 9	254	num
Cell1 R_a 10	315	num
Cell1 R_a 11	437	num
Cell1 R_a 12	651	num
Cell1 R_a 13	1001	num
Cell1 R_a 14	1458	num
R_a2	-	-
Cell2 R_a flag	FF55	
Cell2 R_a 0	160	num
Cell2 R_a 1	166	num
Cell2 R_a 2	153	num
Cell2 R_a 3	151	num
Cell2 R_a 4	145	num
Cell2 R_a 5	152	num
Cell2 R_a 6	176	num
Cell2 R_a 7	204	num
Cell2 R_a 8	222	num
Cell2 R_a 9	254	num

Name	Value	Unit
Cell2 R_a 10	315	num
Cell2 R_a 11	437	num
Cell2 R_a 12	651	num
Cell2 R_a 13	1001	num
Cell2 R_a 14	1458	num
R_a3	-	-
Cell3 R_a flag	FF55	
Cell3 R_a 0	160	num
Cell3 R_a 1	166	num
Cell3 R_a 2	153	num
Cell3 R_a 3	151	num
Cell3 R_a 4	145	num
Cell3 R_a 5	152	num
Cell3 R_a 6	176	num
Cell3 R_a 7	204	num
Cell3 R_a 8	222	num
Cell3 R_a 9	254	num
Cell3 R_a 10	315	num
Cell3 R_a 11	437	num
Cell3 R_a 12	651	num
Cell3 R_a 13	1001	num
Cell3 R_a 14	1458	num
R_a0x	-	-
xCell0 R_a flag	FFFF	
xCell0 R_a 0	160	num
xCell0 R_a 1	166	num
xCell0 R_a 2	153	num
xCell0 R_a 3	151	num
xCell0 R_a 4	145	num
xCell0 R_a 5	152	num
xCell0 R_a 6	176	num
xCell0 R_a 7	204	num
xCell0 R_a 8	222	num
xCell0 R_a 9	254	num
xCell0 R_a 10	315	num
xCell0 R_a 11	437	num
xCell0 R_a 12	651	num
xCell0 R_a 13	1001	num
xCell0 R_a 14	1458	num
R_a1x	-	-
xCell1 R_a flag	FFFF	
xCell1 R_a 0	160	num
xCell1 R_a 1	166	num
xCell1 R_a 2	153	num
xCell1 R_a 3	151	num

Name	Value	Unit
xCell1 R_a 4	145	num
xCell1 R_a 5	152	num
xCell1 R_a 6	176	num
xCell1 R_a 7	204	num
xCell1 R_a 8	222	num
xCell1 R_a 9	254	num
xCell1 R_a 10	315	num
xCell1 R_a 11	437	num
xCell1 R_a 12	651	num
xCell1 R_a 13	1001	num
xCell1 R_a 14	1458	num
R_a2x	-	-
xCell2 R_a flag	FFFF	
xCell2 R_a 0	160	num
xCell2 R_a 1	166	num
xCell2 R_a 2	153	num
xCell2 R_a 3	151	num
xCell2 R_a 4	145	num
xCell2 R_a 5	152	num
xCell2 R_a 6	176	num
xCell2 R_a 7	204	num
xCell2 R_a 8	222	num
xCell2 R_a 9	254	num
xCell2 R_a 10	315	num
xCell2 R_a 11	437	num
xCell2 R_a 12	651	num
xCell2 R_a 13	1001	num
xCell2 R_a 14	1458	num
R_a3x	-	-
xCell3 R_a flag	FFFF	
xCell3 R_a 0	160	num
xCell3 R_a 1	166	num
xCell3 R_a 2	153	num
xCell3 R_a 3	151	num
xCell3 R_a 4	145	num
xCell3 R_a 5	152	num
xCell3 R_a 6	176	num
xCell3 R_a 7	204	num
xCell3 R_a 8	222	num
xCell3 R_a 9	254	num
xCell3 R_a 10	315	num
xCell3 R_a 11	437	num
xCell3 R_a 12	651	num
xCell3 R_a 13	1001	num
xCell3 R_a 14	1458	num

Cell0 R_a flag,
Cell1 R_a flag,
Cell2 R_a flag,
Cell3 R_a flag,
xCell0 R_a flag,
xCell1 R_a flag,
xCell2 R_a flag,
xCell3 R_a flag

Each subclass (R_a0-R_a3 and R_a0x-R_a3x) in the Ra Table class is a separate profile of resistance values normalized at 0 degrees for each of the cells in a design (cells 0–3) There are 2 profiles for each cell. They are denoted by the x or absence of the x at the end of the subclass Title:
R_a0 or **R_a0x** for cell 0
R_a1 or **R_a1x** for cell 1
R_a2 or **R_a2x** for cell 2
R_a3 or **R_a3x** for cell 3
The purpose for 2 profiles for each series cell is to ensure that at any given time there is at least one profile is enabled and being used while attempts can be made to update the alternate profile without interference. Having 2 profiles also helps reduce stress on the Flash Memory. At the beginning of each of the 8 subclasses (profiles) is a flag called *CellM R_a flag* or *xCellM R_a flag* where “M” is the cell number (0-3). This flag is a status flag indicates the validity of the table data associated with this flag and whether this particular table is enabled/disabled. There are 2 bytes in each flag:

1. The LSB (least significant byte) indicates whether the table is currently enabled or disabled. It has the following options:
   a. 0x00 : means the table has had a resistance update in the past; however, it is not the currently enabled table for this cell. (the alternate table for the indicated cell must be enabled at this time)
   b. 0xff: This means that the values in this table are default values. This table resistance values have never been updated, and this table is not the currently enabled table for this cell. (the alternate table for the indicated
   c. 0x55: This means that this table is enabled for the indicated cell (the alternate table must be disabled at this time.) cell must be enabled at this time)
2. The MSB (Most significant byte) indicates that status of the data in this particular table. The possible values for this byte are:
   a. 0x00: The data associated with this flag has had a resistance update and the *QMax Pack* has been updated
   b. 0x05: The resistance data associated with this flag has been updated and the pack is no longer discharging (this is prior to a *Qmax Pack* update).
   c. 0x55: The resistance data associated with this flag has been updated and the pack is still discharging (Qmax update attempt not possible until discharging stops).
   d. 0xff: The resistance data associated with this flag is all default data.

This data is used by the bq20z90 to determine which tables need updating and which tables are being used for the Impedance Track™ algorithm.
Normal Setting: This data is used by the bq20z90 Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This description of the *xCellM R_a flags* are intended for information purposes only. It is not intended to give a detailed functional description for the bq20z90 resistance algorithms.

Cell0 R_a0 – Cell0 R_a14,
xCell0 R_a0 – xCell0 R_a14,
Cell1 R_a0 – Cell1 R_a14,
xCell1 R_a0 – xCell1 R_a14,
Cell2 R_a0 – Cell2 R_a14,
xCell2 R_a0 – xCell2 R_a14,
Cell3 R_a0 – Cell3 R_a14,
xCell3 R_a0 – xCell3 R_a14,

There are 15 values for each R_a subclass in the **Ra Table** class. Each of these values represent a resistance value normalized at 0°C for the associated *Qmax Pack* based SOC gridpoint as found by the following rules:

For *CellN R_aM* where:

1. if $0 \leq M \leq 8$: The data is the resistance normalized at 0° for: SOC = 100% – (M × 10%)
2. if $9 \leq M \leq 14$: The data is the resistance normalized at 0 degrees for: SOC = 100% – [80% + (M – 8) × 3.3%]

This gives a profile of resistance throughout the entire SOC profile of the battery cells concentrating more on the values closer to 0%.
Normal Setting: SOC as stated in this description is based on *Qmax Pack*. It is not derived as a function of RSOC or ASOC. These resistance profiles are used by the bq20z90 for the Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This resistance profile description is for information purposes only. It is not intended to give a detailed functional description for the bq20z90 resistance algorithms. It is important to note that this data is in units of milliohms and is normalized to 0°C. Useful observations to note with this data throughout the application development cycle:

1. Watch for negative values in the **Ra Table** class. There should never be negative numbers in profiles anywhere in this class.
2. Watch for smooth consistent transitions from one profile gridpoint value to the next throughout each profile. As the bq20z90 does resistance profile updates these values should be roughly consistent from one learned update to another without huge jumps in consecutive gridpoints.

Chapter 3

Configuring the bq20z70 Data Flash

Battery Management

ABSTRACT

The bq20z70 has numerous data flash constants that can be used to configure the device with a variety of different options for most features. The data flash of the bq20z70 is split into sections which are described in detail within this document.

3.1 Glossary

RSOC: Relative state of Charge

ASOC: Absolute State of Charge

Bit: This word has a different meaning than Flag. This word is used to refer to a configuration setting bit. It is primarily used in data flash settings.

Blink, Flash and Delay: There are 3 different display modes for the LEDs in this document that need clarification.

- Blinking: When the display is said to be blinking, then the word "blinking" is used to refer to the LED located closest to the LED used to indicate 100% that is illuminated and "blinking" when the LED display is activated and displaying SOC (state of charge). Only this "topmost" activated LED in the display blinks. All other LEDs that are activated is steady state when activated. (see *LED Blink Rate*)
- Flashing: When the display is said to be flashing, then the word "flashing" means all LEDs that are activated to indicate the SOC will flash with a period of (2 ×*LED Flash Rate*).
- Delay: When the display is activate, all LEDs that are required to indicate the SOC may not illuminate at the same time. Starting from the LED that represents the lowest SOC, there can be a delay (*LED Delay*) between each LED illuminating from the LED that represents the lowest possible SOC up to the LED that represents the present SOC.

***Cell Voltage(Max)*:** This represents the maximum value among all the SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)

***Cell Voltage(Min)*:** This represents the minimum value among all the SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)

***Cell Voltage(Any)*:** This represents any of the possible SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)

[DSG] in *Battery Status*: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. This can be confused in many descriptions in this document because different functions require different methods for determining charging or discharging. The SBS description sometimes does not give enough resolution for correct part function so these functions require other data flash registers as described in their respective definitions. SBS states that if the battery is charging then [DSG] is 0, and any other time (Current less than or equal to 0), the [DSG] flag is set. The actual formula that the bq20z70 uses for setting or clearing the [DSG] flag are as follows:

[DSG] clear: [DSG]=0 if *Current*≥*Chg Current Threshold*

[DSG] set: [DSG]=1 if

1. Current ≤*Dsg Current Threshold* or
2. Relaxation Mode which is defined by one of the following statements:
   - A) *Current* transitioning from below (–)*Quit Current* to (above (–)*Quit Current* and below *Quit Current*) for *Dsg Relax Time*
   - B) *Current* transitioning from above *Quit Current* to (below *Quit Current* and above (–)*Quit Current*) for *Chg Relax Time*

FCC: Full Charge Capacity

FET opened/Closed: It is common to say FET opened or FET closed. This is used throughout this document to mean the FET is turned off or the FET is turned on respectively.

Flag: This word is usually used to represent a read only status bit that indicates some action has occurred or is occurring. This bit usually cannot be modified by the user.

Precharge/ZVCHG: The words Precharge and ZVCHG are interchangeable throughout the document

RCA: Remaining Capacity Alarm

RM: Remaining Capacity

RSOC: Relative state of Charge

RTA: Remaining Time Alarm

SOC: This is used as a generic meaning of State-of-Charge. It can mean RSOC, ASOC, or percentage of actual chemical capacity.

System: The word system is sometimes used in this document. It always means a host system that is consuming current from the battery pack that includes the bq20z70.

***Italics*:** All words in this document that are in italics represent names of data flash locations exactly as they are shown in the EV software.

***Bold Italics*:** All words that are bold italic represent SBS compliant registers exactly as they are shown in the EV software.

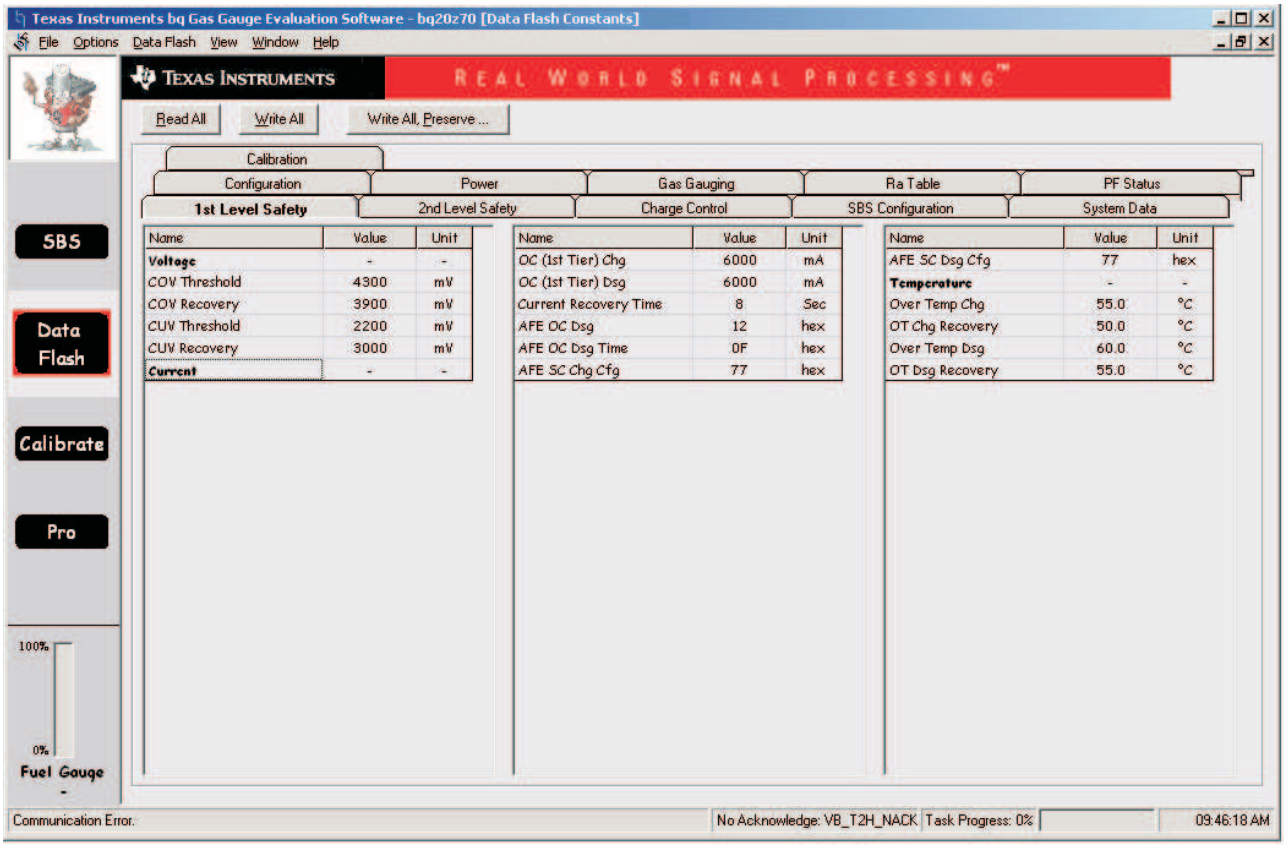
[brackets]: All words or letters in brackets represent bit/flag names exactly as they are shown in the SBS and Data Flash in the EV software.

(–): This is commonly used in this document to represent a minus sign. It is written this way to ensure that the sign is not lost in the translation of formulas in the text of this document.

3.2 Data Flash Descriptions

1st Level Safety

All 1st Level Safety functions are temporary. There should be no permanent failures or damage to the battery if any of the 1st Level Safety functions are triggered.



Voltage

COV Threshold

When any cell voltage measured by ***Cell Voltage (Any)*** rises to this threshold, then the Cell Over Voltage (COV) protection process is triggered, initiating a [COV] in detection sequence for 2 seconds. If the COV condition clears prior to the expiration of the 2 second timer, then [COV] detection sequence is cleared and no [COV] flag is set in ***Safety Status***. If the Cove condition does not clear then {COV} is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes {TCA} in Battery Status to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.

Normal Setting: Default is 4300 mV. This cell is chemistry dependent, but 4200–4300 is the most common settings.

COV Recovery

When a [COV] is set in Safety Status, it can only be cleared when **ALL** cell voltages as measured by ***Cell Voltage(All)*** fall be below this threshold.

Normal Setting: This defaults to 3900 mV. Set low enough that the hysteresis between *COV Threshold* fault and this recovery prevents oscillation of the Charge FET.

CUV Threshold

When any cell voltage measured by ***Cell Voltage(Any)*** falls below this threshold then the Cell Under Voltage (CUV) detection process is triggered. If the CUV condition clears within a 2 second timer window then the CUV detection process is cleared and no [CUV] is set in ***Safety Status***. If the CUV condition does not clear then a [CUV] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [TDA] and [FD] in ***Battery Status*** to be set. It also causes [XDSG] in ***Operation Status***.

Normal Setting: Default is 2200 mV. This is cell chemistry dependent by 2200 mV–2300 mV is the most common setting

CUV Recovery

When [CUV] is set in ***Safety Status***, it can only be cleared when **ALL** cell voltages as measured by ***Cell Voltage(All)*** rise above this threshold.

Normal Setting: The default for this register is 3000 mV. Set high enough that the hysteresis between *CUV Threshold* fault and this recovery prevents oscillation of the Discharge FET.

Current

There are 2 levels or tiers of current protection in the bq20z70. The first 2 levels, 1st Tier and 2nd Tier is slow responding (>1 second). The 2nd level (denoted by AFE in the labels of the data flash locations) is a very quick responding current protection controlled directly by the bq29330.

IT is important to note that the bq29330 makes the triggering decision for any of the AFE fault conditions. This is to ensure quick response to dangerous faults that could not only cause damage but also hazards. It is also designed in such a way that the AFE can act completely autonomously in the event of damage to the bq20z70 in the triggering of any AFE fault. The bq29330 cannot, however, clear the fault condition. It is cleared only by the bq20z70. The AFE data is transferred to the bq29330 on reset and (if enabled in the **AFE Verification** subclass) is continually monitored by the bq20z70 to ensure no corruption has occurred at any time. If corruption has occurred the bq20z70 will attempt to correct it and if after repeated attempts (as set in the **AFE Verification** subclass) it cannot correct the condition then it will set a permanent failure. If enabled in *Permanent Fail Cfg*, then the SAFE pin is driven high on the bq20z70. (See *Permanent Fail Cfg*)

OC (1st Tier) Chg

When current measured by ***Current*** reaches up to or above this threshold during charging then the 1st Tier Over Current in Charge [OCC] detection process is triggered. If the 1st Tier OCC condition clears prior to the expiration of a 2 second timer, then [OCC] detection process is cleared and no [OCC] is set in ***Safety Status***. If the 1st Tier OCC condition does not clear then a [OCC] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.

Normal Setting: This register is application dependent. It should be set above the absolute maximum expected discharge current. It should be set high enough that unexpected mild charge spikes or inaccuracies will not create a false over current trigger but low enough to force the Charge FET to open before damage can occur to the pack.

OC (1st Tier) Dsg

When current measured by ***Current*** falls down to or below this threshold during discharging then the 1st Tier Over Current in discharge (OCD) detection process is triggered. If the 1st Tier OCD condition clears prior to the expiration of 2 second timer, then no [OCD] is set is ***Safety Status***. If the 1st Tier OCD condition does not clear then [OCD] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [XDSG] and [XDSGI] in ***Operation Status*** to be set. It also causes ***Charging Current*** to be set to 0.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent. It should be set **below** the absolute maximum expected discharge current. It should be set **low** enough that unexpected mild discharge spikes or inaccuracies will not create a false over current trigger but **high** enough to force the Discharge FET open before damage can occur to the pack.

Current Recovery Timer

The *Current Recovery Timer* is used in the recovery process of any of the over current fault conditions. After a fault condition exists, depending on if enabled, the fault condition is cleared only after *Current Recovery Timer* time in seconds with ***AverageCurrent*** falling below the corresponding recovery threshold in the charge direction or rising above the corresponding recovery threshold in the discharge direction. The corresponding recovery does not happen immediately after the recovery condition exits. As soon as the recovery condition exists then the *Current Recovery Time* timer starts and the condition clears and the corresponding FET is enabled after the *Current Recovery Time* timer expires. This timer is associated with the following Fault Conditions as described in this section:

1. *OC (1st Tier) Dsg*
2. *OC (1st Tier) Chg*
3. *AFE OC Dsg*
4. *AFE SC Dsg*
5. *AFE SC Chg*

This Recovery method is enabled if [NR] is set in *Operation Cfg B*, or if ([NR] is cleared and the corresponding bits are set in the *Non-Removable Cfg* register:

1. *OC (1st Tier) Dsg* [OCD]
2. *OC (1st Tier) Chg* [OCC]
3. *AFE OC Dsg* [AOCD]
4. *AFE SC Dsg* [SCD]
5. *AFE SC Chg* [SCC]

Normal Setting: The default for this register is 8 seconds. This is a recommended number to prevent heating up in the corresponding FET.

AFE OC Dsg

See the important note about all AFE fault conditions at the beginning of the **Current** section.

This is the third level Over Current protection in the discharge direction. This is a last effort protection function before using the Permanent Fail Functions in the Second Level Safety Class. This register displays in HEX using the EV Software. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If the *AFE OC DSG* condition exists for *AFE OC Dsg Time* in milliseconds, then the discharge FET opens as controlled by the bq29330. This fault condition causes [AOCD] to be set in ***Safety Status*** and [XDSG], [XDSGI] is set in ***Operation Status***, and [TDA] is set in ***Battery Status***. It also causes ***Charging Current*** to be set to 0. See Table 10 for settings for this register.

Table 10. AFE OC Dsg Configuration

0X00	**0.050 V**	**0x08**	**0.090 V**	**0x10**	**0.130 V**	**0x18**	**0.170 V**
0x01	**0.055 V**	**0x09**	**0.095 V**	**0x11**	**0.135 V**	**0x19**	**0.175 V**
0x02	**0.060 V**	**0x0a**	**0.100 V**	**0x12**	**0.140 V**	**0x1a**	**0.180 V**
0x03	**0.065 V**	**0x0b**	**0.105 V**	**0x13**	**0.145 V**	**0x1b**	**0.185 V**
0x04	**0.070 V**	**0x0c**	**0.110 V**	**0x14**	**0.150 V**	**0x1c**	**0.190 V**
0x05	**0.075 V**	**0x0d**	**0.115 V**	**0x15**	**0.155 V**	**0x1d**	**0.195 V**
0x06	**0.080 V**	**0x0e**	**0.120 V**	**0x16**	**0.160 V**	**0x1e**	**0.200 V**
0x07	**0.085 V**	**0x0f**	**0.125 V**	**0x17**	**0.165 V**	**0x1f**	**0.205 V**

Normal Setting: Note that the maximum value for this register is 0x1F. Values above 0x1F cause unpredictable results. This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is **below** the *OC (2nd Tier) Dsg* given the application sense resistor value.

AFE OC Dsg Time

This is the time after detection of an *AFE OC Dsg* fault before the Discharge FET attempts to open. This trigger function is completely controlled by the bq29330. The setting of this register is in HEX, and it is in milliseconds (See *AFE OC Dsg*). See Table 11 for setting for this register.

Table 11. AFE OC Dsg Time Configuration

0x00	**1 ms**	**0x04**	**9 ms**	**0x08**	**17 ms**	**0x0c**	**25 ms**
0x01	**3 ms**	**0x05**	**11 ms**	**0x09**	**19 ms**	**0x0d**	**27 ms**
0x02	**5 ms**	**0x06**	**13 ms**	**0x0a**	**21 ms**	**0x0e**	**29 ms**
0x03	**7 ms**	**0x07**	**15 ms**	**0x0b**	**23 ms**	**0x0f**	**31 ms**

Normal Setting: Note that the maximum value for this register is 0x0F. Values above 0x0F will cause unpredictable results. This register is completely application specific. It should be set long enough to prevent false triggering of the [AOCD] in ***Safety Status***, but short enough to prevent damage to the battery pack.

AFE SC Chg Cfg

See the **NOTE** at the beginning of the Current section for an important note about all AFE fault conditions.

This register includes 2 settings. The registers are refered to as *AFE SC Chg* and *AFE SC Chg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4-7) sets the time for the AFE short circuit in the Charge direction fault detection time (*AFE SC Chg Time*). The least significant nibble (bits 0-3) set the threshold at which the bq29330 detects a AFE short circuit fault (*AFE SC Chg*). This is an extreme condition with settings for very large voltages and very short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Charge FET opens as controlled by the bq29330. This fault condition causes [SCC] to be set in ***Safety Status***, and [TCA] to be set in ***Battery Status***. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. See Table 13 for settings for this register.

Table 12. AFE SC Chg Cfg Bit Description

7	6	5	4	3	2	1	0
SCCT3	SCCT2	SCCT1	SCCT0	SCCV3	SCCV2	SCCV1	SCCV0
AFE SC Chg Time				*AFE SC Chg*			

Table 13. AFE SC Chg Cfg Least Significant Nibble (SCCV3-SCCV0)

0x00	**0.100 V**	**0x04**	**0.200 V**	**0x08**	**0.300 V**	**0x0c**	**0.400 V**
0x01	**0.125 V**	**0x05**	**0.225 V**	**0x09**	**0.325 V**	**0x0d**	**0.425 V**
0x02	**0.150 V**	**0x06**	**0.250 V**	**0x0a**	**0.350 V**	**0x0e**	**0.450 V**
0x03	**0.175 V**	**0x07**	**0.275 V**	**0x0b**	**0.375 V**	**0x0f**	**0.475 V**

Table 14. AFE SC Chg Cfg Most Significant Nibble (SCCT3-SCCT0)

0x00	**0 µs**	**0x04**	**244 µs**	**0x08**	**488 µs**	**0x0c**	**732 µs**
0x01	**61 µs**	**0x05**	**305 µs**	**0x09**	**549 µs**	**0x0d**	**793 µs**
0x02	**122 µs**	**0x06**	**366 µs**	**0x0a**	**610 µs**	**0x0e**	**854 µs**
0x03	**183 µs**	**0x07**	**427 µs**	**0x0b**	**671 µs**	**0x0f**	**915 µs**

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is sufficiently above *OC (2nd Tier) Chg*.

AFE SC Dsg Config

See the important note about all AFE fault conditions at the beginning of the Current section.

This register includes 2 settings. See these as *AFE SC Dsg* and *AFE SC Dsg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4–7) sets the time for the AFE short circuit in the discharge direction fault detection time (*AFE SC Dsg Time*). The least significant nibble (bits 0–3) sets the threshold at which the bq29330 detects an AFE short circuit fault in the discharge direction (*AFE SC Dsg*). This is an extreme condition with settings for very large voltages and very short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Discharge FET opens as controlled by the bq29330. This fault condition causes [SCD] to be set in ***Safety Status***, [XDSG] and [XDSGI] to be set in ***Operation Status***, and [TDA] to be set in ***Battery Status***. See Table 16 and Table 17 for settings for this register.

Table 15. AFE SC Dsg Cfg Bit Description

7	6	5	4	3	2	1	0
SCDT3	SCDT2	SCDT1	SCDT0	SCDV3	SCDV2	SCDV1	SCDV0
AFE SC Dsg Time				*AFE SC Dsg*			

Table 16. AFE SC Dsg Cfg Least Significant Nibble (SCDV3-SCDV0)

0x00	**0.10 V**	**0x04**	**0.20 V**	**0x08**	**0.30 V**	**0x0c**	**0.40 V**
0x01	**0.125 V**	**0x05**	**0.225 V**	**0x09**	**0.325 V**	**0x0d**	**0.425 V**
0x02	**0.150 V**	**0x06**	**0.250 V**	**0x0a**	**0.350 V**	**0x0e**	**0.450 V**
0x03	**0.175 V**	**0x07**	**0.275 V**	**0x0b**	**0.375 V**	**0x0f**	**0.475 V**

Table 17. AFE SC Dsg Cfg Most Significant Nibble (SCDT3-SCDT0)

0x00	**0 µs**	**0x04**	**244 µs**	**0x08**	**488 µs**	**0x0c**	**732 µs**
0x01	**61 µs**	**0x05**	**305 µs**	**0x09**	**549 µs**	**0x0d**	**793 µs**
0x02	**122 µs**	**0x06**	**366 µs**	**0x0a**	**610 µs**	**0x0e**	**854 µs**
0x03	**183 µs**	**0x07**	**427 µs**	**0x0b**	**671 µs**	**0x0f**	**915 µs**

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required to determine the proper setting for this register. Be sure that this value is **below** AFE OC Dsg.

Temperature

Over Temp Chg

When the pack temperature measured by ***Temperature*** rises up to or above this threshold while charging (***Current*** > *Chg Current Threshold*) then the Over Temperature in charge direction (OTC) detection process is triggered. If the OTC condition clears within 2 seconds, then no [OTC] is set in ***Safety Status***. If the condition does not clear, then [OTC] is set in ***Safety Status*** and if [OTFET] is set in *Operation Cfg B* the Charge FET is opened. If [OTFET] is not set in *Operation Cfg B*, then the Charge FET is not opened by this fault. This fault condition causes [TCA] and [OTA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 55°C which should be sufficient for most Li-Ion applications.

OT Chg Recovery

OT Chg Recovery is the temperature at which the battery recovers from an *OT Temp Chg* fault. This is the only recovery method for an *OT Temp Chg* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Charge FET if it was opened with the fault. The default is 50°C which is a 5 degree difference which should be sufficient to protect against oscillation during the transition between conditions.

Over Temp Dsg

When the pack temperature measured by ***Temperature*** rises up to or above this threshold while discharging (***Current*** <(–)(*Dsg Current Threshold*)), then the Over Temperature in discharge direction (OTD) protection process is triggered. If the OTD condition clears within 2 seconds, then no [OTD] is set in ***Safety Status***. If the condition does not clear then [OTD] is set in ***Safety Status*** and if [OTFET] is set in *Operation Cfg B* the Discharge FET is opened. If [OTFET] is not set in *Operation Cfg B*, then the Discharge FET is not opened by this fault. This fault condition causes [TDA] and [OTA] in ***Battery Status*** to be set. It also causes ***Charging Current*** to be set to 0.

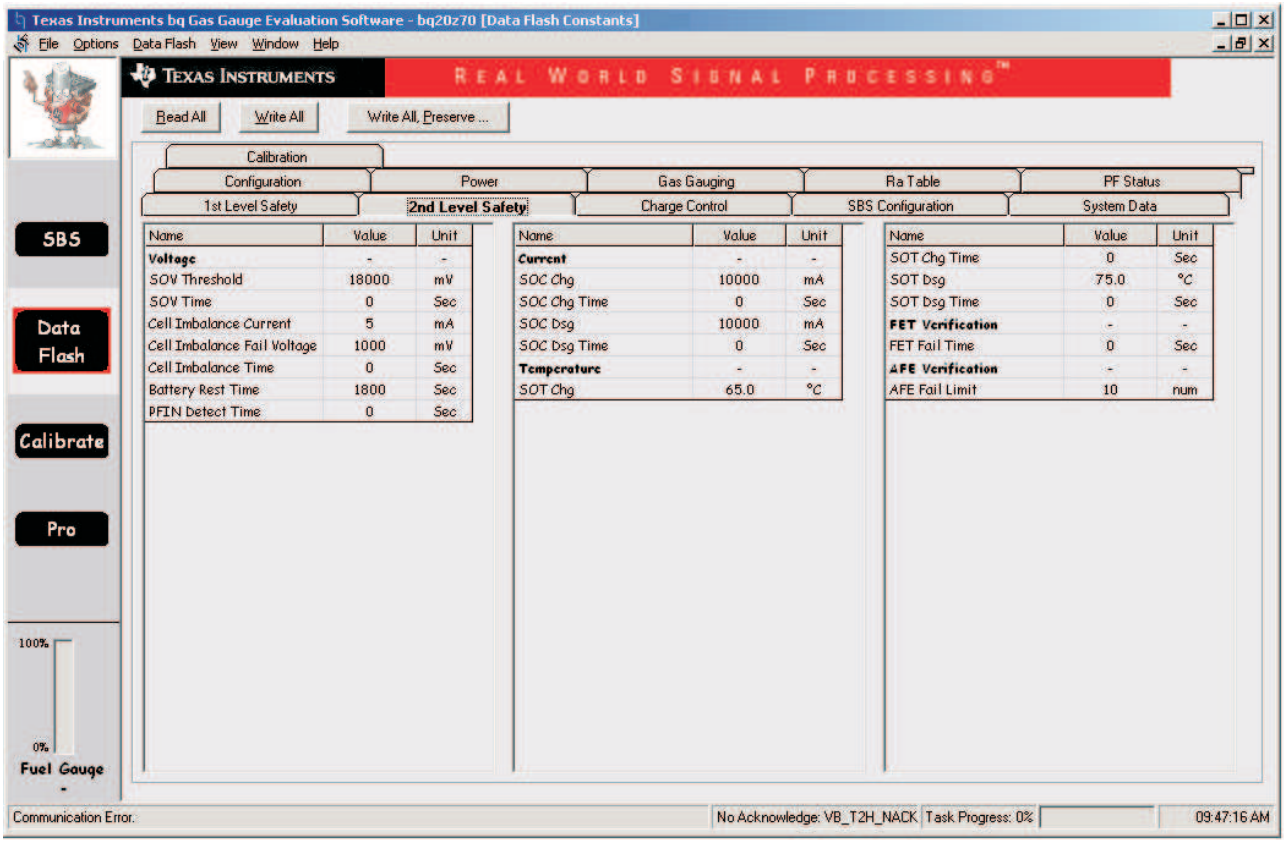
Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 60°C which is sufficient for most Li-Ion applications. The reason why the default *Over Temp Dsg* setting is higher than the default *Over Temp Chg* is because Li-Ion can handle a higher temperature in the discharge direction than in the charge direction.

OT Dsg Recovery

OT Dsg Recovery is the temperature at which the battery recovers from an *OT Temp Dsg* fault. This is the only recovery method for an *OT Temp Dsg* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Discharge FET if it was opened with the fault. The default is 55°C which is a 5 degrees difference which is sufficient to protect against this oscillation during the transition between conditions.

3.3 2nd Level Safety



Voltage

SOV Threshold

This is a final level of protection. It is permanent. When the pack voltage measured by ***Voltage*** rises up to this threshold then the Safety Over Voltage (SOV) detection process is triggered. If the SOV condition clears within 2 seconds, then no [SOV] is set in ***PF Status***. If the SOV condition does not clear then [SOV] is set in ***PF Status***. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOV] in *Permanent Fail Cfg*, then the Safety Output pin is activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a voltage above the *POV Threshold*. This is meant to be a permanent condition, and it is recommended that [XSOV] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOV Time

See *SOV Threshold*. This is a buffer time allotted for an SOV condition. The timer starts When the Safety Over Voltage [SOV] detection process is triggered. When it expires, the bq20z70 forces an [SOV] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOV Time* timer, then [SOV] is cleared in ***PF Alert***, and the *SOV Time* timer resets without setting [SOV] in ***PF Status***. If *SOV Time* is 0, then the *SOV Threshold* function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. It is highly recommended to enable this function in the final application. The most common values for this register are between 2–5 seconds.

Cell Imbalance Current

This is part of the safety cell imbalance detection algorithm. There are 4 registers that go together to make up this algorithm. *Cell Imbalance Current* is the value that ***Current*** must be below for the entire *Battery Rest Time* before Cell Imbalance detection is enabled. The bq20z70 does not start detecting a cell imbalance for this safety algorithm until the battery ***Current*** has been below this ***Cell Imbalance Current*** for at least the *Battery Rest Time*.

Normal Setting: This register should be set low to ensure the battery is completely relaxed when this algorithm is enabled. This Safety algorithm if triggered is permanent, and renders the battery useless. It is imperative that all data is valid prior to activation. The default setting is 5 mA which is sufficient for most applications.

Cell Imbalance Fail Voltage

This is part of the safety cell imbalance detection algorithm. For the purpose of this description:

Cell Voltage H = the highest SBS cell voltage

Cell Voltage L = the lowest SBS cell voltage

Delta Cell Voltage = ***Cell Voltage H–Cell Voltage L***

There are 4 registers that go together to make up this algorithm. After the *Battery Rest Time* portion of the Cell Imbalance algorithm has passed the test criteria (see *Battery Rest Time* and *Cell Imbalance Current*), then if ***Delta Cell Voltage*** is greater than the *Cell Imbalance Fail Voltage* in millivolts, then the *Cell Imbalance Fail Voltage* protection process is triggered. This process starts by setting [CIM] in ***PF Alert*** for *Cell Imbalance Time*. If the cell imbalance condition does not clear then [CIM] is set in ***PF Status***. This triggers many permanent protection features as listed here::

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XCIM] in *Permanent Fail Cfg* then the Safety Output pins are activated which is intended to blow a fuse
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a voltage high enough to prevent any possibility of false triggering because this application is irreversible. This is meant to be a permanent condition and it is recommended that [XCIM] be set in Permanent Fail Cfg with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

Cell Imbalance Time

See *Cell Imbalance Fail Voltage*. This is a buffer time allotted for a cell imbalance safety condition. The timer starts after the *Battery Rest Time* has expired with current below the *Cell Imbalance Current* and ***Delta Cell Voltage*** (see *Cell Imbalance Fail Voltage*) is above the *Cell Imbalance Fail Voltage*. When the *Cell Imbalance Time* timer then the bq20z70 forces a [CIM] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Cell Imbalance Time* timer, then the *Cell Imbalance Time* timer resets without setting [CIM] in ***PF Status***. The *Cell Imbalance Fail Voltage* function is disabled with *Cell Imbalance Time* equal to 0 or *Battery Rest Time* set to 0.

Normal Setting: This register defaults to 0. This disables the function. It is recommended that this function be enabled and the [XCIM] be enabled in *Permanent Failure Cfg* to protect against a potentially dangerous condition. *Battery Rest Time* helps prevent false triggering of this condition, so a good setting for Cell imbalance Time is 5 seconds. This gives several readings to ensure that the condition does exist.

Battery Rest Time

See *Cell Imbalance Current*. *Battery Rest Time* is the time in seconds that the battery ***Current*** must be below the *Cell Imbalance Current* for before Cell Imbalance detection is enabled. The bq20z70 does not start detecting a cell imbalance for this safety algorithm until the battery ***Current*** has been below *Cell Imbalance Current* for at least the *Battery Rest Time*. The *Cell Imbalance Fail Voltage* function is disabled with *Cell Imbalance Time* equal to 0 or *Battery Rest Time* set to 0.

Normal Setting: This register should be set for a relatively long time period to ensure the battery is completely relaxed when this algorithm is enabled. This safety algorithm, if triggered, is permanent and renders the battery useless. It is imperative that all data is valid prior to activation. The default setting is 1800 seconds which is sufficient for most applications.

PFIN Detect Time

This is a buffer time allotted for an $\overline{\text{PFIN}}$ safety condition. The timer *PFIN Detect Time* timer starts after the $\overline{\text{PFIN}}$ input pin has been set logic low by some external device (normally an external protector). When the *PFIN Detect Time* timer expires then the bq20z70 forces an {PFIN} in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *PFIN Detect Time* timer then the *PFIN Detect Time* timer resets without setting {PFIN} in ***PF Status***. If *PFIN Detect Time* is 0 then this function is disabled. This fault condition triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XPFIN] in *Permanent Fail Cfg* then the Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

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Normal Setting: If this fault condition occurs then it is because an external device has already triggered a fault that should be nonrecoverable. This is meant to be a permanent condition, and it is recommended that [XPFIN] be set in *Permanent Fail Cfg*. If a fault occurs, and the external device sets the $\overline{\text{PFIN}}$ input low, the fuse will blow. If the fuse does not blow, then the bq20z70 attempts to blow the fuse (SAFE pin is set high. There is a clear function for this condition, but it is only intended to be used during the development process. The default for this function is 0. If the $\overline{\text{PFIN}}$ input is not used, then this function should be disabled. It is recommended that this function be used, and that [XPFIN] be set to ensure safe operation

Current

SOC Chg

SOC Chg is a final level of current protection from the bq20z70. This is not related to the 2nd level (AFE) protection which is a fast acting protection. It is also intended to be permanent. When the charge current as measured by ***Current*** rises to or above this threshold, then the Safety Over Current in the Charge direction (SOCC) protection process is triggered. This process starts by setting [SOCC] in ***PF Alert*** for *SOC Chg Time*. If the SOCC condition clears prior to the expiration of the *SOC Chg Time* timer, then the [SOCC] is cleared in ***PF Alert*** and with no [SOCC] being set in ***PF Status***. If the SOC condition does not clear, then [SOCC] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET ware all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOCC] in *Permanent Fail Cfg* then the Safety Output pins is activated which is intended to blow a fuse
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and should be set to a current above *OC(2nd Tier) Chg*. It is not necessarily required to set above *AFE OC Chg* which is a fast acting fault condition meant for high current spike detection. This function is meant to be a permanent condition, and it is recommended that [XSOCC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Chg Time

See *SOC Chg*. This is a buffer time allotted for an SOCC condition. The timer starts after [SOCC] is set in ***PF Alert***. When it expires, then the bq20z70 forces an [SOCC] in ***PF Status***, and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Chg Time* timer, then the *SOC Chg Time* timer resets without setting [SOCC] in ***PF Status***. If *SOC Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

SOC Dsg

SOC Dsg is a final level of current protection from the bq20z70. This is not related to the 2nd level (AFE) protection because that is a fast acting protection. This is very slow relatively speaking. It is also intended to be permanent. When the discharge current as measured by ***Current*** falls **down** to or **below** a negative of this threshold (– (*SOC Dsg*)) then the Safety Over Current in the discharge direction (SOCD) detection process is triggered. If the SOCC condition clears prior to the expiration of the *SOC Dsg Time* timer, then no [SOCC] is set in ***PF Status***. If the SOC condition does not clear then [SOCD] is set in PF Status. This triggers many permanent protection features as listed here:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOCD] in *Permanent Fail Cfg* then the Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: Care must taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This is the last level of protection and must be set to a current below *OC(2nd Tier) Dsg*. It is not required to set above *AFE OC Dsg* which is a fast acting fault condition meant for high current spike detection. This is meant to be a permanent condition and it is recommended that [XSOCD] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Dsg Time

See *SOC Dsg*. This is a buffer time allotted for an SOCD condition. The timer starts after the Safety Over Current in the discharge direction (SOCD) detection process is triggered. When it expires then the bq20z70 forces an [SOCD] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Dsg Time* timer then the *SOC Dsg Time* timer resets without setting [SOCD] in ***PF Status***. If *SOC Dsg Time* is 0 then this function is disabled

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

Temperature

SOT Chg

SOT Chg is a final level of temperature protection from the bq20z70. This fault condition is intended to be permanent. When the temperature as measured by ***Temperature*** rises to or above this threshold while charging ([DSG] cleared in ***Battery Status***), then the Safety Over Temperature in the Charge direction (SOTC) detection process is triggered. If the SOTC condition clears prior to the expiration of the *SOT Chg Time* timer, then the no [SOTC] is set in ***PF Status***. If the SOT condition does not clear then [SOT] is set in ***PF Status***. This triggers many permanent protection features as listed here:

1. The Charge FET, Discharge FET, and Pre-Charge FET ware all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOTC] in *Permanent Fail Cfg* then the Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a temperature above *Over Temp Chg*. This is meant to be a permanent condition and it is recommended that [XSOTC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOT Chg Time

See *SOT Chg*. This is a buffer time allotted for a Safety Over Temperature Condition. The timer starts after [SOTC] is set in ***PF Alert***. When it expires, then the bq20z70 forces an [SOTC] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOT Chg Time* timer, then [SOTC] is cleared in ***PF Alert***, and the *SOT Chg Time* timer resets without setting [SOTC] in **PF Status**. If *SOT Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

SOT Dsg

SOT Dsg is a final level of temperature protection from the bq20z70. This fault condition is intended to be permanent. When the temperature as measured by ***Temperature*** rises to or above this threshold while discharging ([DSG] set in ***Battery Status***), then the Safety Over Temperature in the discharge direction (SOTD) protection process is triggered. This process starts by setting [SOTD] in ***PF Alert*** for SOT Dsg Time. If the SOTD condition clears prior to the expiration of the *SOT Dsg Time* timer, then the [SOTD] is cleared in ***PF Alert*** and with no [SOTD] being set in ***PF Status***. If the SOT condition does not clear then [SOTD] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all be opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOTD] in *Permanent Fail Cfg* then the Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a temperature above *Over Temp Chg*. This is meant to be a permanent condition, and it is recommended that [XSOTC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOT Dsg Time

See SOT Dsg. This is a buffer time allotted for a Safety Over Temperature Condition. The timer starts after the Safety Over Temperature in the discharge direction (SOTD) detection process is triggered. When it expires, the bq20z70 forces an [SOTD] in ***PF Status***, and opens the Charge FET Discharge FET and Pre-Charge FET if they are on. If the condition clears prior to the expiration of the *SOT Dsg Time* timer, then the *SOT Dsg Time* timer resets without setting [SOTD] in ***PF Status***. If *SOT Dsg Time* is 0, then this function is disabled

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

FET Verification

FET Fail Limit

The *FET Fail Time* register is a buffer time allotted for a FET circuit fault protection algorithm in the bq20z70 that detects potentially hazardous FET circuit damage. In the bq20z70 this is set to ±50 milliAmps and is not adjustable. This fault condition is intended to be permanent and has 2 possible trigger functions that are listed separately here to help prevent confusion.

1. If the Charge and Pre-Charge FET (if enabled) have been commanded to be off for any reason by either the bq20z70 or the bq29330 (any AFE fault condition) and charge current as measured by ***Current*** still exists which is more than 50 milliAmps, then the FET Fault detection process is triggered. If the [CFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then the no [CFETF] is set in ***PF Status***. If the [CFETF] condition does not clear, then [CFETF] is set in ***PF Status***. This triggers many permanent protection features as listed below::
2. If the discharge FET has been commanded to be off for any reason by either the bq20z70 or the bq29330 (any AFE fault condition) and discharge current as measured by ***Current*** still exists which is less than or equal to –50 milliAmps then the *FET Fail Limit* protection process is triggered. If the [DFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then no [DFETF] is set in ***PF Status***. If the [DFETF] condition does not clear then [DFETF] is set in ***PF Status***. This triggers many permanent protection features as listed below:

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if A and [XCFETF] or B and [XDFETF] in *Permanent Fail Cfg* then the Safety Output pins is activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

If *FET Fail Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application, is recommended. The most common values for this register are between 2–5 seconds. The Charge and Discharge FETs arguably have more stress than any other component on the gas gauge PCB. This function is an excellent safety feature to help protect against the possibility of a shorted FET that could be potentially hazardous. This is meant to be a permanent condition and it is recommended that [XCFETF] and [XDFETF] both be set in *Permanent Fail Cfg* with a fuse designed into the application.

AFE Verification

AFE Fail Limit

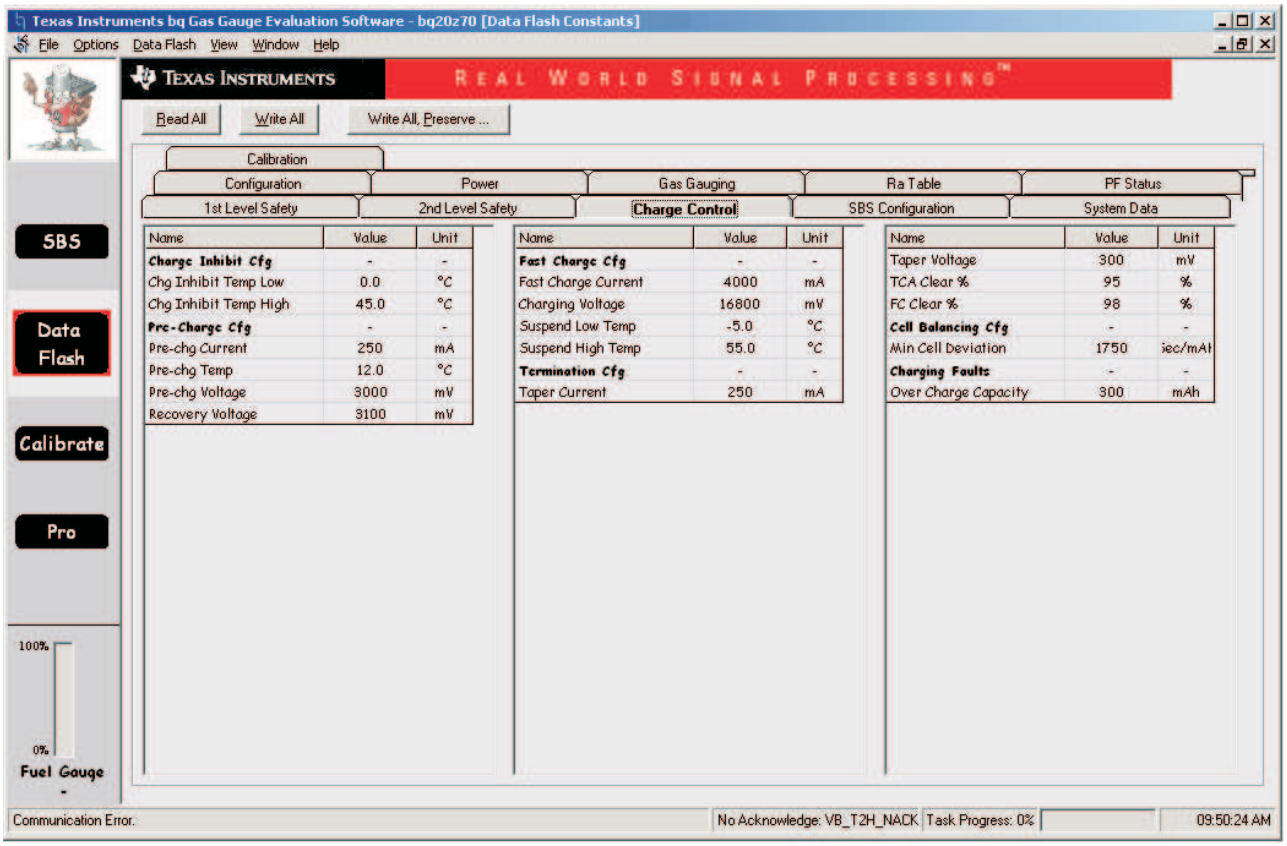
Anytime a communication with the bq29330 is performed over the I^2C bus then an internal counter (for the sake of this document this is referred to as AFE_C Fail Counter) will increment. When the AFE_C Fail Counter increments, the AFE_C Fail detection process is triggered. As long as the AFE_C Fail Counter stays below the *AFE Fail Limit* and above 0, then this detection process is active. During this process, every 20 seconds AFE_C Fail Counter is decremented by 1 until it reaches 0 which will turn off the detection process. If the AFE_C Fail Counter reaches the *AFE Fail Limit*, then [AFE_C] is set in ***PF Status***. Setting *AFE Fail Limit* to 0 disables the AFE_C Fail protection process.

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if A. [XAFE_P] set or if B and [XAFE_C] set in *Permanent Fail Cfg*, then the Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the PF Status class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting:*AFE Fail Limit* defaults to 10. It is very important to note that setting *AFE Fail Limit* to 0 only disables the AFE_C functions. The default of 10 should be appropriate for most applications. This gives sufficient buffer for ESD, resets and other unknown failures that should be recoverable.

3.4 Charge Control



Charge Inhibit Config

Chg Inhibit Temp Low

When the pack temperature measured by ***Temperature*** falls to or below this threshold while discharging ([DSG] flag set in ***Battery Status***), the Charge Inhibit Mode is triggered. This causes ***Charging Current*** and ***Charging Voltage*** to be set to 0, [XCHG] is set in ***Charging Status***, and if [CHGIN] set in *Operation Cfg B*, then Charge FET is turned off and/or the Pre-Charge FET is turned off. There are two primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** rises above (*Charge Inhibit Temp Low* + 5°C).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated with [DSG] flag set in ***Battery Status***.

With either of these recoveries, [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.

Normal Setting: The purpose of this low inhibit temperature is not to suspend charging, but to prevent it from starting when the conditions are not acceptable. This prevents damage to the pack. The default for this is 0 degrees, and can be modified to fit the application.

Chg Inhibit Temp High

When the pack temperature measured by ***Temperature*** rises to or above this threshold while discharging ([DSG] flag set in ***Battery Status***) the Charge Inhibit Mode is triggered. This causes ***Charging Current*** and ***Charging Voltage*** to be set to 0, [XCHG] is set in ***Charging Status***, and if [CHGIN] set in *Operation Cfg B* then Charge FET is turned off and/or the Pre-Charge FET is turned off. There are two primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** falls below (*Charge Inhibit Temp Low – Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated with [DSG] flag set in ***Battery Status***.

With either of these recoveries, [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.

Normal Setting: The purpose of this high inhibit temperature is not to suspend charging but to prevent it from starting when the conditions are not acceptable. This prevents damage to the pack. The default for this is 45°. Notice that this is less than the default charge suspend mode (see *Suspend High Temp*).

Pre-Charge Config

Pre-Charge Current

This is the current that the bq20z70 reports in the ***Charging Current*** register when the bq20z70 is in Pre-Charge mode (see *Pre-Chg Temperature* and *Pre-Chg Voltage*). This current is broadcast to a smart charger when bq20z70 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Pre-Charge Mode (***Charging Current*** = *Pre-Charge Current*), [PCHG] is set in ***Charging Status***, then the appropriate charging FET is enabled as set with [ZVCHG1] and [ZVCHG0] in *Operation Cfg A*.

Table 18. FET Control Bits in *Operation Cfg A*

ZVCHG1	ZVCHG0	FET Used
0	0	ZVCHG
0	1	CHG
1	0	OD
1	1	No Action

There are three primary recoveries from Pre-Charge mode:

1. Independent of the method (*Pre-Chg Voltage* or *Pre-Chg Temperature*) that caused the Pre-Charge Mode:
   a. ***Cell Voltage (All)*** must be above *Recovery Voltage*
   b. ***Temperature*** must be above (*Pre Chg Temperature* + *5°C*)

   Either of these conditions cause the bq20z70 to enter Fast Charge Mode (See *Fast Charge Current*)
2. Pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated with any of the Pre-Charge criteria.
3. This is considered a recovery, but it is really a transition from one mode to another. A charge suspend condition (see *Suspend High Temp* and *Suspend Low Temp*) which forces the bq20z70 to transition from Pre-Charge Mode to Charge Suspend Mode.

Normal Setting: This register is application dependent. If a Pre-Charge FET and a current limiting resistor is used to control the current allowed into the battery during Pre-Charge Mode ([ZVCHG1] and [ZVCHG1] both equal 0), then this register accuracy is not as important as if it were used for a smart charger which initiate a current equal to the requested Pre-Charge current. It is important to note that use of the OD pin is not recommended because it does not have limiting circuitry to ensure "hard" on control for a Zero Volt charging condition. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is always recommended.

Pre-Chg Temp

See *Pre-Charge Current*. With either the *Pre-Chg Voltage* or the *Pre-Chg Temperature* criteria being met, then the bq20z70 triggers Pre-Charge Mode. With ***Temperature*** falling to or below *Pre-Chg Temp*, but above *Charge Inhibit Temp Low*, then the bq20z70 enters the Pre-Charge Mode (see *Pre-Charge Current*).

Normal Setting: Ensure that this register is above the *Charge Inhibit Temp Low* . This ensures that *Pre-Chg Temperature* is above the charge suspend temperature because the charge suspend is below the charge inhibit. (See *Charge Inhibit Temp Low* and *Charge Suspend Temp Low*). At cold temperatures, lower currents are better for the battery cells. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Pre-Chg Voltage

See *Pre-Charge Current*. With either the *Pre-Chg Voltage* or the *Pre-Chg Temperature* criteria being met, then the bq20z70 triggers Pre-Charge Mode. With ***Cell Voltage (Any)*** falling to or below *Pre-Chg Voltage*, then the bq20z70 enters Pre-Charge Mode (see *Pre-Charge Current*).

Normal Setting: Ensure that this voltage is set per the battery cell specifications. Setting this value too high is not harmful (except for slower charging from empty), but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage which brings them up to a normal charging voltage before hitting them with a fast current. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Recovery Voltage

If the battery pack is in Pre-Charge mode due to ***Cell Voltage (Any)*** falling to or below *Pre-Chg Voltage*, then it exits the Pre-Charge mode and enter the Fast Charge Mode (see *Fast Charge Current*) when ***Cell Voltage (All)*** rises above *Recovery Voltage*. This is one of three primary recovery methods for a battery pack in Pre-Charge mode.

Normal Setting: This is battery cell dependent. Ensure that it is set per the battery cell specifications. Setting this value too high is not harmful (except for slower charging from empty), but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage which brings them up to normal charging voltage before hitting them with a fast current. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Fast Charge Config

Fast Charge Current

This is the current that the bq20z70 reports in the ***Charging Current*** register when the bq20z70 is in Fast Charge mode (see *Pre-Chg Temperature*, *Pre-Chg Voltage*, and *Pre-Chg Current*). This current is also broadcast to a smart charger when bq20z70 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Fast Charge Mode (***Charging Current*** = *Fast Charge Current*), [FCHG] is set in ***Charging Status*** and the Charge FET is enabled.

There are three primary criteria that must be met to be in Fast Charge Mode:

1. Assuming all temperature faults are configured correctly (*Pre-Chg Temperature* configured in Data Flash as the highest low temperature mode), ***Temperature*** is above *Pre-Chg Temperature* with [PCHG] clear in ***Charging Status***
2. ***Temperature*** is below *Suspend High Temp* and no [CHGSUSP] in ***Charging Status***
3. ***Voltage*** must be above *Pre-Chg Voltage* with [PCHG] clear in ***Charging Status***
4. ***Voltage*** must be below ***Charging Voltage*** + *Over Charging Voltage*

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

Charging Voltage

When in any charging mode without a fault condition present, the *Charging Voltage* is the voltage that is put in ***Charging Voltage***. With most fault conditions ***Charging Voltage*** is set to 0. This is also used in bq20z70 charge qualification and termination algorithms.

Normal Setting: This register is normally set based on the charger specifications. Charger tolerances are considered when setting this register.

Suspend Low Temp

When the pack temperature measured by ***Temperature*** falls to or below *Suspend Low Temp* while charging ([DSG] flag clear in ***Battery Status***), then the Charge Suspend Mode is triggered. This causes ***Charging Current*** to be set to 0, [CHGSUSP] is set in ***Charging Status***, and if [CHGSUSP] set in *Operation Cfg B*, then the Charge FET and Pre-Charge FET are both opened regardless of their prior open/close state. There are two primary possible recoveries to this mode

1. The primary recovery is if ***Temperature*** rises above (*Suspend Low Temp* + 5°*C*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the suspend mode is reactivated with [DSG] flag cleared in ***Battery Status***.

With either of these recoveries, [CHGSUSP] is cleared in ***Charging Status***. This enables the charging process to resume.

Normal Setting: Notice that default *Suspend Low Temp* is lower than *Chg Inhibit Low Temp*. This value is application and battery cell dependent.

Suspend High Temp

When the pack temperature measured by ***Temperature*** rises to or above *Suspend High Temp* while charging the ([DSG] flag in ***Battery Status***), then the Charge Suspend Mode is triggered. This causes ***Charging Current*** to be set to 0, [CHGSUSP] is set in ***Charging Status***, and if [CHGSUSP] set in *Operation Cfg B*, then the Charge FET and Pre-Charge FET are both opened regardless of their prior open/close state. There are two primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** falls below (*Suspend High Temp* – 5°).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the suspend mode is reactivated with [DSG] flag cleared in ***Battery Status***.

With either of these recoveries, [CHGSUSP] is cleared in ***Charging Status***. This enables the charging process to resume.

Normal Setting: Notice that default *Suspend High Temp* is higher than *Chg Inhibit High Temp*. This value is application and battery cell dependent.

Termination Config

Taper Current

Taper Current is used in the Primary Charge Termination algorithm. ***Current*** is integrated over each of the two consecutive periods of 40 seconds each separately and then they are averaged separately to give 2 averages. Both of these averages must be below the *Taper Current* to qualify for a Primary Charge Termination. In total, a primary charge termination has the following requirements:

1. ***Voltage*** must be above (*Charging Voltage* – *Taper Voltage*) for the bq20z70 to start trying to qualify a termination. It must be above this voltage before bq20z70 starts trying to detect a primary charge termination.
2. An average of all ***Current*** measurements must be below *Taper Current* for two consecutive periods of 40 seconds from beginning to end of each window.
3. An average of all ***Current*** measurements during each of two consecutive periods of 40 seconds from beginning to end of each window must be above 0.25mAh as integrated and averaged over the two consecutive 40 second windows.

When these conditions are met, the primary charge termination has occurred and the following happens:

1. [TCA] is set in ***Battery Status*** and either of the following happens:
   a. if [CHGFET] set in *Operation Cfg B* then and ***Charging Current*** is set to 0, and the Charge FET is opened.

b. if [CHGFET] is cleared in *Operation Cfg B* then and ***Charging Current*** is set to 0.

2. [FC] is set in ***Battery Status***
3. If [CSYNC] is set in *Operation Cfg B*, then ***Remaining Capacity*** is written to ***Full Charge Capacity***.

The primary charge termination mode has two clearing methods:

1. It is cleared when ***RSOC*** falls below *FC Clear %*
2. if [CHGTERM] in *Operation Cfg B* set, and ***Current*** is less than *Chg Current Threshold* for two consecutive periods of 40 seconds.

Normal Settings: This register is dependent on battery cell characteristics and charger specifications. ***Average Current*** is not used for this qualification because its time constant is not long enough which is why we use 2 consecutive 40 second windows. The reason for making 2 Current Taper qualifications is to prevent false current taper qualifications. False primary terminations can happen with pulse charging and with random starting and stopping of the charge current. This is particularly critical at the beginning or end of the qualification period. .

Taper Voltage

During Primary Charge Termination detection, one of the 3 requirements is that ***Voltage*** must be above (*Charging Voltage – Taper Voltage*) for the bq20z70 to start trying to qualify a termination. It must be above this voltage before bq20z70 starts trying to detect a primary charge termination.

Normal Setting: This value is dependent on charger characteristics. It needs to be set so that ripple voltage, noise, and charger tolerances are taken into account. A value selected too low can cause early termination. If the value selected is too high, then it can cause no or late termination detection. A good example value is 200mV (see *Taper Current*).

TCA Clear %

If during discharge ([DSG] set in ***Battery Status***), ***RSOC*** falls below this value, then [TCA] is cleared.

Normal Setting: Application dependant.

FC Clear %

If during discharge ([DSG] set in ***Battery Status***), ***RSOC*** falls below this value, then [FC] is cleared.

Normal Setting: Application dependant.

Cell Balancing Config

Min Cell Deviation

The cell balancing algorithm with be active only during charging ([DSG] cleared in ***Battery Status***). The function is disabled completely if *Min Cell Deviation* is set to 0. With impedance track, the bq20z70 knows the Full Charge Capacity for each cell independently. Each cell input in the bq29330 has an internal FET that shorts the cell filtering resistors, and an internal 500-Ω resistor across the cells that need reduced charging to help balance the cells. The bq20z70 use impedance track information along with the value for *Min Cell Deviation* to know how long to turn on the shorting FET. The algorithm works based on the formula:

Min Cell Deviation = dQ × R / (V × duty cycle)

Where:

dQ = correction factor = 3600 seconds/hour

V = nominal cell voltage = 3600 mV

duty cycle = 40% = 0.4

R = Total resistance from cell top to cell bottom (2 filter resistors and internal 500-Ω resistor), so for the bq20z70 EVM, the filter resistors are 100 Ω; therefore, R = 100 × 2 + 500 = 700 Ω

So for 700 Ω in resistance *Min Cell Deviation* = 1750 sec/mAh

Normal Setting: The bq20z70 default value for this register is 1750s/mAH. The only values that is needed to be changed in the formula are R (Resistance), and V (nominal cell voltage). (See SLUA340 for more information)

Charging Faults

Over Charge Capacity

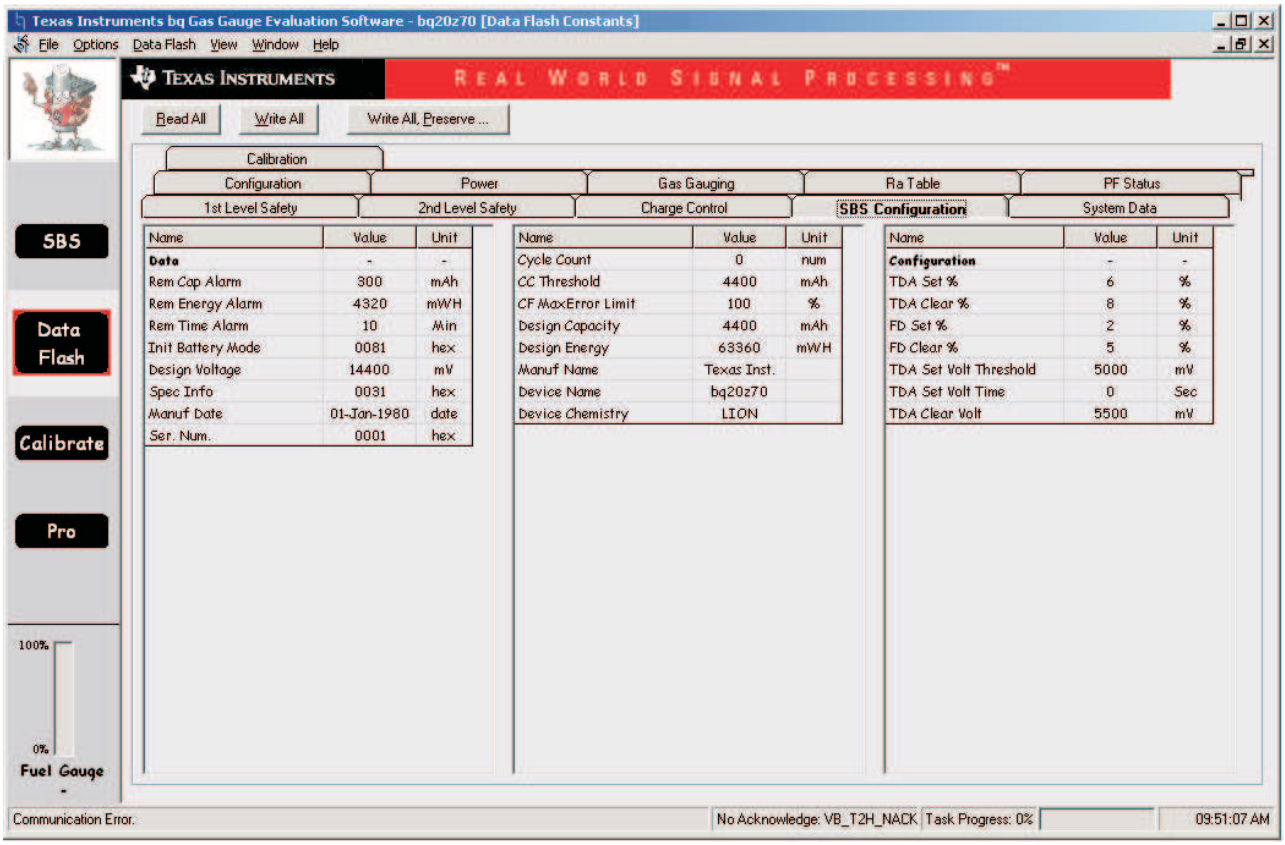
Over Charge Capacity is detected in a two-step process. First the battery must be charged to the point where Remaining Capacity reaches ***FCC*** (***Full Charge Capacity***). Then any charge applied after this point is still measured but not displayed by the bq20z70. When this charge as measured by the bq20z70 reaches a threshold as defined by ***FCC*** + *Over Charge Capacity*, then the bq20z70 goes into a charging fault condition. The [OC] in ***Charging Status*** is set. ***Charging Voltage*** and ***Charging Current*** are both set to 0. If [OC] set in *Charge Fault Cfg*, then the Charge FET is turned off.

There are three recovery methods for the bq20z70.

1. The first only happens if [NR] in *Operation Cfg B* is set. With this setting the bq20z70 will recover from an overcharged condition with a continuous discharge of 2 mAHs.
2. With [NR] cleared in *Operation Cfg B*, the bq20z70 recovers from the overcharge fault with a pack removal and reinsertion ($\overline{\text{PRES}}$ transition).
3. The third recovery happens when ***RSOC*** falls below the *FC Clear %*. This recovery also is the only one that returns ***Charging Voltage*** and ***Charging Current*** to normal.

Normal Setting: This register is application dependent but a good example is 100 to 300 mAh for each cell in parallel. To small of a value could force false detections, and to large a value could damage the cells if normal charge termination methods fail.

3.5 SBS Configuration



SBS Data

Rem Cap Alarm

When the ***Remaining Capacity*** falls below this value, [RTA] is set in ***Battery Status***.

Normal Setting: About 10% of the *Full Charge Capacity*. This value is programmed into ***RemainingCapacityAlarm*** on device initialization

Rem Energy Alarm

When the bq20z70 is in milliwatt mode ([CapM] set in ***Battery Mode***), the value in *Rem Energy Alarm* is written to the ***Rem Cap Alarm***. Once this value is written to ***Rem Cap Alarm***, then the function acts the same as *Rem Cap Alarm* except units are in milliwatts. (See *Rem Cap Alarm*)

Normal Setting: About 10% of the *Full Charge Capacity* but units have to be converted to milliwatts. This data flash value is only used when in milliwatt mode. This value is programmed into *RemainingCapacityAlarm* on device initialization if in milliwatt mode.

Rem Time Alarm

When the average time to empty falls below this value, then the [RTA] flag is set in ***Battery Status***.

Normal Setting: Approximately 10 minutes. This value is programmed into ***RemainingTimeAlarm*** on device initialization.

Init Battery Mode

This is the default value loaded into ***Battery Mode*** on all resets, and when the bq20z70 wakes from sleep. The primary purpose of having an initial value for this register is to enable milliwatt mode whenever the bq20z70 resets or wakes up from sleep.

Normal Setting: In most applications, this register should be 0x0081. If the application requires the bq20z70 to wake in mW mode, then this value can be set to 0x8081. Care should be taken with this setting; however, because the ***Battery Mode*** register is writable even when the bq20z70 is sealed. The mW mode bit can be accidentally written to a 0.

Design Voltage

This is the theoretical nominal voltage of the battery pack. This value is used in ***ATRATE*** calculations and milliWatt mode (***Battery Mode*** MSByte bit 7).

Normal Setting: This varies by cell manufacturer, but Li-Ion is normally about 3.6-V per cell. See the cell manufacturer data sheet for the exact numbers. This value is programmed into ***DesignVoltage*** on device initialization.

Spec Info

This performs two purposes. The high byte has the current and voltage multipliers. The bq20z70 does not require any multiplier, so use 0x00. The low byte is the SBS specification revision. See the SBS Implementers Forum web page for more information (http://www.sbs-forum.org/specs/index.html).

Normal Setting: 0x0031 for SBS specification v1.1 with PEC error checking, or 0x0021 for SBS specification V1.1 without PEC error checking.

Mfg Date

This is the date of manufacture. It is stored in the Data Flash in packed format. All bqEV Software and bqMTester both accept input of this date in standard date format so the packed format does not need to be used input. It is then translated by the software to packed format. This data does not affect the operation, nor is it used by the part in any way.

Ser Num

This is a 16 bit serial number that does not affect the operation nor is it used by the part in any way. It is normally used for battery identification.

Cycle Count(CC)

Cycle Count Threshold is used to increment Cycle Count. When the bq20z70 accumulates enough discharge capacity equal to the *Cycle Count Threshold* then it increments *Cycle Count* by 1. This discharge capacity does not have to be consecutive. In other words the internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *Cycle Count Threshold*. Then *Cycle Count* is incremented. Every increment of *Cycle Count* between QMAX updates will increment ***MaxErr*** by 0.05%. It takes 20 increments of Cycle Count to increment ***MaxErr*** by 1% so that it is visible in the SBS register.

Normal Setting: This should be set to 0.

Cycle Count Threshold

Cycle Count Threshold is used to increment Cycle Count. When the bq20z70 accumulates enough discharge capacity equal to the *Cycle Count Threshold*, then it increments *Cycle Count* by 1. This discharge capacity does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *Cycle Count Threshold* and increments *Cycle Count*.

Normal Setting: This is normally set to about 80% of the *Design Capacity*.

CF Max Error Limit

The bq20z70 forces [CF] to be set in ***Battery Mode*** if ***MaxErr*** goes above the value stored in this register. This value is used to give an alternate method for setting the [CF] flag in ***Battery Mode***, other than the impedance track algorithm. The [CF] flag is a condition request flag indicating the battery would like a full charge/discharge cycle, and rarely is set by impedance track because accurate capacity measurements are always updated.

Normal Setting: This register is normally set to 100 and is in units of %.

Design Capacity

Design Capacity is the data flash location that is reported in the ***Design Capacity*** register when [CapM] is clear in ***Battery Mode***. If [CapM] is set in ***Battery Mode***, then *Design Energy* is reported in ***Design Capacity***. This value is used also for the ***ASOC*** calculation by the bq20z70 if [CapM] is cleared in ***Battery Mode***.

Normal Setting: This value should be set based on the application battery specification. See the battery manufacturer data sheet.

Design Energy

Design Energy is the data flash location that is reported in the ***Design Capacity*** register if [CapM] is set in ***Battery Mode***. If [CapM] is clear in ***Battery Mode***, then *Design Capacity* is reported in *Design Capacity*. This value is used also for the ASOC calculation by the bq20z70 if [CapM] is set in ***Battery Mode***.

Normal Setting: This value is be set based on the application battery specification. See the battery manufacturer data sheet. At higher rates of discharge, energy is less, so referring to discharge data similar to the typical rate of the user's application is important to obtain a meaningful value.

Manuf Name

String data that can be a maximum of 11 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x20.

Device Name

String data that can be a maximum of 7 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x21.

Device Chemistry

String data that can be a maximum of 4 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x22.

Configuration

These are alternative methods for setting and clearing [TDA] and [FD] in ***Battery Status***. They are in addition to traditional methods or fault conditions explained in other areas of this document.

TDA Set %

If set to a value between 0 and 100 then when ***RSOC*** falls to or below this value, then [TDA] in ***Battery Status*** is set. If set to (–)1, then this function is disabled. *TDA Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference. This is the threshold that the bq20z70 requests that discharge be halted because the battery is nearing depletion. If used, it is normally set around 6%. Be sure that if *TDA Clear %* is used, then this should be used as well. They only work together.

TDA Clear %

If set to a value between 0 and 100 then when ***RSOC*** rises to or above this value after being set by *TDA Set %*, then [TDA] in ***Battery Status*** is cleared. This register can only be used to clear [TDA] if it was set by TDA Set %. If set to (–)1, then this function is disabled. *TDA Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 8%. Be sure that if *TDA Set %* is used then this should be used as well. They only work together.

FD Set %

If set to a value between 0 and 100 then when ***RSOC*** falls to or below this value then [FD] in ***Battery Status*** is set. If set to (–)1 then this function is disabled. *FD Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [FD] is completely unaffected by this register.

Normal Setting: This is user preference. This is a stronger request than TDA. The battery is presumed dead at this point. If used it is normally set around 2%. Be sure that if FD *Clear %* is used then this should be used as well.

FD Clear %

If set to a value between 0 and 100 then when ***RSOC*** rises to or above this value after being set by *FD Set %*, then [FD] in ***Battery Status*** is cleared. If set to (–)1, then this function is disabled. *FD Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 5%. If FD Set % is used, then this should be used as well. They only work together.

TDA Set Volt Threshold

When battery voltage as measured by ***Voltage*** falls to or below the *TDA Set Volt Threshold* value for *TDA Set Volt Time* seconds, then [TDA] in ***Battery Status*** is set. This works completely independent of *TDA Set %*. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 6% ***RSOC***.

TDA Set Volt Time

See *TDA Set Volt*. This is the time that the battery voltage must be equal to or below *TDA Set Volt Threshold* before [TDA] is set in ***Battery Status***.

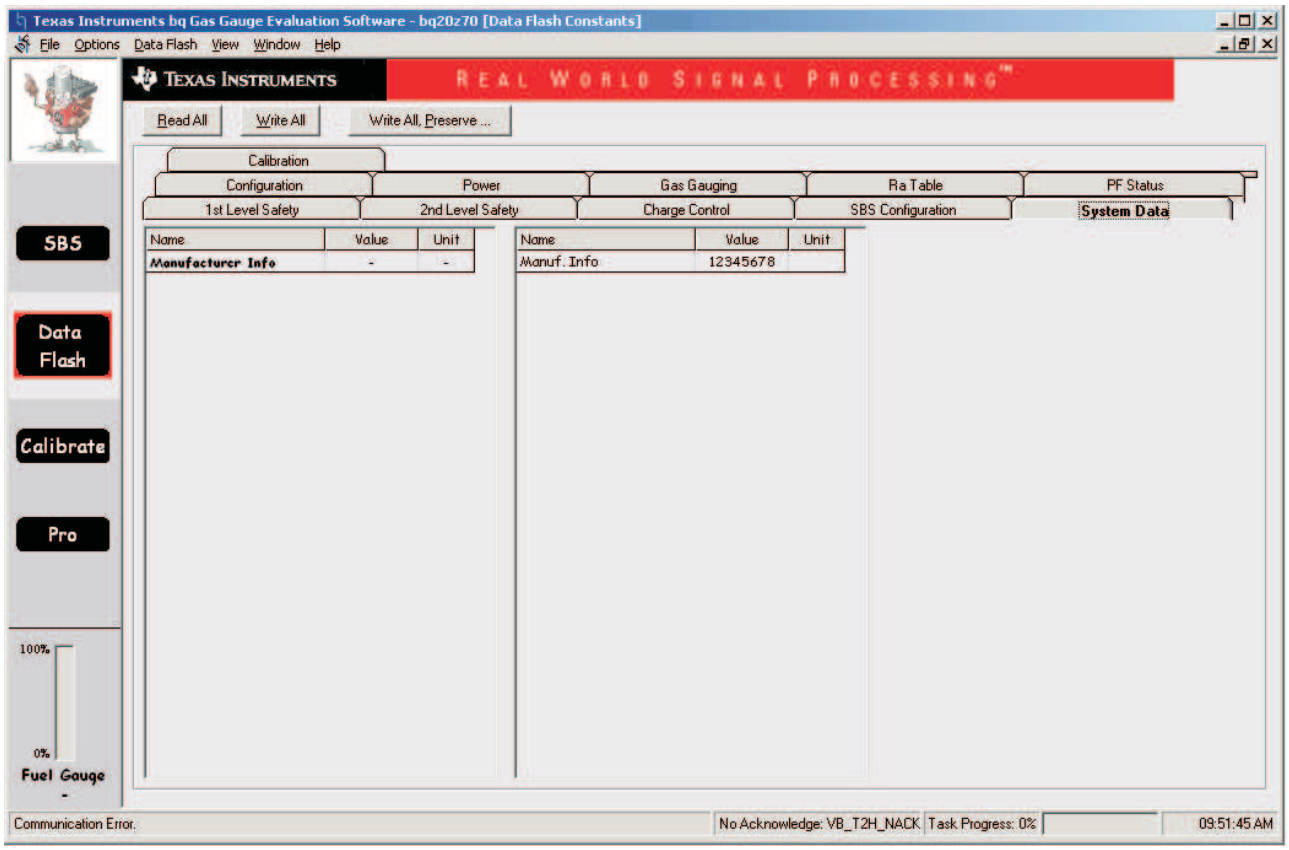
Normal Setting: This is normally set to 5 seconds but depends on the application.

TDA Clear Volt Threshold

When battery voltage (as measured by ***Voltage***) rises to or above this value, then [TDA] in ***Battery Status*** is cleared. [TDA] is only cleared with this threshold if it was set by *TDA Set Volt* criteria. It is not cleared if it was set by any other methods.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 8% ***RSOC***.

3.6 System Data



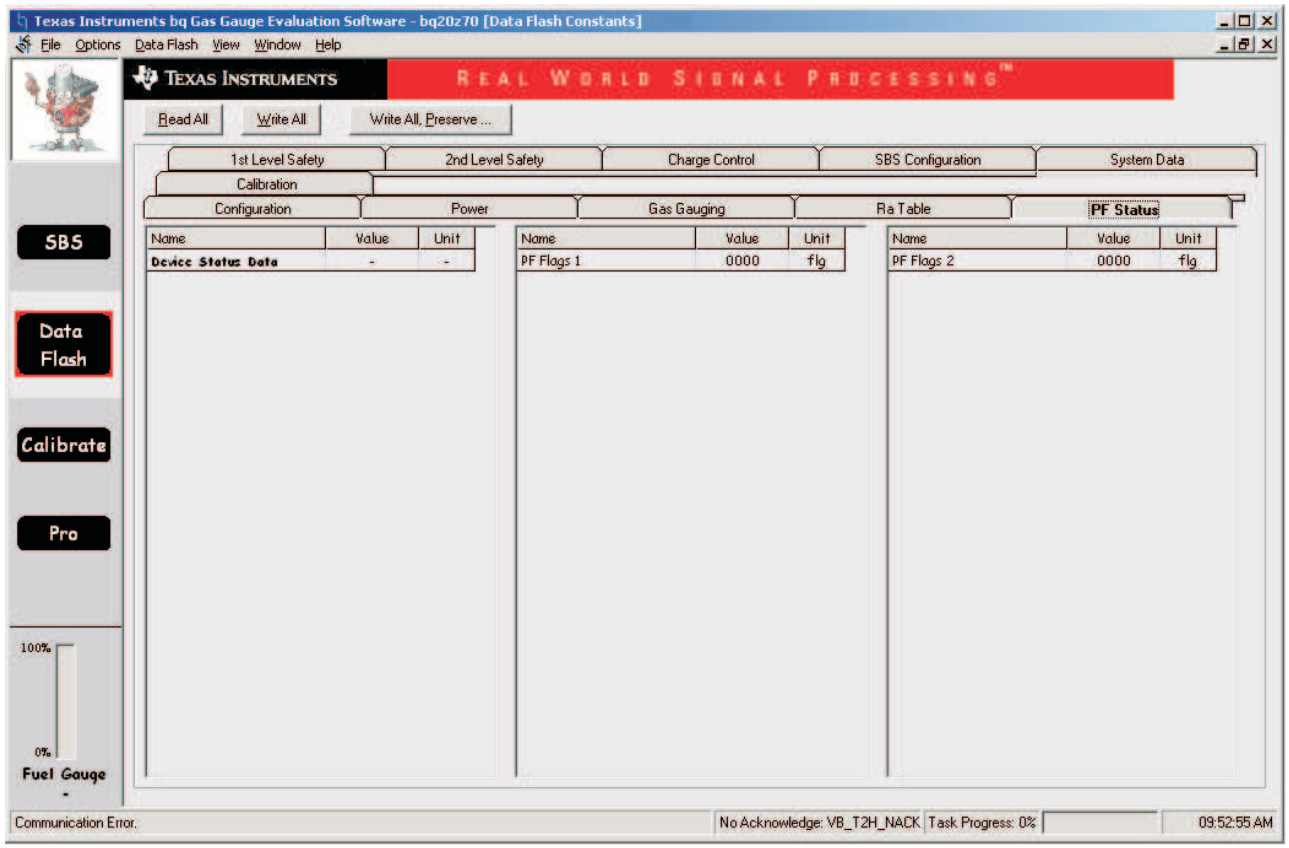
Manufacturer Info

Manuf. Info

This is string data that can be any user data. It can be a maximum of 8 characters.

Normal Setting: Can be used for any user data.

3.7 PF Status



There is no configuration or settings required for the PF Status Class. The entire PF Status class should all be zeros for every register. This class is intended only for reporting failure information to the factory and Texas Instruments. In fact, it only reports any information with catastrophic failures or during development time as a tool to help with configuration or layout issues.

Device Status Data

PF Flags 1

This location indicates all the causes of permanent failures that have occurred from the time the bq20z70 was last programmed with new firmware or the last time this register was cleared. It is important to understand that more than one fault can be recorded here if multiple faults have occurred. *PF Flags 1* bit locations and definitions correspond to ***PF Status***. If the corresponding bit in PF Flags 1 is enabled in the *Permanent Fail Cfg* register, then the bq20z70 attempts to blow the fuse in addition to record the permanent failure in the *PF Flags 1 register*. This register is cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z70 (See the bq20z70 data sheet). This is the only register in the data flash which ignores the disabled data flash writing setting when a permanent failure occurs. (See *Permanent Fail Cfg*)

—	PFVSHUT	—	—	SOCD	SOCC	—	AFE_C
DFF	DFETF	CFETF	CIM	SOTD	SOTC	SOV	PFIN

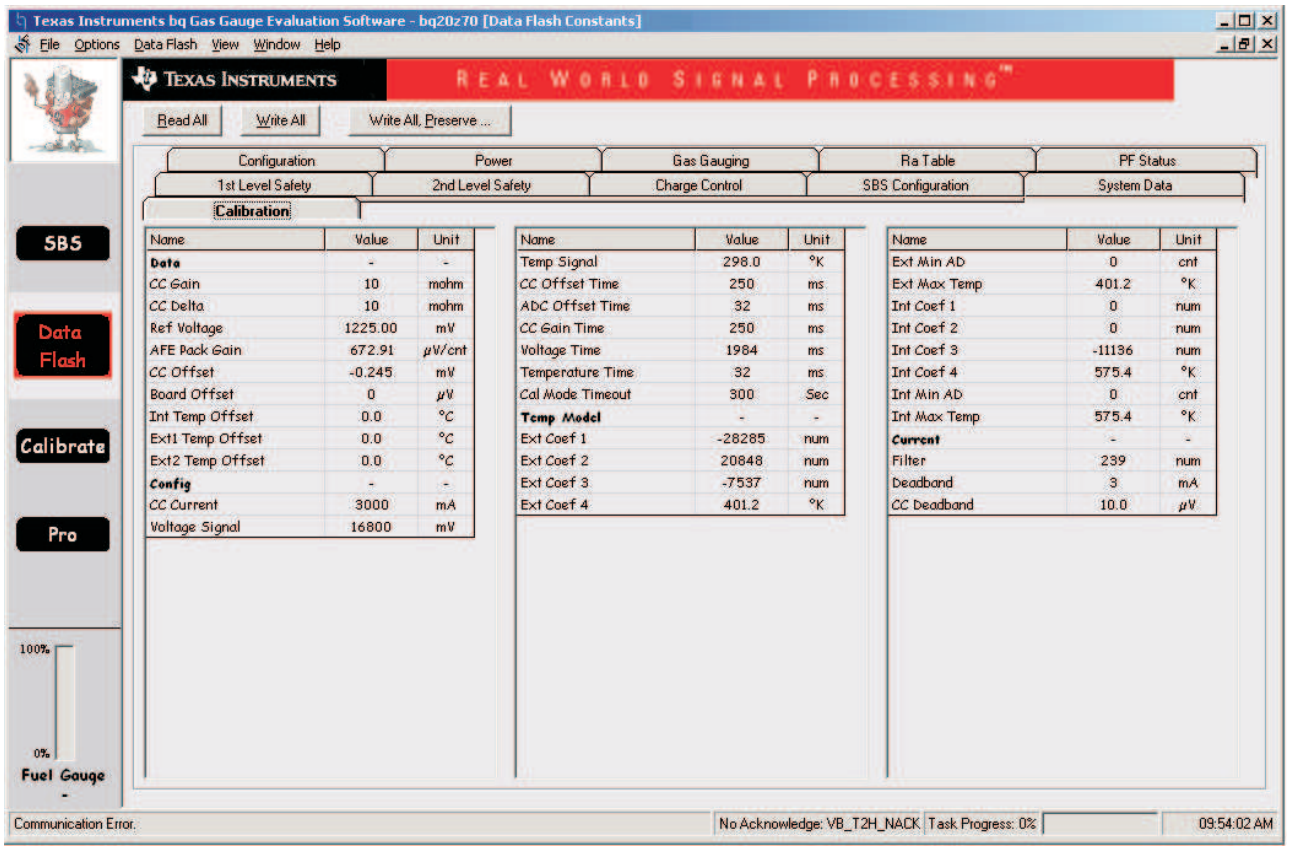
- PFVSHUT: This bit causes much confusion for customers. At first, the attempt was to label it reserved, but there were many questions on its function. It serves no purpose in the operation of the bq20z70 but it does get set periodically. It does not function like any of the other PF Flags in that it there does not necessarily have to be a permanent failure for this flag to be set. It is basically a “shutdown” process monitor bit. When the bq20z70 starts the shutdown process, then it sets this bit. When it wakes, this bit is cleared. If this bit is set and then a real permanent failure occurs during the shutdown process, then this bit is set along with the bit that indicates the actual permanent failure.

- SOCD: Set if a Safety Over Current Discharge Fault has occurred and the function is enabled. If *SOC Dsg Time* is set to 0, then this function is disabled. If [XSOCD] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high. (See *SOC Dsg*).
- SOCC: Set if a Safety Over Current Charge Fault has occurred, and the function is enabled. If *SOC Chg Time* is set to 0, then this function is disabled. If [XSOCC] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high (See *SOC Chg*).
- AFE_C: Set if an AFE Communication Fault has occurred. If *AFE Fail Limit* is set to 0, then this function is disabled. If [XAFE_C] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high (See *AFE Fail Limit*).
- DFF: The bq20z70 verifies all data flash writes and will set [DFF] if a Data Flash Verify Fault has occurred Only the setting of [DFF] can be disabled. If [XDFF] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high.
- DFETF: Set if a Discharge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XDFETF] is set in *Permanent Fail Cfg* then the SAFE pin is driven high. (See *FET Fail Time*).
- CFETF: Set if a Charge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XCFETF] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high. (See *FET Fail Time*).
- CIM: Set if a Cell Imbalance Fault has occurred and the function is enabled. If *Battery Rest Time* is set to 0, then that function is disabled. If [XCIM] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high. (See *Battery Rest Time*).
- SOTD: Set if a Safety Over Temperature Discharge Fault has occurred and the function is enabled. If *SOT Dsg Time* is set to 0, then this function is disabled. if [XSOTD] is set in *Permanent Fail Cfg,* then the SAFE pin is driven high. (See *SOT Dsg*).
- SOTC: Set if a Safety Over Temperature Charge Fault has occurred and the function is enabled. If *SOT Chg Time* is set to 0, then this function is disabled. If [XSOTC] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high. (See *SOT Chg*).
- SOV: Set if a Safety Over Voltage Threshold Fault has occurred and the function is enabled. If *SOV Time* is set to 0, then this function is disabled. if [XSOV] is set in *Permanent Fail Cfg*, then the SAFE pin is driven high. (See *SOV Threshold*).
- PFIN: The bq20z70 monitors the PFIN line. When the PFIN line goes low for *PFIN Detect Time*, then the bq20z70 attempts to report a PFIN Fault if the function is enabled. If *PFIN Detect Time* is set to 0, then this function is disabled. if [XPFIN] is set in *Permanent Fail Cfg*, then the SAFE pin is driven. (See *PFIN Detect Time*)

PF Flags 2

This register reports the first permanent failure that occurred from the time the bq20z70 was last programmed with new firmware. The difference between this register and PF Flags 1 is that this register only records one failure, and it is the first one in a possible series of failures. This method gives a better chance to learn what could have caused a whole series of failures by knowing what the first failure was.

3.8 Calibration



Data

Most of these values should never need to be modified by the user. They should only be modified by the Calibration commands in Calibration mode as explained in the *Callibration Application Note* SLUA379.

CC Gain

This is the gain factor for calibrating out Sense Resistor, Trace, and Internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports ***Current***. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports Current cancels out the time base since ***Current*** does not have a time component (it reports in mA) and *CC Delta* requires a time base for reporting ***Remaining Capacity*** (it reports in mAh).

Normal Setting: *CC Gain* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the latest calibration application note for the bq20z70 (SLUA379: Data Flash Programming and Calibrating the bq20z70 and bq20z90 Family of Gas Gauges) for more information on calibration.CC Gain

CC Delta

This is the gain factor for calibrating out Sense Resistor, Trace, and internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports charge and discharge in and out of the battery through the ***Remaining Capacity*** register. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports ***Current*** cancels out the time base since ***Current*** does not have a time component (it reports in mA) and *CC Delta* requires a time base for reporting ***Remaining Capacity*** (it reports in mAh).

Normal Setting:*CC Delta* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the latest calibration application note for the bq20z70 (SLUA379: *Data Flash Programming and Calibrating the bq20z70 and bq20z90 Family of Gas Gauges*) for more information on calibration.

Ref Voltage

The *Ref Voltage* is based on the actual reference voltage that the bq29330 uses for reference when sending voltage readings to the bq20z70. Therefore, this is a required constant in all the bq20z70 voltage computation formulas for displaying individual cell voltages (***Cell Voltage 1-4***) and the computed battery voltage (***Voltage***) in millivolts. By tweaking this value before it is used in the voltage computation formulas, the errors introduced by the bq20z70 ADC and bq29330 reference are canceled out before they affect the reported voltages.

Normal Setting:*Ref Voltage* should never need to be modified by the user. It is modified by the voltage calibration command in Calibration mode. See the latest calibration application note for the bq20z70 (SLUA379: *Data Flash Programming and Calibrating the bq20z70 and bq20z90 Family of Gas Gauges*) for more information on calibration.

AFE Pack Gain

The *AFE Pack Gain* is used for calibrating out errors in the bq29330 reference and bq20z70 ADC. It is used for reporting the ***Pack Voltage*** as measured on the PACK pin of the bq29330. Therefore, this is a required constant in all the bq20z70 voltage computation formulas for displaying ***Pack Voltage*** in millivolts. By tweaking this value before it is used in the voltage computation formulas, it changes the gain of the reported voltage which gives a method for calibrating this reported voltage.

Normal Setting: AFE Pack Gain may not need to be calibrated depending on the application. Unless ***Pack Voltage*** is used for display by the application then it is only used for charger detection, and it does not need to be accurate for function. *AFE Pack Gain* should never need to be modified by the user. It is modified by the pack voltage calibration command in Calibration mode. See the latest calibration application note for the bq20z70 (SLUA379: *Data Flash Programming and Calibrating the bq20z70 and bq20z90 Family of Gas Gauges*) for more information on calibration.

CC Offset

There are 2 offsets for calibrating the offset of the internal Coulomb Counter, board layout, sense resistor, copper traces and other offsets from the Coulomb Counter readings. *CC Offset* is the calibration value that primarily corrects for the offset error of the bq20z70 Coulomb Counter circuitry. The other offset calibration is *Board Offset* described below. To minimize external influences when doing *CC Offset* calibration either by either automatic *CC Offset* calibration or by the *CC Offset* calibration function in Calibration Mode an internal short is places across the SR1 and SR2 pins inside the bq20z70. *CC Offset* is a correction for very small noise/errors; therefore, to maximize accuracy, it takes about 20 seconds to calibrate out the offset. Since it is not practical to do a 20 second offset during production, 2 different methods for calibrating CC Offset were developed.

1. The first method is to calibrate CC Offset by the putting the bq20z70 in Calibration Mode and initiating the CC Offset function as part of the entire bq20z70 calibration suite. See the SLUA379 for more information on Calibration Mode. This is a short calibration that is not as accurate as the second method described below. Its primary purpose is to calibrate CC Offset so that it will not affect any other Coulomb Counter calibrations. This is only intended as a temporary calibration because the automatic calibration described below is done the first time SMBus is low for more than 20 seconds which is a more accurate calibration.
2. During normal Gas Gauge Operation (***Temperature*** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*) when the SMBus clock and data lines are low for more than *Bus Low Time* seconds and ***Current*** is less than *Sleep Current* in milliAmps then an automatic *CC Offset* calibration is performed. This takes around 16 seconds and is much more accurate than the method in Calibration mode.

Normal Setting: *CC Offset* should never be modified directly by the user. It is modified by the current calibration function from Calibration Mode or by Automatic Calibration. See the latest calibration application note for the bq20z70 (SLUA379: *Data Flash Programming and Calibrating the bq20z70 and bq20z90 Family of Gas Gauges*) for more information on calibration.

Board Offset

Board Offset is the second offset register. Its primary purpose is to calibrate all that the *CC Offset* does not calibrate out. This includes board layout, sense resistor and copper trace and other offsets that are external to the bq20z70 IC. The simplified ground circuit design in the bq20z70 requires a separate board offset for each tested device. The bq20z70 board offset calibration is explained in the SLUA379 application note.

Normal Setting: This value needs to be modified for each device being tested unlike the bq20z80. See the latest calibration application note for the bq20z70 (SLUA379: *Data Flash Programming and Calibrating the bq20z70 and bq20z90 Family of Gas Gauges*) for more information on calibration.

Int Temp Offset

The bq20z70 has a temperature sensor built into the IC. The *Int Temp Offset* is used for calibrating out offset errors in the measurement of the reported ***Temperature*** if the internal temperature sensor is used. The gain of the internal temperature sensor is accurate enough that a calibration for Gain is not required.

Normal Setting:*Int Temp Offset* should never need to be modified by the user. It is modified by the internal temperature sensor calibration command in Calibration mode. *Int Temp Offset* should only be calibrated if the internal temperature sensor is used. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of Gas Gauges* application note SLUA379 for more information on calibration.

Ext1 Temp Offset

Ext1 Temp Offset is for calibrating the offset of the thermistor connected to the TS1 pin of the bq20z70 as reported by ***Temperature***. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting:*Ext1 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext1 Temp Offset* should only be calibrated if a thermistor is connected to the TS1 pin of the bq20z70. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of Gas Gauges* application note SLUA379 for more information on calibration.

Ext2 Temp Offset

Ext2 Temp Offset is for calibrating the offset of the thermistor connected to the TS2 pin of the bq20z70 as reported by ***Temperature***. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting: *Ext2 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext2 Temp Offset* should only be calibrated if the a thermistor is connected to the TS1 pin of the bq20z70. See the *Data Flash Programming/Calibrating the bq20z70 and bq20z90 Family of Gas Gauges* application note SLUA379 for more information on calibration.

Config

These are all setting for adjusting Calibration Mode applied voltage, current, and temperature as well as the times associated with these calibrations. The Times should not need to be modified with normal applications. The values in Data Flash for these registers are defaults for Calibration Mode. If no other values are assigned to the calibration commands associated with each of these registers when in Calibration Mode, then these default values are used. See the *Data Flash Programming/Calibrating the bq20z90 Gas Gauges* application note SLUA355A for more information on calibration.

CC Current

This register holds the default current that is applied during the calibration process while in Calibration mode. While in calibration mode, if the *CC Current* is not modified by calibration command, then this value is what is used to calibrate *CC Gain* and *CC Delta*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z70.

Normal Setting: This depends on the sense resistor used. Higher currents increase the voltage across the SR1 and SR2 pins which decreases noise and offset errors. It also increases the calibration accuracy because the granularity has less effect on the measurements. Good numbers for a 10 milliohm sense resistor are 2 to 3 amps.

Voltage Signal

This register holds the default voltage that is applied during the calibration process while in Calibration Mode. While in calibration mode, if the *Voltage Signal* is not modified by calibration command, then this value is what is used to calibrate *Reference Voltage* and *AFE Pack Gain*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z70. This value is a pack voltage, not a cell voltage.

Normal Setting: This depends on the number of cells, but it is good idea to use a voltage that is within the normal operating voltages of the cells used in the application times the number of cells.

Temperature Signal

This register holds the default Temperature that is applied during the calibration process while in Calibration Mode. If, while in calibration mode, the *Temperature Signal* is not modified by calibration command then this value is what is used to calibrate all the Temperature inputs that are used in this application. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z70.
Normal Setting: This value more than any of the others must be modified using the calibration commands in Calibration Mode instead of using this Data Flash location because temperature is continually changing.

CC Offset Time

CC Offset Time is the time that the calibration command for initiating a *CC Offset* calibration takes to do a *CC Offset* calibration. This is also used in Board Offset calibration in the bq20z70 EV software.

Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function rounds the *CC Offset Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Remember that this is only a temporary calibration to minimize offset effects on other CC calibrations. The Automatic Offset calibration that happens during normal Gas Gauging mode does a more accurate calibration. It is important to note that this is also used by the bq20z70 EV software to do Board Offset calibration. It is a good idea to increase this number to 20,000 to get a very accurate board offset measurement for production testing (see *Board Offset*) .

ADC Offset Time

ADC Offset Time is the time that the calibration command for initiating an ADC Offset calibration takes for an ADC Offset calibration. *ADC Offset* is not associated with a Data Flash location, but it is done every time Automatic *ADC Offset* is done in Gas Gauging mode and should be initiated at the same time as *ADC Offset* when in Calibration Mode.

Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the *ADC Offset Time* down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It reports a calibration error if a value less than 32 is used. Remember that this is only a temporary calibration. The Automatic Offset calibration that happens during normal Gas Gauging mode keeps this value accurate.

CC Gain Time

CC Gain Time is the time that the calibration command for initiating a CC Gain calibration takes for a *CC Gain Time* calibration. It uses the value in *CC Current* over *CC Gain Time* to do the calibration.
Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function will round the *CC Gain Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Depending on the current used, it is possible that 250 ms not enough time for a good calibration. It is recommended that 500 ms to 1000 ms be used for best results.

Voltage Time

Voltage Time is the time that the calibration commands for initiating a *Reference Voltage* or *AFE Pack Gain* calibration takes for a *Reference Voltage* or *AFE Pack Gain* calibration. These commands use the value in *Voltage Signal* over *Voltage Time* to do the calibration.
Normal Setting: The default is 1984 and the units are in milliseconds. Only use values in multiples of 1984ms. The calibration function will round the *Voltage Time* down to the next lower multiple of 1984ms if an exact multiple of 1984 is not used. It will report a calibration error if a value less than 1984 is used.

Temperature Time

Temperature Time is the time that the calibration commands for initiating any of the *3 temperature* calibrations takes for the respective calibrations. These commands uses the value in *Temperature Signal* over *Temperature Time* to do the calibration.
Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the *Temperature Time* down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It reports a calibration error if a value less than 32 is used.

Cal Mode Timeout

Cal Mode Timeout is the maximum amount of time allowed for all calibrations to complete before the bq20z70 reverts to Gas Gauge mode automatically. The timer for this function starts when the ***Call Mode*** command is initiated.
Normal Setting: The purpose of this function is ensure that the bq20z70 has the ability to get out of Calibration Mode on its own if it was accidentally put into Calibration Mode for any reason. The default for this register is 300 which is in units of seconds. This translates to 5 minutes. It is unlikely that this register will need to be modified.

Temp Model

None of these registers must not be changed for any reason. The only reason these values are listed is for the purpose of using a different thermistor; however, this is not recommended, and has not been tested with the bq20z70 at the time this was written.

Ext Coef 1, Ext Coef 2, Ext Coef 3, Ext Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Ext Min AD

This is the minimum ADC value allowed for the Temperature conversion formula.
Normal Setting: This value is 0 and should not be changed.

Ext Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.
Normal Setting: This value is 4012 and should not be changed.

Int Coef 1, Int Coef 2, Int Coef 3, Int Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Int Min AD

This is the minimum ADC value allowed for the Temperature conversion formula.
Normal Setting: This value is 0 and should not be changed.

Int Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.
Normal Setting: This value is 4012 and should not be changed.

Current

Filter

This constant defines the filter constant used in the ***Average Current*** formula. This is a very common question how this is calculated. The formula used to compute ***Average Current*** is :

New (***Average Current***) = A × *Old* (***Average Current***) + (1-A) × ***Current***

A = *Filter*/256. Default value is 239

The time constant = 1 sec/ln(1/a) (default 14.5 sec)
Normal Setting: It is unlikely that this value should ever need to be changed.

Deadband

The purpose of the *Deadband* is to create a filter window to the reported ***Current*** register where the current is reported as 0. Any negative current above this value or any positive current below this value is displayed as 0.
Normal Setting: This defaults to 3 mA. There are not many reasons to change this value. Here are a few.

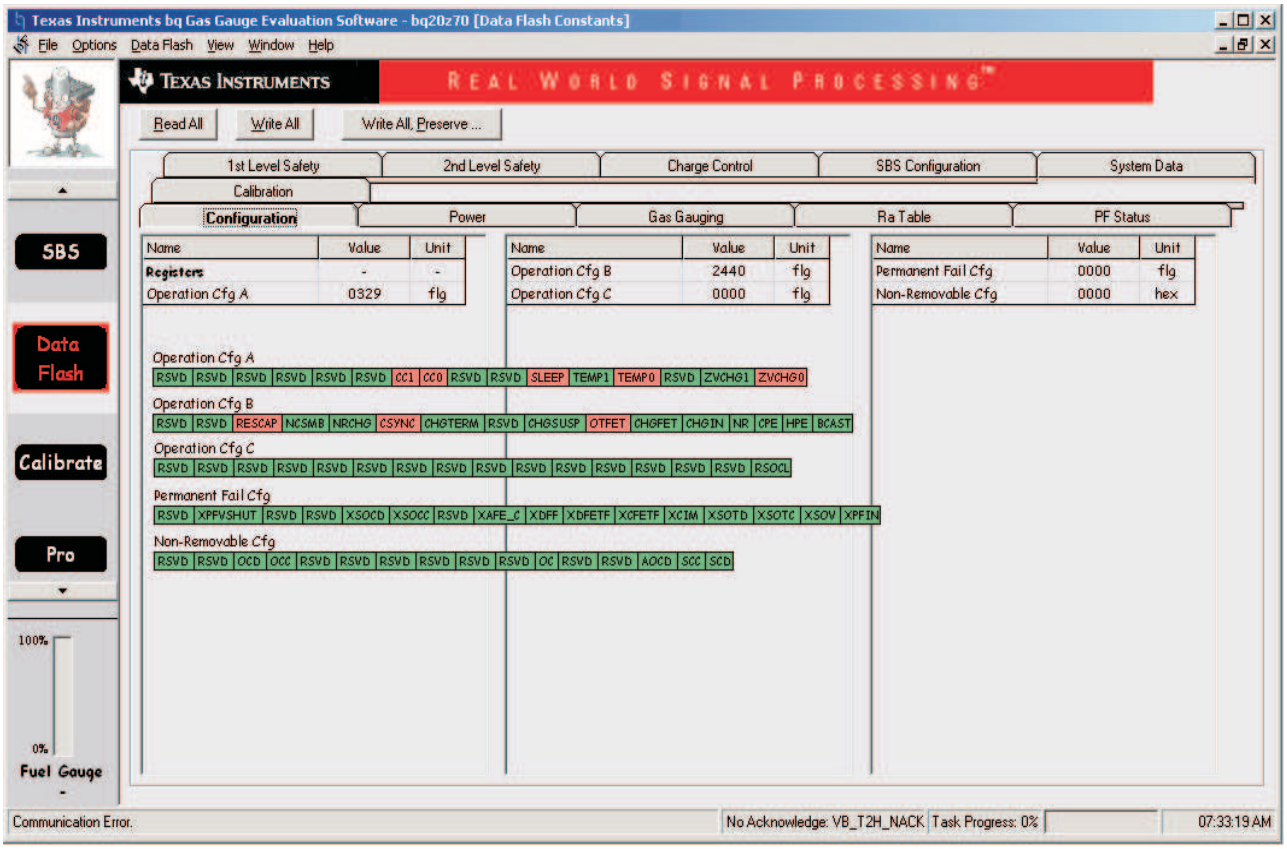
1. If the bq20z70 is not calibrated.
2. *Board Offset* has not been characterized.
3. If the PCB layout has issues that cause inconsistent board offsets from board to board.
4. An extra noisy environment in conjunction with number 3.

If this value must be modified be sure and verify the CC Deadband as well.

CC Deadband

This is also referred to as Digital Filter. This works much in the same way as the *Deadband* except it works for capacity counting on the ***Remaining Capacity*** register. Any absolute voltage between SR1 and SR2 below this value does not contribute to capacity measurement. The purpose of this is to minimize the possibility of unwanted noise from being counted towards capacity.
Normal Setting: The default for this register is 10 microvolts. This value is most likely too small for most applications. A better value would be 2 or 3 times this default. Unlike *Deadband* this value is not influenced by what value of sense resistor is used since this value is stored in microvolts and not milliamps.

3.9 Configuration



Registers

Operation Cfg A

This register is used to enable or disable various functions on the bq20z70. These bits are continued in *Operation Cfg B*.

—	—	—	—	—	—	CC1	CC0
—	—	SLEEP	TEMP1	TEMP0	—	ZVCHG1	ZVCHG0

- RESERVED [15-10]: These bits are reserved.
- CC1,0 [9,8]: These bits are used to tell the bq20z70 the number of LION battery cells in series the application has. This setting is critical for every aspect of the Data Flash configuration with regards to voltage based functions.
  - 1,1 = 4 series cell application
  - 1,0 = 3 series cell application
  - 0,1 = 2 series cell application
  - 0,0 = Reserved (Not Valid)

  Normal Setting: The default value for these bits are both set for a 4 series cell application. These bits are application and user dependant.
- RESERVED [7,6]:These bits are reserved
- SLEEP [5]: This bit enables or disables the ability to go to sleep when SMBus Clock and Data lines go low for *Bus Low Time* and ***Current*** is below *Sleep Current* (See *Sleep Current* and *Bus Low Time*)
  - 0: bq20z70 will not go to sleep with the above criteria
  - 1: bq20z70 will go to sleep when the sleep criteria is set

Normal Setting: This bit defaults to a 1 which should be used in most applications. There are very few reasons why this should be set to 0.

- Temp1,0 [4,3]: These bits are used to tell the bq20z70 the temperature sensor configuration. The bq20z70 can use up to 2 external sensors and there is also an internal sensor available if needed. All of these sensors are able to use various configurations to report temperature in the ***Temperature*** register.
  - 1,1 = The Average of TS1 and TS2 external inputs are used to generate ***Temperature***
  - 1,0 = Greater Value of TS1 and TS2 external inputs are used to generate ***Temperature***
  - 0,1 = Only Temperature sensor TS1 is used to generate ***Temperature***
  - 0,0 = 0,0 = Only internal temperature sensor is used to generate ***Temperature***.

  Normal Setting: The default setting for these bits is [Temp1] cleared and [Temp0] set. This requires one external temperature sensor on TS1. The bq20z70 default configuration is for a Semitec 103AT thermistor as briefly described in the ***Temp Model*** subclass (See ***Temp Model***). The internal temperature sensor is slightly less accurate than using a Semitc 103AT and is not recommended. It also is not as accurate because it cannot be put as close to the battery cells in the application as can be done with an external thermistor.
- RESERVED [2]: This bit is reserved
- ZVCHG1,0 [1,0]: These bits are also known as Pre-Charge 1,0. These bits are used to tell the bq20z70 how the Pre-Charge circuit is configured in the application. It tells the bq20z70 what pin on the bq29330 to use for Pre-Charge functions when required.
  - 1,1 = No action is taken in Pre-Charge functions with this setting.
  - 1,0 = OD pin is used for Pre-Charge functions.
  - 0,1 = Charge FET is used for Pre-Charge functions.
  - 0,0 = ZVCHG FET is being used for Pre-Charge functions.

  Normal Setting: If using a separate Pre-Charge FET it is recommended not to use the OD pin for this function because it does not have good “zero volt charging” capabilities when a battery is completely dead. Therefore, the ZVCHG pin should be used because it has excellent clamping abilities. The default is for using the Charge FET pin on the bq29330.

Operation Cfg B

This register is used to enable or disable various functions on the bq20z70. This is a continuation of *Operation Cfg A*.

—	—	RESCAP	NCSMB	NRCHG	CSYNC	CHGTERM	—
CHGSUP	OTFET	CHGFET	CHGIN	NR	CPE	HPE	BCAST

- RESCAP [13]: The bq20z70 reports ***Remaining Capacity*** and ***Full Charge Capacity*** that is falsely lower than the actual capacity of the battery as defined by the *Reserve Cap-mAh* in mAh mode or *Reserve Cap-mW* in mWh mode (configured by [CAPM] in ***Battery Mode***). RESCAP sets a load compensation for this function.
  - 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
  - 1: If set to a 1, then a more normal rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See **IT Cfg** class)

  Normal Setting: This bit defaults to a 1. For most applications, this along with *Load Select* should be left at the default values.
- NCSMB [12]: This bit is used to enable a special mode for the SMBus engine in the bq20z70 where it allows for unlimited timeouts for SMBus communications more like I^2C. This mode was made for customers that were using older legacy parts that had longer timeouts and were not SMBus compliant.
  - 0: Timeout extension is disabled.
  - 1: Unlimited Timeout extension enabled.

  Normal Setting: The default for this register is 0. It is recommended that this always be set to 0. There have been many complications with customers using this function in the past. When set to a 1, it is important to note that if clocking in data with a SMBus read command and the communication gets interrupted with data low then data can be stuck low until more clocks are sent to finish the communication.

- NRCHG [11]: This bit is used to configure whether or not the bq20z70 turns off the Charge FET when it goes to Sleep if [NR] bit is set in *Operation Cfg B*. If [NR] cleared then this bit is not used.
  - 0: Charge FET turns off in sleep mode as long as the bq20z70 is setup with [NR] set.
  - 1: Charge FET remains on in sleep mode with the [NR} bit set.

  Normal Setting: This bit defaults to a 0 which should be used for most applications with [NR] set. This could be a problem for some applications that expect the battery to start charging immediately when charge is applied when asleep.
- CSYNC [10]: This bit is used in the Primary Charge Termination Algorithm (See *Maintenance Current*). When this bit is set, then with a Primary Charge Termination the bq20z70 writes the ***Remaining Capacity*** to ***Full Charge Capacity***
  - 0: ***Remaining Capacity*** is not written up to ***Full Charge Capacity*** on Primary Charge Termination.
  - 1: ***Remaining Capacity*** is written up to ***Full Charge Capacity*** on Primary Charge Termination.

  Normal Setting: The default setting for this bit is 1. This should be used for most applications to ensure that the Remaining Capacity starts from ***Full Charge Capacity*** when the charger terminates charging. This is a synchronization function to ensure the bq20z70 discharges from full when it has been determined that the battery is full.
- CHGTERM [9]: This bit enables the ability for the bq20z70 to turn off [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination is detected and then ***Current*** falls below the *Chg Current Threshold* for 2 consecutive periods of *Taper Current Window*.
  - 0: bq20z70 does not clear [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination.
  - 1: bq20z70 does clear [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination.

  Normal Setting: This bit defaults to 0. This should be acceptable for most applications.
- CHGSUSP [7]: This bit enables the ability to turn off the Charge FET and/or Pre-Charge FET in charge suspend mode (See **Charge Control** Class).
  - 0 = The Charge FET is unaffected by any type of charge suspension.
  - 1 = The Charge FET and/or Pre-Charge FET are opened with any charge suspension.

  Normal Setting: The default setting for this bit is 0. It is common for this to be set to 1 to give the bq20z70 the control for additional protection.
- OTFET [6]: This bit is used to configure how the bq20z70 controls the current FETs (Charge or Discharge) during *Over Temp Chg* or *Over Temp Dsg* faults. (See *Over Temp Chg* and *Over Temp Dsg*)
  - 0: FET control is unaffected by any *Over Temp Chg* or *Over Temp Dsg* faults.
  - 1: During a *Over Temp Chg* fault the Charge FET is opened. During a *Over Temp Dsg* fault the Discharge FET is opened.

  Normal Setting: This bit defaults to a 1 which should be used in production for most applications. Over temperature conditions can be dangerous and every level of protection possible should be used.
- CHGFET [5]: This bit is used to configure how the bq20z70 controls the Charge FETs when [TCA] gets set in ***Battery Status***. (See *TCA Set* % for an explanation for when [TCA] gets set).
  - 0: Charge FET is unaffected anytime [TCA] gets set.
  - 1: Charge FET is turned off anytime [TCA] gets set.

  Normal Setting: This bit defaults to a 0 which should be used in production for most applications. Setting it to a 1 turns the Charge FET off is only if *Maintenance Current* is set to 0.
- CHGIN [4]: This bit is used to configure how the bq20z70 controls the Charge FETs when in charge inhibit mode. (See *Chg Inhibit Temp Low* and *Chg Inhibit Temp High*).
  - 0: Charge FET is unaffected when in charge inhibit mode.
  - 1: Charge FET is turned off when in charge inhibit mode.

  Normal Setting: This bit defaults to a 0 which should be acceptable for most applications. It is important to note that this is different than charge suspend mode because this inhibits the charge cycle from occurring. This function acts while discharging.
- NR [3]: Use this bit to configure the bq20z70 for either a removable or a nonremovable battery pack. A removable pack uses the System Present pin (PRES) and a nonremovable pack does not. This affects many functions in the bq20z70. Primarily it affects the way it handles recovery methods of most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With

[NR] set, the *NR Config* register is used to enable many nonremovable pack fault recovery methods for use with a removable pack. (See *NR Config* and **Current** subclass in **1st Level Safety** class)

- 0: Configures battery for removable mode. Transition on System Present pin (PRES) triggers certain recovery functions. *NR Config* can be used to enable nonremovable functions for this mode as well
- 1: Configures battery for nonremovable mode.

Normal Setting: Default for this bit is application specific. Set to 0 for batteries that are removed, and use the PRES pin. Set to 1 for packs that do not use the PRES pin.

- CPE [2]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z70 broadcasts to the SMBus Device Address 0x12 (SMBus charger device address) (See SBS and SMBus specification that can be downloaded from the web).
  - 0: No PEC byte is sent to SMBus Device Address 0x12.
  - 1: Every broadcast from the bq20z70 to SMBus Device Address 0x12 includes a PEC byte as the last byte sent.

  Normal Setting: If a smart charger (SMBus Device Address 0x12) is used that is PEC capable, then this should be set to a 1. It is always recommended to use PEC when possible.
- HPE [1]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z70 broadcasts to the SMBus Device Address 0x14 (SMBus Host device address)
  - 0: No PEC byte is set to SMBus Device Address 0x14. (See SBS and SMBus specification that can be downloaded from the web)
  - 1: Every broadcast from the bq20z70 to SMBus Device Address 0x14 includes a PEC byte as the last byte sent.

  Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.
- BCAST [0]: This bit enables or disables Master Mode Message broadcasting periodically to a smart charger or host. The bq20z70 broadcasts are completely disabled (See SBS and SMBus specification that can be downloaded from the web)
  - 0: The bq20z70 never masters the SMBus for any reason.
  - 1: The bq20z70 is enabled to Master the bus periodically to inform a host or charger of critical information

  Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.

Operation Cfg C

This register is used to enable or disable various functions on the bq20z70. This is a continuation of Operation Cfg B.

—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	RSOCL

- RSOCL[0]: This bit is used to modify the functionality of RSOC at 100%
  - 1 = When set to 1, then ***RSOC*** is only written to 100% if there is a primary charge termination (see *Taper Current* for more information on primary charge termination).
  - 0 = When set to 0, then ***RSOC*** at 100% functions like every other percentage for RSOC. When it reaches 99%, then any fraction above 99% in the ***RSOC*** computation will force ***RSOC*** to be written to 100%

  Normal Setting: This function is very application specific. Some customers have requested that they do not want ***RSOC*** to be 100% under any circumstances unless the bq20z70 detects a full condition. If this is a requirement, then consider setting this to a 1.

Permanent Fail Cfg

This enables or disables the various permanent failure protection functions ability to activate the SAFE output or not when the function is triggered.

—	SPFVSHUT	—	—	XSOCD	XSOCC	—	XAFE_C
XDFF	XDFETF	XCFETF	XCIM	XSOTD	XSOTC	XSOV	XPFIN

- RESERVED [15–12]: These bits are reserved. Even XPFVSHUT serves no purpose. These bits should always be set to 0.
- XSOPT [11]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an Safety Over Current in the discharge direction condition. (See *SOC Chg*)
  - 0: The SAFE pin is not activated for a Safety Over Current in the discharge direction Condition
  - 1: The SAFE pin is driven high on the bq20z70 for a Safety Over Current in the discharge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOPT] be set for production packs to protect against hazardous failures.
- XSOCC [10]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Current in the charge direction condition. (See *SOC Dsg*).
  - 0: The SAFE pins are not activated for a Safety Over Current in the charge direction Condition
  - 1: The SAFE pin is driven high on the bq20z70 for a Safety Over Current in the charge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOCC] be set for production packs to protect against hazardous failures.
- RESERVED [9]: This bit is reserved.
- XAFE_C [8]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an AFE communication verification failure. (See *AFE Fail Limit*)
  - 0: The SAFE pin are not activated for an AFE communication verification failure.
  - 1: The SAFE pin is driven high on the bq20z70 for an AFE communication verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XAFE_C] be set for production packs to protect against hazardous failures.
- XDFF [7]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Data Flash verification failure. (See *PF Flags 1*)
  - 0: The SAFE pin is not activated and the *Fuse Flag* is not written to 0x3672 for a Data Flash verification failure.
  - 1: The SAFE pin is driven high on the bq20z70 for a Data Flash verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFF] be set for production packs to protect against hazardous failures.
- XDFETF [6]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Discharge FET Failure condition. (See *FET Fail Limit*)
  - 0: The SAFE pin is not activated for a Discharge FET Failure Condition.
  - 1: The SAFE pin is driven high on the bq20z70 for a Discharge FET Failure Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFETF] be set for production packs to protect against hazardous failures.

- XCFETF [5]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Charge FET Failure condition . (See *FET Fail Limit*)
  - 0: The SAFE pin is not activated for a Charge FET Failure Condition.
  - 1: The SAFE pin is driven high on the bq20z70 for a Charge FET Failure Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCFETF] be set for production packs to protect against hazardous failures.
- XCIM [4]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a extreme Cell Imbalance condition. (See *Cell Imbalance Fail Voltage*)
  - 0: The SAFE pin is not activated for a extreme Cell Imbalance Condition.
  - 1: The SAFE pin is driven high on the bq20z70 for a extreme Cell Imbalance Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCIM] be set for production packs to protect against hazardous failures.
- XSOTD [3]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Temperature in the discharge direction condition. (See *SOT Chg*)
  - 0: The SAFE pin is not activated for a Safety Over Temperature in the discharge direction Condition.
  - 1: The SAFE pin is driven high on the bq20z70 for a Safety Over Temperature in the discharge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOTD] be set for production packs to protect against hazardous failures.
- XSOTC [2]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Temperature in the charge direction condition. (See *SOT Chg*)
  - 0: The SAFE pin are not activated for a Safety Over Temperature in the charge direction Condition.
  - 1: The SAFE pin is driven high on the bq20z70 for a Safety Over Temperature in the charge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOTC] be set for production packs to protect against hazardous failures.
- XSOV [1]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Voltage condition. (See *SOV Threshold*).
  - 0: The SAFE pin are not activated for a Safety Over Voltage Condition.
  - 1: The SAFE pin is driven high for a Safety Over Voltage Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOV] be set for production packs to protect against hazardous failures.
- XPFIN [0]: This bit enables the ability for the bq20z70 to force the SAFE pin high which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a PFIN input low condition. (See *PFIN Detect Time*)
  - 0: The SAFE pin is not activated for a PFIN input low Condition.
  - 1: The SAFE pin is driven high on the bq20z70 for a PFIN input low Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing

of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XPFIN] be set for production packs to protect against hazardous failures.

Non-Removable Cfg

This register affects the way the bq20z70 handles recovery methods for most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register can be used to enable many nonremovable pack fault recovery methods for use with a removable pack. NR Config can be used to enable nonremovable fault recovery functions for a battery pack that is configured as removable.

—	—	OCD	OCC	—	—	—	—
—	—	OC	—	—	AOCD	SCC	SCD

- RESERVED [15, 14]: These bits are reserved.
- OCD [13]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z70. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the discharge direction fault (See (OC*1st Tier) Dsg*).
  - 0: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is not enabled.
  - 1: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- OCC [12]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z70. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the charge direction fault (See *OC (1st Tier) Chg*).
  - 0: The nonremovable recovery option associated with *OC (1st Tier) Chg* is not enabled
  - 1: The nonremovable recovery option associated with *OC (1st Tier) Chg* is enabled.

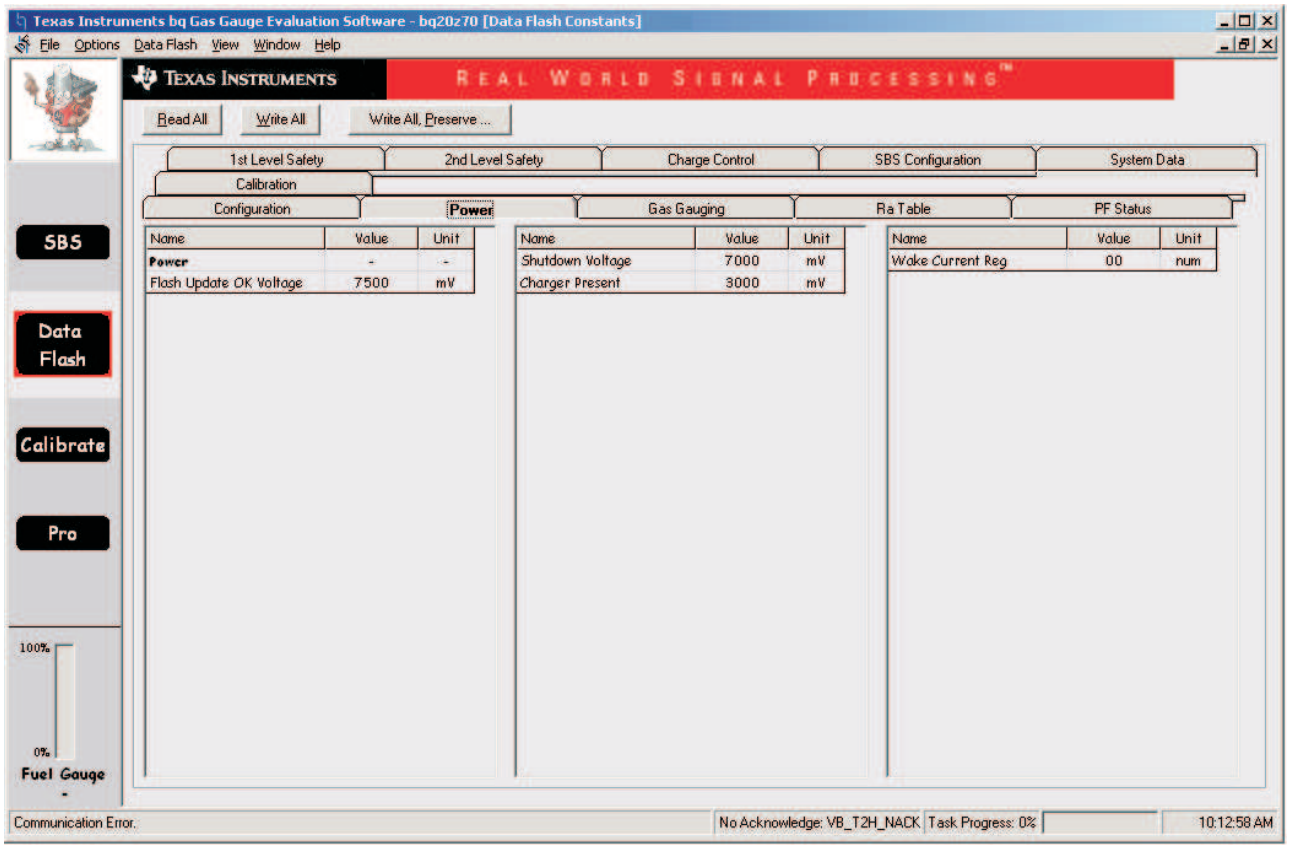
  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- RESERVED [11-3]: These bits are reserved.
- AOCD [2]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z70. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE Over Current in the discharge direction fault (*AFE OC Dsg*).
  - 0: The nonremovable recovery option associated with *AFE OC Dsg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE OC Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- SCC [1]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z70. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the charge direction fault (*AFE SC Chg*).
  - 0: The nonremovable recovery option associated with *AFE SC Chg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE SC Chg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- SCD [0]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z70. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the discharge direction fault (*AFE SC Dsg*).
  - 0: The nonremovable recovery option associated with *AFE SC Dsg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE SC Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

3.10 Power



Power

Flash Update OK Voltage

This register controls one of several data flash protection features. It is critical that data flash is not updated when the battery voltage is low. Data Flash programming takes much more current than normal operation of the bq20z70/bq29330 chipset and with a depleted battery this current can cause the battery voltage to crater (drop dramatically) forcing the bq20z70 into reset before completing a data flash write. The effects of an incomplete Data Flash write can corrupt the memory resulting in unpredictable and extremely undesirable results. The voltage setting in *Flash Update OK Voltage* is used to prevent any writes to the data flash below this value. If a charger is detected then this register is ignored.

Normal Setting: The default for this register is 7500 millivolts. For 2-cell applications, this can cause production issues with writing to the data flash because at nominal cell voltages, 2-cell applications can easily be below 7500 millivolts. The way to solve this problem is to connect a charger voltage to the battery which overrides this register while connected. Ensure that this register is set to a voltage where the battery has plenty of capacity to support data flash writes but below any normal battery operation conditions.

Shutdown Voltage

The bq20z70 goes into shutdown mode when ***Voltage*** falls below the *Shutdown Voltage* for at least Shutdown Time seconds. Also ***Current*** must be less than 0 and the ***Pack Voltage*** must be less than *Charger Present* for the entire time. So when the following conditions are met:

1. ***Voltage*** is below *Shutdown Voltage*
2. ***Current*** is less than 0
3. ***Pack Voltage*** less than *Charger Present*

Then a 10 second timer is initiated. If the above conditions remain until the timer expires, then the bq20z70 goes into shutdown mode. Every time the bq20z70 wakes up from shutdown mode, the 10 second timer is reset. It is not possible for the bq20z70 to go back into shutdown mode for 10 seconds after waking. When in shutdown mode, VCC is completely removed from the bq20z70 by the bq29330. (See *Shutdown Voltage*)
Normal Setting: This voltage should be far below any normal operating voltage but above any threshold that can cause damage to the cells. This threshold is met after the Charge and Discharge FETs are turned off from an under voltage fault condition.

Charger Present

A charger is deemed present when ***Pack Voltage*** is at or above this level.
Normal Setting: It is important to note that a charger detection because this function prevents shutdown by either a ***Manufacture Access*** command or *Shutdown Voltage*. Some applications with external voltage sources can confuse the shutdown detection which prevents the bq20z70 shutdown mode from functioning properly. The bq29330 wakes up with a voltage above the “Start-up” voltage which is a wake up feature built into the bq29330 (see the bq29330 data sheet: SLUS673). If there is an external voltage source that has a voltage above the “Start-up” voltage threshold, but below the *Charger Present* threshold, then the bq20z70 oscillates between awake and shutdown. This causes abnormal operational side effects. Therefore, it is recommended that *Charger Present* be set to 3000-4000 mV if there are any external voltage sources. Otherwise, this voltage can be set to between (3000–4000 mV per cell) × (number of cells).

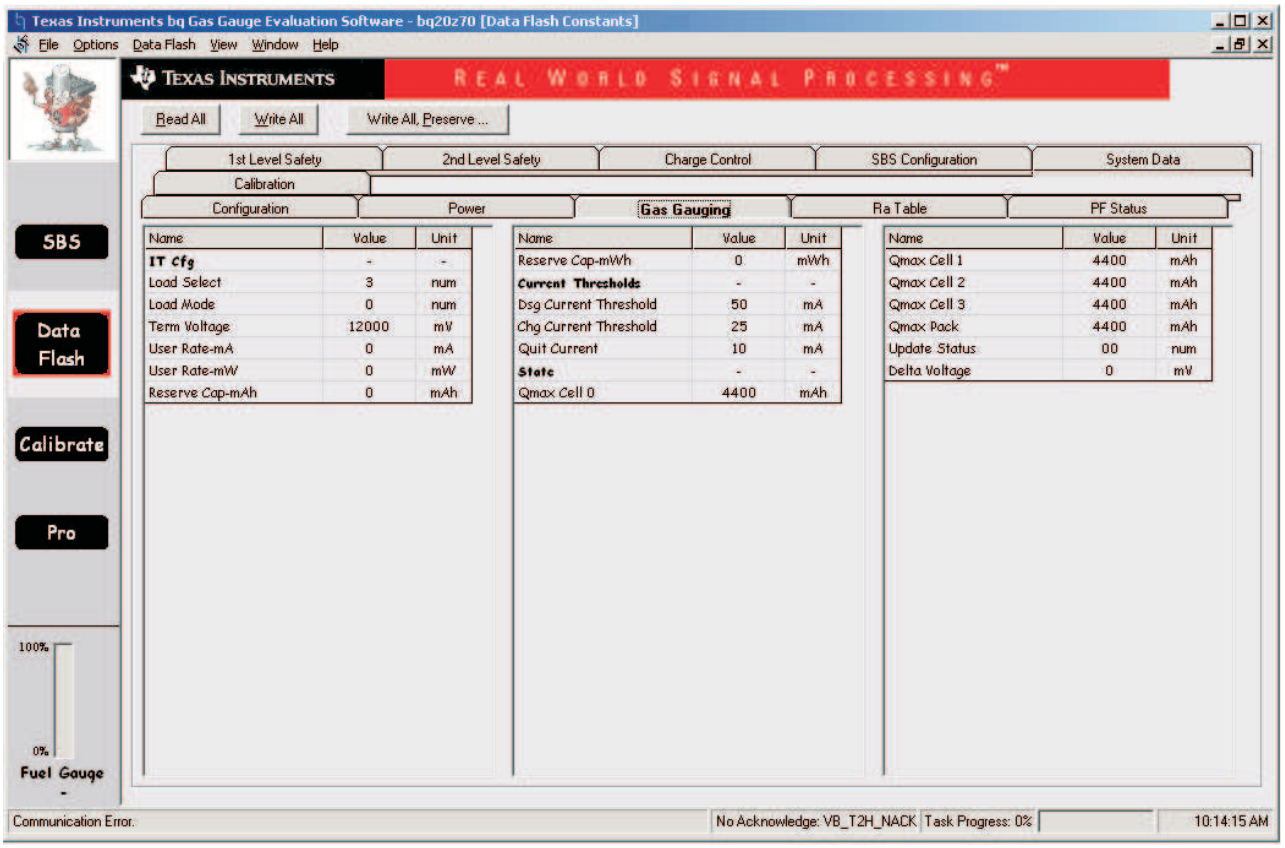
Wake Current Reg

This is one option for waking the bq20z70 from sleep. When the ***Current*** becomes more than what is set in *Wake Current Reg*, then the bq20z70 wakes from sleep.
Normal Setting: The default for this register is 0x00. This means that the function is disabled. The function is based on current; therefore, a sense resistor value must be selected as part of the option in (RSNS1, RSNS0).

—	—	—	—	—	—	—	—
—	—	—	—	—	IWAKE	RSNS1	RSNS0

IWAKE	RSNS1	RSNS0	Current	Sense Resistor Value
0	0	0	Disabled	Disabled
0	0	1	0.5 A	2.5 mΩ
0	1	0	0.5 A	5 mΩ
0	1	1	0.5 A	10 mΩ
1	0	0	Disabled	Disabled
1	0	1	1 A	2.5 mΩ
1	1	0	1 A	5 mΩ
1	1	1	1 A	10 mΩ

3.11 Gas Gauging



IT Config

Load Select

Load Select defines the type of power or current model to be used for *Remaining Capacity* computation in the Impedance Track™ algorithm. If *Load Mode* = Constant Current, then the following options are available:

0 = Average discharge current from previous cycle: There is an internal register that records the average discharge current through each entire discharge cycle. The previous average is stored in this register.

1 = Present average discharge current: This is the average discharge current from the beginning of this discharge cycle till present time.

2 = *Current*: based off of *Current*

3 = *Average Current* (default): based off the *Average Current*

4 = *Design Capacity* / 5: C Rate based off of *Design Capacity* /5 or a C / 5 rate in mA.

5 = *AtRate* (mA): Use whatever current is in *AtRate*

6 = *User_Rate-mA*: Use the value in *User_Rate-mA*. This gives a completely user configurable method.

If *Load Mode* = Constant Power then the following options are available:

0 = Average discharge power from previous cycle: There is an internal register that records the average discharge power through each entire discharge cycle. The previous average is stored in this register.

1 = Present average discharge power: This is the average discharge power from the beginning of this discharge cycle till present time.

2 = *Current* × *Voltage*: based off of *Current* and *Voltage*

3 = *Average Current*×*Voltage* (default): based off the *Average Current* and *Voltage*

4 = *Design Energy* / 5: C Rate based off of *Design Energy* /5 or a C / 5 rate in mA

5 = *AtRate* (10 mW): Use whatever value is in *AtRate*.

6 = *User_Rate-10mW*: Use the value in *User_Rate-mW*. This gives a completely user configurable method.

Normal Setting: The default for this register is 3 which should be acceptable for most applications. This is application dependent.

Load Mode

Load Mode is used to select either the constant current or constant power model for the Impedance Track™ algorithm as used in *Load Select*. (See *Load Select*)

- 0: Constant Current Model
- 1: Constant Power Model

Normal Setting: This is normally set to Current Model but It is application specific. If the application load profile more closely matches a constant power model, then set to 1.

Term Voltage

Term Voltage is used in the Impedance Track™ algorithm to help compute ***Remaining Capacity***. This is the absolute minimum voltage for end of discharge.
Normal Setting: This register is application dependent. It should be set based on battery cell specifications to prevent damage to the cells or the absolute minimum system input voltage taking into account impedance drop from the PCB traces, FETs, and wires.

User Rate-mAh

User Rate-mAh is only used if *Load Select* is set to 6 and *Load Mode* = 0. If these criteria are met then the current stored in this register is used for the ***Remaining Capacity*** computation in the Impedance Track™ algorithm. This is the only function that uses this register.
Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined current at the end of discharge. With this type of discharge, it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment *Term Voltage* is reached.

User Rate-10mWh

User Rate-10mWh is only used if *Load Select* is set to 6 and *Load Mode* = 1. If these criteria are met, then the power stored in this register is used for the ***Remaining Capacity*** computation in the Impedance Track™ algorithm. This is the only function that uses this register.
Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined power at the end of discharge. With this application. it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment *Term Voltage* is reached.

Reserve Cap-mAh

Reserve Cap-mAh determines how much actual remaining capacity exists after reaching SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 0. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- [RESCAP]=0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity

- [RESCAP]=1: If set to a 1, then a higher rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mA mode (configured by [CAPM] in ***Battery Mode***).
Normal Setting: This register defaults to 0 which disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarmlike remaining* or *Remaining Capacity Alarm*.

Reserve Cap-10mWh

Reserve Cap-10mWh determines how much actual remaining capacity exists after reaching SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 1. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
- 1: If set to a 1, then a more normal rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mW mode (configured by [CAPM] in ***Battery Mode***).
Normal Setting: This register defaults to 0 which basically disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarm* or *Remaining Capacity Alarm*.

Current Thresholds

Dsg Current Threshold

This register is used as a threshold by many functions in the bq20z70 to determine if actual discharge current is flowing into and out of the part. This is independent from [DSG] in ***Battery Status*** which indicates whether the bq20z70 is in discharge mode or charge mode.
Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. If the bq20z70 is charging, then [DSG] is 0 and any other time (***Current*** less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z70 require more definitive information about whether current is flowing in either the charge or discharge direction. *Dsg Current Threshold* is used for this purpose. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Chg Current Threshold

This register is used as a threshold by many functions in the bq20z70 to determine if actual charge current is flowing into and out of the part. This is independent from [DSG] in ***Battery Status*** which indicates whether the bq20z70 is in discharge mode.
Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. Basically, if the bq20z70 is charging then [DSG] is 0 and any other time (***Current*** less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z70 require more definitive information about whether current is flowing in either the charge or discharge direction. This is what *Dsg Current Threshold* is used for. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Quit Current

The *Quit Current* is used as part of the Impedance Track™ algorithm to determine when the bq20z70 goes into relaxation mode from a current flowing mode in either the charge direction or the discharge direction. Either of the following criteria must be met to enter relaxation mode:

1. ***Current*** is **less than** (–)*Quit Current* and then goes within (±)*Quit Current* for 1 second.
2. ***Current*** is **greater than***Quit Current* and then goes within (±)*Quit Current* for 60 seconds.

After about 30 minutes in relaxation mode, the bq20z70 attempts to take accurate OCV and Qmax updates which are used in the Impedance Track™ algorithm.
Normal Setting: It is critical that the battery voltage be relaxed during OCV readings to get the most accurate results. This current must not be higher than C/20 when attempting to go into relaxation mode; however, it should not be so low as to prevent going into relaxation mode due to noise. This should always be less than *Chg Current Threshold* or *Dsg Current Threshold*.

State

Qmax Cell 0

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z70 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 1

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z70 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 2

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z70 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 3

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z70 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Pack

This is the maximum capacity of the entire battery pack. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated to the lowest chemical capacity of all the cells (*Qmax Cell 0 – Qmax Cell 3*) by the bq20z70 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity. It is updated with the capacity of the lowest cell during use. This is because the capacity of the entire battery is only as much as the capacity of the lowest cell. When that cell is empty, it does not matter if any other cells have capacity.

Update Status

There are 2 bits in this register that are important.

- Bit 1 (0x02) indicates that the bq20z70 has learned new Qmax parameters and is accurate.
- Bit 2 (0x04) indicates whether Impedance Track™ algorithm is enabled.

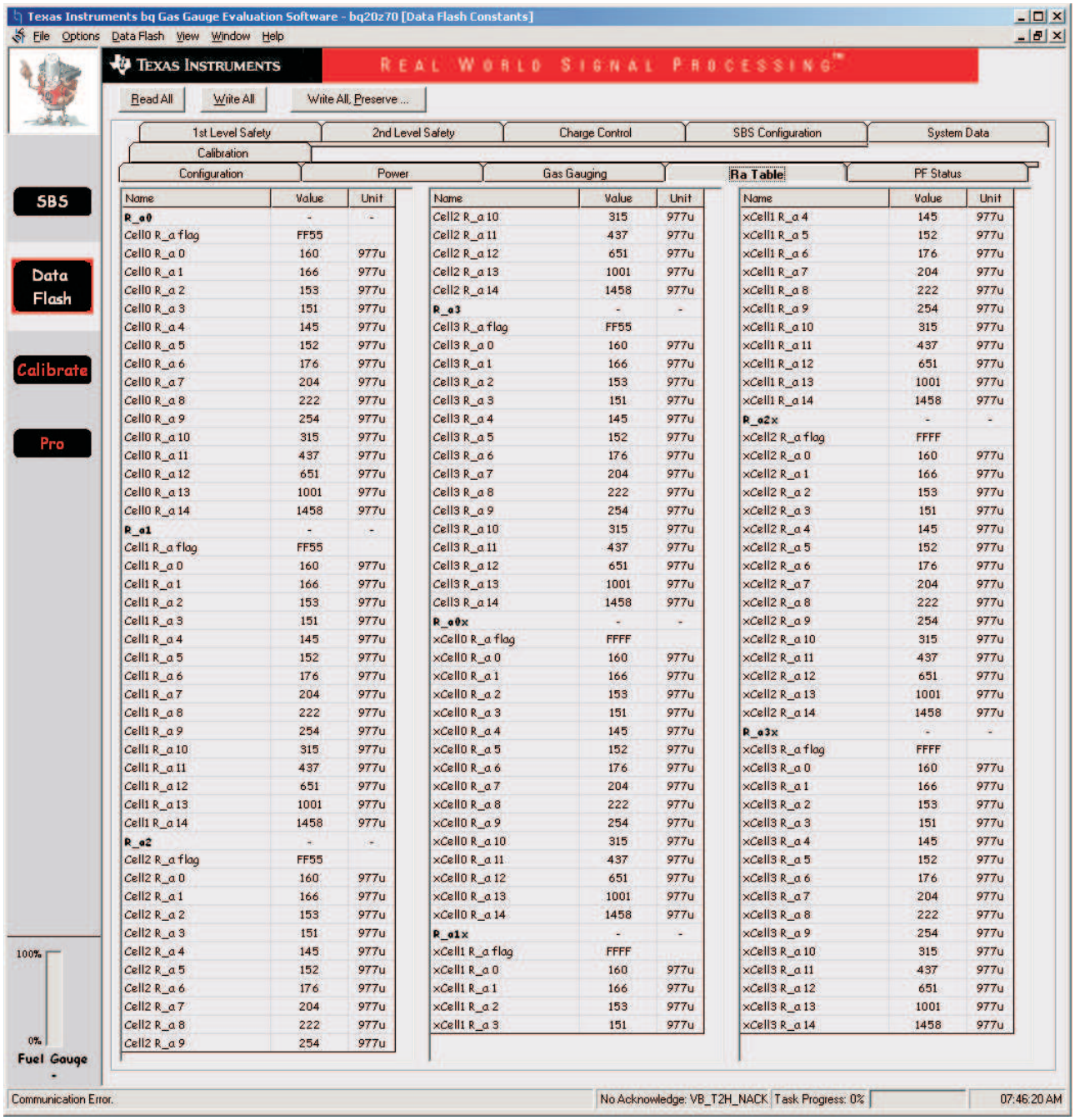
The remaining bits are reserved.
Normal Setting: These bits are user configurable; however, bit 1 is also a status flag that can be set by the bq20z70. These bits should never be modified except when creating a golden image file as explained in the application note *Preparing Optimized Default Flash Constants for specific Battery Types* (see SLUA334.pdf). Bit 1 is updated as needed by the bq20z70 and Bit 2 is set with ***Manufacturers Access*** command 0x0021.

Delta Voltage

The exact computation of this register is very complex so this description, while not exact, gives the general formula. Delta Voltage is derived as a function average Voltage versus immediate ***Voltage***. The average ***Voltage*** is a localized average over the most recent few seconds. The *Delta Voltage* is the maximum (average ***Voltage***–***Voltage***) at any given time. This register is only updated whenever the algorithm computes a value greater than the previous. Every SOC gridpoint (see *Cell0 R_a0*) causes a sort of reset of this computation. To prevent a 0 value in this register and to give more meaning, the reset algorithm uses a percentage of the previous SOC gridpoint *Delta Voltage* to compute a reset value and then starts the process of computing maximum *Delta Voltage* values again.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z70 when required.

3.12 Ra Table

This data is automatically updated during device operation. No user changes should be made except for reading the values from another pre-learned pack for creating “Golden Image Files”. See the application note *Preparation of optimized default flash constants for specific type of battery* (SLUA334). Profiles have format CellN R_a M where N is the cell serial number (from ground up), and M is the number indicating state of charge to which the value corresponds.



Name	Value	Unit
R_a0	-	-
Cell0 R_a flag	FF55	
Cell0 R_a 0	160	977u
Cell0 R_a 1	166	977u
Cell0 R_a 2	153	977u
Cell0 R_a 3	151	977u
Cell0 R_a 4	145	977u
Cell0 R_a 5	152	977u
Cell0 R_a 6	176	977u
Cell0 R_a 7	204	977u
Cell0 R_a 8	222	977u
Cell0 R_a 9	254	977u
Cell0 R_a 10	315	977u
Cell0 R_a 11	437	977u
Cell0 R_a 12	651	977u
Cell0 R_a 13	1001	977u
Cell0 R_a 14	1458	977u
R_a1	-	-
Cell1 R_a flag	FF55	
Cell1 R_a 0	160	977u
Cell1 R_a 1	166	977u
Cell1 R_a 2	153	977u
Cell1 R_a 3	151	977u
Cell1 R_a 4	145	977u
Cell1 R_a 5	152	977u
Cell1 R_a 6	176	977u
Cell1 R_a 7	204	977u
Cell1 R_a 8	222	977u
Cell1 R_a 9	254	977u
Cell1 R_a 10	315	977u
Cell1 R_a 11	437	977u
Cell1 R_a 12	651	977u
Cell1 R_a 13	1001	977u
Cell1 R_a 14	1458	977u
R_a2	-	-
Cell2 R_a flag	FF55	
Cell2 R_a 0	160	977u
Cell2 R_a 1	166	977u
Cell2 R_a 2	153	977u
Cell2 R_a 3	151	977u
Cell2 R_a 4	145	977u
Cell2 R_a 5	152	977u
Cell2 R_a 6	176	977u
Cell2 R_a 7	204	977u
Cell2 R_a 8	222	977u
Cell2 R_a 9	254	977u

Name	Value	Unit
Cell2 R_a 10	315	977u
Cell2 R_a 11	437	977u
Cell2 R_a 12	651	977u
Cell2 R_a 13	1001	977u
Cell2 R_a 14	1458	977u
R_a3	-	-
Cell3 R_a flag	FF55	
Cell3 R_a 0	160	977u
Cell3 R_a 1	166	977u
Cell3 R_a 2	153	977u
Cell3 R_a 3	151	977u
Cell3 R_a 4	145	977u
Cell3 R_a 5	152	977u
Cell3 R_a 6	176	977u
Cell3 R_a 7	204	977u
Cell3 R_a 8	222	977u
Cell3 R_a 9	254	977u
Cell3 R_a 10	315	977u
Cell3 R_a 11	437	977u
Cell3 R_a 12	651	977u
Cell3 R_a 13	1001	977u
Cell3 R_a 14	1458	977u
R_a0x	-	-
xCell0 R_a flag	FFFF	
xCell0 R_a 0	160	977u
xCell0 R_a 1	166	977u
xCell0 R_a 2	153	977u
xCell0 R_a 3	151	977u
xCell0 R_a 4	145	977u
xCell0 R_a 5	152	977u
xCell0 R_a 6	176	977u
xCell0 R_a 7	204	977u
xCell0 R_a 8	222	977u
xCell0 R_a 9	254	977u
xCell0 R_a 10	315	977u
xCell0 R_a 11	437	977u
xCell0 R_a 12	651	977u
xCell0 R_a 13	1001	977u
xCell0 R_a 14	1458	977u
R_a1x	-	-
xCell1 R_a flag	FFFF	
xCell1 R_a 0	160	977u
xCell1 R_a 1	166	977u
xCell1 R_a 2	153	977u
xCell1 R_a 3	151	977u

Name	Value	Unit
xCell1 R_a 4	145	977u
xCell1 R_a 5	152	977u
xCell1 R_a 6	176	977u
xCell1 R_a 7	204	977u
xCell1 R_a 8	222	977u
xCell1 R_a 9	254	977u
xCell1 R_a 10	315	977u
xCell1 R_a 11	437	977u
xCell1 R_a 12	651	977u
xCell1 R_a 13	1001	977u
xCell1 R_a 14	1458	977u
R_a2x	-	-
xCell2 R_a flag	FFFF	
xCell2 R_a 0	160	977u
xCell2 R_a 1	166	977u
xCell2 R_a 2	153	977u
xCell2 R_a 3	151	977u
xCell2 R_a 4	145	977u
xCell2 R_a 5	152	977u
xCell2 R_a 6	176	977u
xCell2 R_a 7	204	977u
xCell2 R_a 8	222	977u
xCell2 R_a 9	254	977u
xCell2 R_a 10	315	977u
xCell2 R_a 11	437	977u
xCell2 R_a 12	651	977u
xCell2 R_a 13	1001	977u
xCell2 R_a 14	1458	977u
R_a3x	-	-
xCell3 R_a flag	FFFF	
xCell3 R_a 0	160	977u
xCell3 R_a 1	166	977u
xCell3 R_a 2	153	977u
xCell3 R_a 3	151	977u
xCell3 R_a 4	145	977u
xCell3 R_a 5	152	977u
xCell3 R_a 6	176	977u
xCell3 R_a 7	204	977u
xCell3 R_a 8	222	977u
xCell3 R_a 9	254	977u
xCell3 R_a 10	315	977u
xCell3 R_a 11	437	977u
xCell3 R_a 12	651	977u
xCell3 R_a 13	1001	977u
xCell3 R_a 14	1458	977u

Cell0 R_a flag,
Cell1 R_a flag,
Cell2 R_a flag,
Cell3 R_a flag,
xCell0 R_a flag,
xCell1 R_a flag,
xCell2 R_a flag,
xCell3 R_a flag

Each subclass (R_a0-R_a3 and R_a0x-R_a3x) in the Ra Table class is a separate profile of resistance values normalized at 0 degrees for each of the cells in a design (cells 0–3) There are 2 profiles for each cell. They are denoted by the x or absence of the x at the end of the subclass Title:
R_a0 or **R_a0x** for cell 0
R_a1 or **R_a1x** for cell 1
R_a2 or **R_a2x** for cell 2
R_a3 or **R_a3x** for cell 3
The purpose for 2 profiles for each series cell is to ensure that at any given time there is at least one profile is enabled and being used while attempts can be made to update the alternate profile without interference. Having 2 profiles also helps reduce stress on the Flash Memory. At the beginning of each of the 8 subclasses (profiles) is a flag called *CellM R_a flag* or *xCellM R_a flag* where “M” is the cell number (0-3). This flag is a status flag indicates the validity of the table data associated with this flag and whether this particular table is enabled/disabled. There are 2 bytes in each flag:

1. The LSB (least significant byte) indicates whether the table is currently enabled or disabled. It has the following options:
   a. 0x00 : Means the table has had a resistance update in the past; however, it is not the currently enabled table for this cell. (the alternate table for the indicated cell must be enabled at this time)
   b. 0xff: This means that the values in this table are default values. This table resistance values have never been updated, and this table is not the currently enabled table for this cell. (the alternate table for the indicated cell must be enabled at this time)
   c. 0x55: This means that this table is enabled for the indicated cell (the alternate table must be disabled at this time.)
2. The MSB (Most significant byte) indicates that status of the data in this particular table. The possible values for this byte are:
   a. 0x00: The data associated with this flag has had a resistance update and the *QMax Pack* has been updated
   b. 0x05: The resistance data associated with this flag has been updated and the pack is no longer discharging (this is prior to a *Qmax Pack* update).
   c. 0x55: The resistance data associated with this flag has been updated and the pack is still discharging (Qmax update attempt not possible until discharging stops).
   d. 0xff: The resistance data associated with this flag is all default data.

This data is used by the bq20z70 to determine which tables need updating and which tables are being used for the Impedance Track™ algorithm.
Normal Setting: This data is used by the bq20z70 Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This description of the *xCellM R_a flags* are intended for information purposes only. It is not intended to give a detailed functional description for the bq20z70 resistance algorithms.

Cell0 R_a0 – Cell0 R_a14,
xCell0 R_a0 – xCell0 R_a14,
Cell1 R_a0 – Cell1 R_a14,
xCell1 R_a0 – xCell1 R_a14,
Cell2 R_a0 – Cell2 R_a14,
xCell2 R_a0 – xCell2 R_a14,
Cell3 R_a0 – Cell3 R_a14,
xCell3 R_a0 – xCell3 R_a14,
There are 15 values for each R_a subclass in the **Ra Table** class. Each of these values represent a resistance value normalized at 0°C for the associated *Qmax Pack* based SOC gridpoint as found by the following rules:

For *CellN R_aM* where:

1. if $0 \le M \le 8$: The data is the resistance normalized at 0° for: SOC = 100% – (M $\times$ 10%)

2. if $9 \leq M \leq 14$: The data is the resistance normalized at 0 degrees for:
   $SOC = 100\% – [80\% + (M – 8) \times 3.3\%]$

This gives a profile of resistance throughout the entire SOC profile of the battery cells concentrating more on the values closer to 0%.

Normal Setting: SOC as stated in this description is based on *Qmax Pack*. It is not derived as a function of RSOC or ASOC. These resistance profiles are used by the bq20z70 for the Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This resistance profile description is for information purposes only. It is not intended to give a detailed functional description for the bq20z70 resistance algorithms. It is important to note that this data is in units of milliohms and is normalized to 0°C. Note this data throughout the application development cycle:

1. Watch for negative values in the **Ra Table** class. There should never be negative numbers in profiles anywhere in this class.
2. Watch for smooth consistent transitions from one profile gridpoint value to the next throughout each profile. As the bq20z70 does resistance profile updates these values should be roughly consistent from one learned update to another without huge jumps in consecutive gridpoints.

Chapter 4

bq20z70, bq20z80, bq20z90 Data Flash Comparison

Battery Management

ABSTRACT

This document compares the dataflash values and functionality of the bq20z70-V110, bq20z80-V102 and the bq20z90-V110 family of gas gauges.

4.1 1st Level Safety

Table 19. 1st Level Safety

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
0	Voltage	COV Threshold	0	3700 to 4700	0	3700 to 5000	0	3700 to 5000
		COV Time	2	0 to 60	2	0 to 240		2
		COV Recovery	3	3900 to 4400	3	0 to 4400	3	0 to 4400
		COV Delta	5	0 to 200	5	0 to 200		
		COV Temp. Hys	6	0 to 250	6	0 to 250		
		POV Threshold	7	0 to 18000	7	0 to 18000		
		POV Time	9	0 to 60	9	0 to 240		
		POV Recovery	10	0 to 17000	10	0 to 17000		
		CUV Threshold	12	0 to 3500	12	0 to 3500	12	0 to 3500
		CUV Time	14	0 to 60	14	0 to 240		2
		CUV Recovery	15	0 to 3600	15	0 to 3600	15	0 to 3600
		PUV Threshold	17	0 to 16000	17	0 to 16000		
		PUV Time	19	0 to 60	19	0 to 240		
		PUV Recovery	20	0 to 16000	20	0 to 16000		
1	Current	OC (1st Tier) Chg	0	0 to 20000	0	0 to 20000	0	0 to 20000
		OC (1st Tier) Chg Time	2	0 to 60	2	0 to 240		2
		OC Chg Recovery	3	–1000 to 1000	3	–1000 to 1000		100
		OC (1st Tier) Dsg	5	0 to 20000	5	0 to 20000	5	0 to 20000
		OC (1st Tier) Dsg Time	7	0 to 60	7	0 to 240		2
		OC Dsg Recovery	8	0 to 1000	8	0 to 1000		100
		OC (2nd Tier) Chg	10	0 to 20000	10	0 to 20000		
		OC (2nd Tier) Chg Time	12	0 to 60	12	0 to 240		
		OC (2nd Tier) Dsg	13	0 to 22000	13	0 to 22000		
		OC (2nd Tier) Dsg Time	15	0 to 60	15	0 to 240		
		Current Recovery Time	16	0 to 60	16	0 to 240	16	0 to 240
		AFE OC Dsg	17	0x00 to 0xFF	17	0x00 to 0xFF	17	0x00 to 0xFF
		AFE OC Dsg Time	18	0x00 to 0xFF	18	0x00 to 0xFF	18	0x00 to 0xFF
		AFE OC Dsg Recovery	19	10 to 1000	19	10 to 1000		100
		AFE SC Chg Cfg	21	0x00 to 0xFF	21	0x00 to 0xFF	21	0x00 to 0xFF
		AFE SC Dsg Cfg	22	0x00 to 0xFF	22	0x00 to 0xFF	22	0x00 to 0xFF
		AFE SC Recovery	23	0 to 200	23	0 to 200		5
2	Temperature	Over Temp Chg	0	0 to 1200	0	0 to 1200	0	0 to 1200
		OT Chg Time	2	0 to 60	2	0 to 240		2
		OT Chg Recovery	3	0 to 1200	3	0 to 1200	3	0 to 1200
		Over Temp Dsg	5	0 to 1200	5	0 to 1200	5	0 to 1200
		OT Dsg Time	7	0 to 60	7	0 to 240		2
		OT Dsg Recovery	8	0 to 1200	8	0 to 1200	8	0 to 1200
3	Host Comm	Host Watchdog Timeout	0	0 to 255	0	0 to 255		

4.2 2nd Level Safety

Table 20. 2nd Level Safety

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
16	Voltage	SOV Threshold	0	0 to 20000	0	0 to 20000	0	0 to 20000
		SOV Time	2	0 to 30	2	0 to 240	2	0 to 240
		Cell Imbalance Current	3	0 to 200	3	0 to 200	3	0 to 200
		Cell Imbalance Fail Voltage	4	0 to 5000	4	0 to 5000	4	0 to 5000
		Cell Imbalance Time	6	0 to 30	6	0 to 240	6	0 to 240
		Battery Rest Time	7	0 to 65535	7	0 to 65535	7	0 to 65535
		PFIN Detect Time	9	0 to 30	9	0 to 240	9	0 to 240
17	Current	SOC Chg	0	0 to 30000	0	0 to 30000	0	0 to 30000
		SOC Chg Time	2	0 to 30	2	0 to 240	2	0 to 240
		SOC Dsg	3	0 to 30000	3	0 to 30000	3	0 to 30000
		SOC Dsg Time	5	0 to 30	5	0 to 240	5	0 to 240
18	Temperature	SOT Chg	0	0 to 1200	0	0 to 1200	0	0 to 1200
		SOT Chg Time	2	0 to 30	2	0 to 240	2	0 to 240
		SOT Dsg	3	0 to 1200	3	0 to 1200	3	0 to 1200
		SOT Dsg Time	5	0 to 30	5	0 to 240	5	0 to 240
		Open Thermistor	6	–1000 to – 333	6	–1000 to – 333		
		Open Time	8	0 to 30	8	0 to 240		
19	FET Verification	FET Fail Limit	0	0 to 500	0	0 to 500		50
		FET Fail Time	2	0 to 30	2	0 to 240	2	0 to 240
20	AFE Verification	AFE Check Time	0	0 to 255	0	0 to 255		
		AFE Fail Limit	1	0 to 255	1	0 to 255	1	0 to 255
		AFE Fail Recovery Time	2	0 to 255	2	0 to 255		20
		AFE Init Retry Limit	3	0 to 255	3	0 to 255		
		AFE Init Limit	4	0 to 255	4	0 to 255		
21	Fuse Verification	Fuse Fail Limit	0	0 to 20	0	0 to 20		
		Fuse Fail Time	2	0 to 30	2	0 to 240		

4.3 Charge Control

Table 21. Charge Control

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
32	Charge Inhibit Cfg	Chg Inhibit Temp Low	0	–400 to 1200	0	–400 to 1200	0	–400 to 1200
		Chg Inhibit Temp High	2	–400 to 1200	2	–400 to 1200	2	–400 to 1200
		Temp Hys.	4	0 to 100	4	0 to 100		50
33	Pre-Chg Cfg	Pre-chg Current	0	0 to 2000	0	0 to 2000	0	0 to 2000
		Pre-chg Temp	2	–400 to 1200	2	–400 to 1200	2	–400 to 1200
		Pre-chg Voltage	4	0 to 20000	4	0 to 20000	4	0 to 20000
		Recovery Voltage	6	0 to 20000	6	0 to 20000	6	0 to 20000
34	Fast Charge Cfg	Fast Charge Current	0	0 to 10000	0	0 to 10000	0	0 to 10000
		Charging Voltage	2	0 to 20000	2	0 to 20000	2	0 to 20000
		Over Charging Voltage	4	0 to 2000				
		Delta Temp	6	0 to 500	4	0 to 500		
		Suspend Low Temp	8	–400 to 1200	6	–400 to 1200	6	–400 to 1200
		Suspend High Temp	10	–400 to 1200	8	–400 to 1200	8	–400 to 1200
35	Pulse Charge Cfg	Turn ON Voltage	0	0 to 5000	0	0 to 5000		
		Turn OFF Voltage	2	0 to 5000	2	0 to 5000		
		Max ON Pulse Time	4	0 to 240	4	0 to 240		
		Min OFF Pulse Time	5	0 to 240	5	0 to 240		
		Max OFF Voltage	6	0 to 5000	6	0 to 5000		
36	Termination Cfg.	Maintenance Current	0	0 to 1000	0	0 to 1000		0
		Taper Current	2	0 to 1000	2	0 to 1000	2	0 to 1000
		Termination Voltage	6	0 to 1000				
		Taper Voltage			6	0 to 1000	6	0 to 1000
		Current Taper Window	8	0 to 60	8	0 to 240		40
		TCA Set %	9	–1 to 100	9	–1 to 100		
		TCA Clear %	10	–1 to 100	10	–1 to 100	10	–1 to 100
		FC Set %	11	–1 to 100	11	–1 to 100		
		FC Clear %	12	–1 to 100	12	–1 to 100	12	–1 to 100
37	Cell Balancing Cfg	Min Cell Deviation	0	0 to 65535	0	0 to 65535	0	0 to 65535
38	Charging Faults	Over Charging Voltage	0	0 to 3000	0	0 to 3000		
		Over Charging Volt Time	2	0 to 60	2	0 to 240		
		Over Charging Current	3	0 to 2000	3	0 to 2000		
		Over Charging Curr Time	5	0 to 60	5	0 to 240		
		Over Charging Curr Recov	6	0 to 2000	6	0 to 2000		
		Depleted Voltage	8	0 to 16000	8	0 to 16000		
		Depleted Voltage Time	10	0 to 60	10	0 to 240		
		Depleted Recovery	11	0 to 16000	11	0 to 16000		
		Over Charge Capacity	13	0 to 4000	13	0 to 4000	13	0 to 4000
		Over Charge Recovery	15	0 to 100	15	0 to 100		2
		FC-MTO	17	0 to 65535	17	0 to 65535		
		PC-MTO	19	0 to 65535	19	0 to 65535		
		Charge Fault Cfg	21	0x0000 to 0xffff	21	0x0000 to 0xffff		

4.4 SBS Configuration

Table 22. SBS Configuration

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
48	SBS Configuration	Rem Cap Alarm	0	0 to 700	0	0 to 700	0	0 to 700
		Rem Energy Alarm			2	0 to 1000	2	0 to 1000
		Rem Time Alarm	2	0 to 30	4	0 to 30	4	0 to 240
		Init Battery Mode	4	0x0000 to 0xffff	6	x0000 to 0xffff	6	x0000 to 0xffff
		Design Voltage	6	7000 to 18000	8	7000 to 18000	8	7000 to 18000
		Spec Info	8	0x0000 to 0xffff	10	0x0000 to 0xffff	10	0x0000 to 0xffff
		Manuf Date	10	0 to 65535	12	0 to 65535	12	0 to 65535
		Ser. Num.	12	0x0000 to 0xffff	14	0x0000 to 0xffff	14	0x0000 to 0xffff
		Cycle Count	14	0 to 65535	16	0 to 65535	16	0 to 65535
		CC Threshold	16	100 to 32767	18	100 to 32767	18	100 to 32767
		CC %	18	0 to 100	20	0 to 100		
		CF MaxError Limit	19	0 to 100	21	0 to 100	21	0 to 100
		Design Capacity	20	0 to 65535	22	0 to 65535	22	0 to 65535
		Design Energy	22	0 to 65535	24	0 to 65535	24	0 to 65535
		Manuf Name	24	11 Char String	26	11 Char String	26	11 Char String
		Device Name	36	7 Char String	38	7 Char String	38	7 Char String
		Device Chemistry	44	4 Char String	46	4 Char String	46	4 Char String
49	Configuration	TDA Set %	0	-1 to 100	0	-1 to 100	0	-1 to 100
		TDA Clear %	1	-1 to 100	1	-1 to 100	1	-1 to 100
		FD Set %	2	-1 to 100	2	-1 to 100	2	-1 to 100
		FD Clear %	3	-1 to 100	3	-1 to 100	3	-1 to 100
		TDA Set Volt Threshold	4	0 to 16800	4	0 to 16800	4	0 to 16800
		TDA Set Volt Time	6	0 to 60	6	0 to 240	6	0 to 240
		TDA Clear Volt	7	0 to 16800	7	0 to 16800	7	0 to 16800
		FD Set Volt Threshold	9	0 to 16800	9	0 to 16800		
		FD Volt Time	11	0 to 60	11	0 to 240		
		FD Clear Volt	12	0 to 16800	12	0 to 16800		

4.5 System Data

Table 23. System Data

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
56	Manufacturer Data	Pack Lot Code	0	0x0000 to 0xffff	0	0x0000 to 0xffff		
		PCB Lot Code	2	0x0000 to 0xffff	2	0x0000 to 0xffff		
		Firmware Version	4	0x0000 to 0xffff	4	0x0000 to 0xffff		
		Hardware Revision	6	0x0000 to 0xffff	6	0x0000 to 0xffff		
		Cell Revision	8	0x0000 to 0xffff	8	0x0000 to 0xffff		
58	Manufacturer Info	Manuf. Info	0	8 Char String	0	20 Char String	0	20 Char String
59	Lifetime Data	Lifetime Max Temp	0	0 to 1400	0	0 to 1400		
		Lifetime Min Temp	2	–600 to 1400	2	–600 to 1400		
		Lifetime Max Cell Voltage	4	0 to 65535	4	0 to 32767		
		Lifetime Min Cell Voltage	6	0 to 65535	6	0 to 32767		
		Lifetime Max Pack Voltage	8	0 to 65535	8	0 to 32767		
		Lifetime Min Pack Voltage	10	0 to 65535	10	0 to 32767		
		Lifetime Max Chg Current	12	0 to 65535	12	–32768 to 32767		
		Lifetime Max Dsg Current	14	0 to 65535	14	–32768 to 32767		
		Lifetime Max Chg Power	16	0 to 65535	16	–32768 to 32767		
		Lifetime Max Dsg Power	18	0 to 65535	18	–32768 to 32767		
		Lifetime Max AvgDsg Cur	22	0 to 65535	22	–32768 to 32767		
		Lifetime Max AvgDsg Pow	26	0 to 65535	26	–32768 to 32767		
		Lifetime Avg Temp	28	0 to 1400	2	–40 to 1400		
60	Lifetime Temp Samples	LT Temp Samples	0	0 to 140000000	0	0 to 140000000		

4.6 Configuration

Table 24. Configuration

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
64	Registers	Operation Cfg A	0	0x0000 to 0xffff	0	0x0000 to 0xffff	0	0x0000 to 0xffff
		Operation Cfg B	2	0x0000 to 0xffff	2	0x0000 to 0xffff	2	0x0000 to 0xffff
		Operation Cfg C			4	0x0000 to 0xffff	4	0x0000 to 0xffff
		Permanent Fail Cfg	4	0x0000 to 0xffff	6	0x0000 to 0xffff	6	0x0000 to 0xffff
		Non-Removable Cfg	6	0x0000 to 0xffff	8	0x0000 to 0xffff	8	0x0000 to 0xffff

4.7 LED Support

Table 25. LED Support

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
67	LED Cfg	LED Flash Rate	0	0 to 65535	0	0 to 65535		
		LED Blink Rate	2	0 to 65535	2	0 to 65535		
		LED Delay	4	1 to 65535	4	1 to 65535		
		LED Hold TIme	6	0 to 255	6	0 to 255		
		CHG Flash Alarm	7	-1 to 101	7	-1 to 101		
		CHG Thresh 1	8	-1 to 101	8	-1 to 101		
		CHG Thresh 2	9	-1 to 101	9	-1 to 101		
		CHG Thresh 3	10	-1 to 101	10	-1 to 101		
		CHG Thresh 4	11	-1 to 101	11	-1 to 101		
		CHG Thresh 5	12	-1 to 101	12	-1 to 101		
		DSG Flash Alarm	13	-1 to 101	13	-1 to 101		
		DSG Thresh 1	14	-1 to 101	14	-1 to 101		
		DSG Thresh 2	15	-1 to 101	15	-1 to 101		
		DSG Thresh 3	16	-1 to 101	16	-1 to 101		
		DSG Thresh 4	17	-1 to 101	17	-1 to 101		
		DSG Thresh 5	18	-1 to 101	18	-1 to 101		
		Sink Current			19	0 to 3		

4.8 Power

Table 26. Power

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
68	Power	Flash Update OK Voltage	0	6000 to 20000	0	6000 to 20000	0	6000 to 20000
		Shutdown Voltage	2	5000 to 20000	2	5000 to 20000	2	5000 to 20000
		Shutdown Time	4	0 to 60	4	0 to 240		10
		Charger Present	5	0 to 23000	5	0 to 23000	5	0 to 23000
		Sleep Current	7	0 to 100	7	0 to 100		10
		Bus Low Time	9	0 to 255	9	0 to 255		5
		Cal Inhibit Temp Low	10	–400 to 1200	10	–400 to 1200		50
		Cal Inhibit Temp High	12	–400 to 1200	12	–400 to 1200		450
		Sleep Voltage Time	14	0 to 100	14	0 to 240		5
		Sleep Current Time	15	0 to 255	15	0 to 255		20
		Wake Current Reg			16	0x00 to 0xff	16	0x00 to 0xff

4.9 Gas Gauging

Table 27. Gas Gauging

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
80	IT Config	Load Select	0	0 to 255	0	0 to 255	0	0 to 255
		Load Mode	1	0 to 255	1	0 to 255	1	0 to 255
		Term Voltage	45	–32768 to 32767	45	–32768 to 32767	45	–32768 to 32767
		User Rate-mA	60	–9000 to –2000	60	2000 to 9000	60	2000 to 9000
		User Rate-mW	62	–14000 to –3000	62	3000 to 14000	62	3000 to 14000
		Reserve Cap-mAh	64	0 to 9000	64	0 to 9000	64	0 to 9000
		Reserve Cap-mWh	66	0 to 14000	66	0 to 14000	66	0 to 14000
81	Current Thresholds	Dsg Current Threshold	0	0 to 2000	0	0 to 2000	0	0 to 2000
		Chg Current Threshold	2	0 to 2000	2	0 to 2000	2	0 to 2000
		Quit Current	4	0 to 1000	4	0 to 1000	4	0 to 1000
		Dsg Relax Time	6	0 to 255	6	0 to 240		1
		Chg Relax Time	8	0 to 255	8	0 to 240		60
82	State	Qmax Cell 0	0	0 to 65535	0	0 to 32767	0	0 to 32767
		Qmax Cell 1	2	0 to 65535	2	0 to 32767	2	0 to 32767
		Qmax Cell 2	4	0 to 65535	4	0 to 32767	4	0 to 32767
		Qmax Cell 3	6	0 to 65535	6	0 to 32767	6	0 to 32767
		Qmax Pack	8	0 to 65535	8	0 to 32767	8	0 to 32767
		Update Status	12	0x00 to 0x06	12	0x00 to 0x06	12	0x00 to 0x06
		Avg I Last Run	21	–32768 to 32767	21	–32768 to 32767		
		Avg P Last Run	23	–32768 to 32767	23	–32768 to 32767		
		Delta Voltage	25	–32768 to 32767	25	–32768 to 32767	25	–32768 to 32767

4.10 Ra Table

Table 28. Ra Table

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
88	R_a0	Cell0 R-a flag	0	0x0000 to xffff	0	0x0000 to xffff	0	0x0000 to xffff
		Cell0 R_a 0	2	-32768 to 32767	2	-32768 to 32767	2	-32768 to 32767
		Cell0 R_a 1	4	-32768 to 32767	4	-32768 to 32767	4	-32768 to 32767
		Cell0 R_a 2	6	-32768 to 32767	6	-32768 to 32767	6	-32768 to 32767
		Cell0 R_a 3	8	-32768 to 32767	8	-32768 to 32767	8	-32768 to 32767
		Cell0 R_a 4	10	-32768 to 32767	10	-32768 to 32767	10	-32768 to 32767
		Cell0 R_a 5	12	-32768 to 32767	12	-32768 to 32767	12	-32768 to 32767
		Cell0 R_a 6	14	-32768 to 32767	14	-32768 to 32767	14	-32768 to 32767
		Cell0 R_a 7	16	-32768 to 32767	16	-32768 to 32767	16	-32768 to 32767

Table 28. Ra Table (continued)

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
		Cell0 R_a 8	18	-32768 to 32767	18	-32768 to 32767	18	-32768 to 32767
		Cell0 R_a 9	20	-32768 to 32767	20	-32768 to 32767	20	-32768 to 32767
		Cell0 R_a 10	22	-32768 to 32767	22	-32768 to 32767	22	-32768 to 32767
		Cell0 R_a 11	24	-32768 to 32767	24	-32768 to 32767	24	-32768 to 32767
		Cell0 R_a 12	26	-32768 to 32767	26	-32768 to 32767	26	-32768 to 32767
		Cell0 R_a 13	28	-32768 to 32767	28	-32768 to 32767	28	-32768 to 32767
		Cell0 R_a 14	30	-32768 to 32767	30	-32768 to 32767	30	-32768 to 32767
89	R_a1	Cell1 R-a flag	0	0x0000 to xffff	0	0x0000 to xffff	0	0x0000 to xffff
		Cell1 R_a 0	2	-32768 to 32767	2	-32768 to 32767	2	-32768 to 32767
		Cell1 R_a 1	4	-32768 to 32767	4	-32768 to 32767	4	-32768 to 32767
		Cell1 R_a 2	6	-32768 to 32767	6	-32768 to 32767	6	-32768 to 32767
		Cell1 R_a 3	8	-32768 to 32767	8	-32768 to 32767	8	-32768 to 32767
		Cell1 R_a 4	10	-32768 to 32767	10	-32768 to 32767	10	-32768 to 32767
		Cell1 R_a 5	12	-32768 to 32767	12	-32768 to 32767	12	-32768 to 32767
		Cell1 R_a 6	14	-32768 to 32767	14	-32768 to 32767	14	-32768 to 32767
		Cell1 R_a 7	16	-32768 to 32767	16	-32768 to 32767	16	-32768 to 32767
		Cell1 R_a 8	18	-32768 to 32767	18	-32768 to 32767	18	-32768 to 32767
		Cell1 R_a 9	20	-32768 to 32767	20	-32768 to 32767	20	-32768 to 32767
		Cell1 R_a 10	22	-32768 to 32767	22	-32768 to 32767	22	-32768 to 32767
		Cell1 R_a 11	24	-32768 to 32767	24	-32768 to 32767	24	-32768 to 32767
		Cell1 R_a 12	26	-32768 to 32767	26	-32768 to 32767	26	-32768 to 32767
		Cell1 R_a 13	28	-32768 to 32767	28	-32768 to 32767	28	-32768 to 32767
		Cell1 R_a 14	30	-32768 to 32767	30	-32768 to 32767	30	-32768 to 32767
90	R_a2	Cell2 R-a flag	0	0x0000 to xffff	0	0x0000 to xffff	0	0x0000 to xffff
		Cell2 R_a 0	2	-32768 to 32767	2	-32768 to 32767	2	-32768 to 32767
		Cell2 R_a 1	4	-32768 to 32767	4	-32768 to 32767	4	-32768 to 32767
		Cell2 R_a 2	6	-32768 to 32767	6	-32768 to 32767	6	-32768 to 32767
		Cell2 R_a 3	8	-32768 to 32767	8	-32768 to 32767	8	-32768 to 32767
		Cell2 R_a 4	10	-32768 to 32767	10	-32768 to 32767	10	-32768 to 32767
		Cell2 R_a 5	12	-32768 to 32767	12	-32768 to 32767	12	-32768 to 32767

Table 28. Ra Table (continued)

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
		Cell2 R_a 6	14	-32768 to 32767	14	-32768 to 32767	14	-32768 to 32767
		Cell2 R_a 7	16	-32768 to 32767	16	-32768 to 32767	16	-32768 to 32767
		Cell2 R_a 8	18	-32768 to 32767	18	-32768 to 32767	18	-32768 to 32767
		Cell2 R_a 9	20	-32768 to 32767	20	-32768 to 32767	20	-32768 to 32767
		Cell2 R_a 10	22	-32768 to 32767	22	-32768 to 32767	22	-32768 to 32767
		Cell2 R_a 11	24	-32768 to 32767	24	-32768 to 32767	24	-32768 to 32767
		Cell2 R_a 12	26	-32768 to 32767	26	-32768 to 32767	26	-32768 to 32767
		Cell2 R_a 13	28	-32768 to 32767	28	-32768 to 32767	28	-32768 to 32767
		Cell2 R_a 14	30	-32768 to 32767	30	-32768 to 32767	30	-32768 to 32767
91	R_a3	Cell3 R-a flag	0	0x0000 to xffff	0	0x0000 to xffff	0	0x0000 to xffff
		Cell3 R_a 0	2	-32768 to 32767	2	-32768 to 32767	2	-32768 to 32767
		Cell3 R_a 1	4	-32768 to 32767	4	-32768 to 32767	4	-32768 to 32767
		Cell3 R_a 2	6	-32768 to 32767	6	-32768 to 32767	6	-32768 to 32767
		Cell3 R_a 3	8	-32768 to 32767	8	-32768 to 32767	8	-32768 to 32767
		Cell3 R_a 4	10	-32768 to 32767	10	-32768 to 32767	10	-32768 to 32767
		Cell3 R_a 5	12	-32768 to 32767	12	-32768 to 32767	12	-32768 to 32767
		Cell3 R_a 6	14	-32768 to 32767	14	-32768 to 32767	14	-32768 to 32767
		Cell3 R_a 7	16	-32768 to 32767	16	-32768 to 32767	16	-32768 to 32767
		Cell3 R_a 8	18	-32768 to 32767	18	-32768 to 32767	18	-32768 to 32767
		Cell3 R_a 9	20	-32768 to 32767	20	-32768 to 32767	20	-32768 to 32767
		Cell3 R_a 10	22	-32768 to 32767	22	-32768 to 32767	22	-32768 to 32767
		Cell3 R_a 11	24	-32768 to 32767	24	-32768 to 32767	24	-32768 to 32767
		Cell3 R_a 12	26	-32768 to 32767	26	-32768 to 32767	26	-32768 to 32767
		Cell3 R_a 13	28	-32768 to 32767	28	-32768 to 32767	28	-32768 to 32767
		Cell3 R_a 14	30	-32768 to 32767	30	-32768 to 32767	30	-32768 to 32767
92	R_a0x	xCell0 R-a flag	0	0x0000 to xffff	0	0x0000 to xffff	0	0x0000 to xffff
		xCell0 R_a 0	2	-32768 to 32767	2	-32768 to 32767	2	-32768 to 32767
		xCell0 R_a 1	4	-32768 to 32767	4	-32768 to 32767	4	-32768 to 32767
		xCell0 R_a 2	6	-32768 to 32767	6	-32768 to 32767	6	-32768 to 32767
		xCell0 R_a 3	8	-32768 to 32767	8	-32768 to 32767	8	-32768 to 32767

Table 28. Ra Table (continued)

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
		xCell0 R_a 4	10	-32768 to 32767	10	-32768 to 32767	10	-32768 to 32767
		xCell0 R_a 5	12	-32768 to 32767	12	-32768 to 32767	12	-32768 to 32767
		xCell0 R_a 6	14	-32768 to 32767	14	-32768 to 32767	14	-32768 to 32767
		xCell0 R_a 7	16	-32768 to 32767	16	-32768 to 32767	16	-32768 to 32767
		xCell0 R_a 8	18	-32768 to 32767	18	-32768 to 32767	18	-32768 to 32767
		xCell0 R_a 9	20	-32768 to 32767	20	-32768 to 32767	20	-32768 to 32767
		xCell0 R_a 10	22	-32768 to 32767	22	-32768 to 32767	22	-32768 to 32767
		xCell0 R_a 11	24	-32768 to 32767	24	-32768 to 32767	24	-32768 to 32767
		xCell0 R_a 12	26	-32768 to 32767	26	-32768 to 32767	26	-32768 to 32767
		xCell0 R_a 13	28	-32768 to 32767	28	-32768 to 32767	28	-32768 to 32767
		xCell0 R_a 14	30	-32768 to 32767	30	-32768 to 32767	30	-32768 to 32767
93	R_a1x	xCell1 R-a flag	0	0x0000 to xffff	0	0x0000 to xffff	0	0x0000 to xffff
		xCell1 R_a 0	2	-32768 to 32767	2	-32768 to 32767	2	-32768 to 32767
		xCell1 R_a 1	4	-32768 to 32767	4	-32768 to 32767	4	-32768 to 32767
		xCell1 R_a 2	6	-32768 to 32767	6	-32768 to 32767	6	-32768 to 32767
		xCell1 R_a 3	8	-32768 to 32767	8	-32768 to 32767	8	-32768 to 32767
		xCell1 R_a 4	10	-32768 to 32767	10	-32768 to 32767	10	-32768 to 32767
		xCell1 R_a 5	12	-32768 to 32767	12	-32768 to 32767	12	-32768 to 32767
		xCell1 R_a 6	14	-32768 to 32767	14	-32768 to 32767	14	-32768 to 32767
		xCell1 R_a 7	16	-32768 to 32767	16	-32768 to 32767	16	-32768 to 32767
		xCell1 R_a 8	18	-32768 to 32767	18	-32768 to 32767	18	-32768 to 32767
		xCell1 R_a 9	20	-32768 to 32767	20	-32768 to 32767	20	-32768 to 32767
		xCell1 R_a 10	22	-32768 to 32767	22	-32768 to 32767	22	-32768 to 32767
		xCell1 R_a 11	24	-32768 to 32767	24	-32768 to 32767	24	-32768 to 32767
		xCell1 R_a 12	26	-32768 to 32767	26	-32768 to 32767	26	-32768 to 32767
		xCell1 R_a 13	28	-32768 to 32767	28	-32768 to 32767	28	-32768 to 32767
		xCell1 R_a 14	30	-32768 to 32767	30	-32768 to 32767	30	-32768 to 32767
94	R_a2x	xCell2 R-a flag	0	0x0000 to xffff	0	0x0000 to xffff	0	0x0000 to xffff
		xCell2 R_a 0	2	-32768 to 32767	2	-32768 to 32767	2	-32768 to 32767
		xCell2 R_a 1	4	-32768 to 32767	4	-32768 to 32767	4	-32768 to 32767

Table 28. Ra Table (continued)

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
		xCell2 R_a 2	6	-32768 to 32767	6	-32768 to 32767	6	-32768 to 32767
		xCell2 R_a 3	8	-32768 to 32767	8	-32768 to 32767	8	-32768 to 32767
		xCell2 R_a 4	10	-32768 to 32767	10	-32768 to 32767	10	-32768 to 32767
		xCell2 R_a 5	12	-32768 to 32767	12	-32768 to 32767	12	-32768 to 32767
		xCell2 R_a 6	14	-32768 to 32767	14	-32768 to 32767	14	-32768 to 32767
		xCell2 R_a 7	16	-32768 to 32767	16	-32768 to 32767	16	-32768 to 32767
		xCell2 R_a 8	18	-32768 to 32767	18	-32768 to 32767	18	-32768 to 32767
		xCell2 R_a 9	20	-32768 to 32767	20	-32768 to 32767	20	-32768 to 32767
		xCell2 R_a 10	22	-32768 to 32767	22	-32768 to 32767	22	-32768 to 32767
		xCell2 R_a 11	24	-32768 to 32767	24	-32768 to 32767	24	-32768 to 32767
		xCell2 R_a 12	26	-32768 to 32767	26	-32768 to 32767	26	-32768 to 32767
		xCell2 R_a 13	28	-32768 to 32767	28	-32768 to 32767	28	-32768 to 32767
		xCell2 R_a 14	30	-32768 to 32767	30	-32768 to 32767	30	-32768 to 32767
95	R_a3x	xCell3 R-a flag	0	0x0000 to xffff	0	0x0000 to xffff	0	0x0000 to xffff
		xCell3 R_a 0	2	-32768 to 32767	2	-32768 to 32767	2	-32768 to 32767
		xCell3 R_a 1	4	-32768 to 32767	4	-32768 to 32767	4	-32768 to 32767
		xCell3 R_a 2	6	-32768 to 32767	6	-32768 to 32767	6	-32768 to 32767
		xCell3 R_a 3	8	-32768 to 32767	8	-32768 to 32767	8	-32768 to 32767
		xCell3 R_a 4	10	-32768 to 32767	10	-32768 to 32767	10	-32768 to 32767
		xCell3 R_a 5	12	-32768 to 32767	12	-32768 to 32767	12	-32768 to 32767
		xCell3 R_a 6	14	-32768 to 32767	14	-32768 to 32767	14	-32768 to 32767
		xCell3 R_a 7	16	-32768 to 32767	16	-32768 to 32767	16	-32768 to 32767
		xCell3 R_a 8	18	-32768 to 32767	18	-32768 to 32767	18	-32768 to 32767
		xCell3 R_a 9	20	-32768 to 32767	20	-32768 to 32767	20	-32768 to 32767
		xCell3 R_a 10	22	-32768 to 32767	22	-32768 to 32767	22	-32768 to 32767
		xCell3 R_a 11	24	-32768 to 32767	24	-32768 to 32767	24	-32768 to 32767
		xCell3 R_a 12	26	-32768 to 32767	26	-32768 to 32767	26	-32768 to 32767
		xCell3 R_a 13	28	-32768 to 32767	28	-32768 to 32767	28	-32768 to 32767
		xCell3 R_a 14	30	-32768 to 32767	30	-32768 to 32767	30	-32768 to 32767

4.11 PF Status

Table 29. PF Status

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
96	Device Status Data	PF Flags 1	0	0x0000 to 0xffff	0	0x0000 to 0xffff	0	0x0000 to 0xffff
		Fuse Flag	2	0x0000 to 0xffff	2	0x0000 to 0xffff		
		PF Voltage	4	0 to 65535	4	0 to 32767		
		PF C4 Voltage	6	0 to 9999	6	0 to 9999		
		PF C3 Voltage	8	0 to 9999	8	0 to 9999		
		PF C2 Voltage	10	0 to 9999	10	0 to 9999		
		PF C1 Voltage	12	0 to 9999	12	0 to 9999		
		PF Current	14	–32768 to 32767	14	–32768 to 32767		
		PF Temperature	16	–9999 to 9999	16	–9999 to 9999		
		PF Batt Stat	18	0x0000 to 0xffff	18	0x0000 to 0xffff		
		PF RC-mAh	20	0 to 65535	20	0 to 32767		
		PF RC-10mAh	22	0 to 65535	22	0 to 32767		
		PF Chg Status	24	0x0000 to 0xffff	24	0x0000 to 0xffff		
		PF Safety Status	26	0x0000 to 0xffff	26	0x0000 to 0xffff		
		PF Flags 2	28	0x0000 to 0xffff	28	0x0000 to 0xffff	28	0x0000 to 0xffff
97	AFE Regs	AFE Status	0	0x00 to 0xff	0	0x00 to 0xff		
		AFE Output	1	0x00 to 0xff	1	0x00 to 0xff		
		AFE Regs	2	0x00 to 0xff	2	0x00 to 0xff		
		AFE Function	3	0x00 to 0xff	3	0x00 to 0xff		
		AFE Cell Select	4	0x00 to 0xff	4	0x00 to 0xff		
		AFE OLV	5	0x00 to 0xff	5	0x00 to 0xff		
		AFE OLT	6	0x00 to 0xff	6	0x00 to 0xff		
		AFE SCC	7	0x00 to 0xff	7	0x00 to 0xff		
		AFE SCD	8	0x00 to 0xff	8	0x00 to 0xff		

4.12 Calibration

Table 30. Calibration

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
104	Data	CC Gain	0	–1.0E128 to 1.0E128	0	0.1 to 4	0	0.1 to 4
		CC Delta	4	–1.0E128 to 1.0E128	4	29826 to 1193046	4	29826 to 1193046
		Ref Voltage	8	0 to 32767	8	0 to 32767	8	0 to 32767
		AFE Corr	10	0 to 32767				
		AFE Pack Gain	12	0 to 65535	12	0 to 32767	12	0 to 32767
		CC Offset	14	–32768 to 32767	14	–32768 to 32767	14	–32768 to 32767
		Board Offset	16	–128 to 127	16	–32768 to 32767	16	–32768 to 32767

Table 30. Calibration (continued)

Subclass ID	SubClass	Name	bq20z80		bq20z90		bq20z70	
			Offset	Range	Offset	Range	Offset	Range
		Int Temp Offset	17	–128 to 127	18	–128 to 127	18	–128 to 127
		Ext1 Temp Offset	18	–128 to 127	19	–128 to 127	19	–128 to 127
		Ext2 Temp Offset	19	–128 to 127	20	–128 to 127	20	–128 to 127
105	Config	CC Current	0	0 to 65535	0	0 to 32767	0	0 to 32767
		Voltage Signal	2	0 to 65535	2	0 to 32767	2	0 to 32767
		Temp Signal	4	0 to 65535	4	0 to 32767	4	0 to 32767
		CC Offset Time	6	0 to 65535	6	0 to 65535	6	0 to 65535
		ADC Offset Time	8	0 to 65535	8	0 to 65535	8	0 to 65535
		CC Gain Time	10	0 to 65535	10	0 to 65535	10	0 to 65535
		Voltage Time	12	0 to 65535	12	0 to 65535	12	0 to 65535
		Temperature Time	14	0 to 65535	14	0 to 65535	14	0 to 65535
		Cal Mode Timeout	17	0 to 65535	17	0 to 65535	17	0 to 65535
106	Temp Model	Ext Coef 1	0	–32768 to 32767	0	–32768 to 32767	0	–32768 to 32767
		Ext Coef 2	2	–32768 to 32767	2	–32768 to 32767	2	–32768 to 32767
		Ext Coef 3	4	–32768 to 32767	4	–32768 to 32767	4	–32768 to 32767
		Ext Coef 4	6	–32768 to 32767	6	–32768 to 32767	6	–32768 to 32767
		Ext Min AD	8	–32768 to 32767	8	–32768 to 32767	8	–32768 to 32767
		Ext Max Temp	10	–32768 to 32767	10	–32768 to 32767	10	–32768 to 32767
		Int Coef 1	12	–32768 to 32767	12	–32768 to 32767	12	–32768 to 32767
		Int Coef 2	14	–32768 to 32767	14	–32768 to 32767	14	–32768 to 32767
		Int Coef 3	16	–32768 to 32767	16	–32768 to 32767	16	–32768 to 32767
		Int Coef 4	18	–32768 to 32767	18	–32768 to 32767	18	–32768 to 32767
		Int Min AD	20	–32768 to 32767	20	–32768 to 32767	20	–32768 to 32767
		Int Max Temp	22	–32768 to 32767	22	–32768 to 32767	22	–32768 to 32767
107	Current	Filter	0	0 to 255	0	0 to 255	0	0 to 255
		Deadband	1	0 to 255	1	0 to 255	1	0 to 255
		CC Deadband	2	0 to 255	2	0 to 255	2	0 to 255
		CC Max Deadband	3	0 to 255	3	0 to 255	3	0 to 255
		CC Deadband Sample	4	0 to 65535	4	0 to 65535	4	0 to 65535
		CC Max Offset Sample	6	0 to 65535	6	0 to 65535	6	0 to 65535

Chapter 5

Exploring the bq20z70/90 Impedance Track™ Evaluation Kit

Battery Management

ABSTRACT

The bq20z70/90 evaluation module (EVM) and its corresponding evaluation software provides a rich and effective environment for examining the bq20z70/90 – a new, advanced battery gas gauge. This application report covers this EVM and software with an emphasis on how to use it and what to expect. EVM board connections are discussed in detail, and helpful hints are offered. For the evaluation software, components of each major screen are presented along with the various menu options.

5.1 Connecting the EVM

The cell-connection terminal blocks provide screw terminals for connecting 2, 3, or 4 cells to the evaluation module (EVM). The numbering convention for batteries is that Cell 1 is the most negative; so, connect the 1N (N=negative) terminal on the EVM to the most negative point of your battery stack.

If evaluating a 3-cell application, connect both 3P and 4P (P = positive) to the top node of the cell stack. Similarly, for a 2-cell application, connect 2P, 3P, and 4P to the top node.

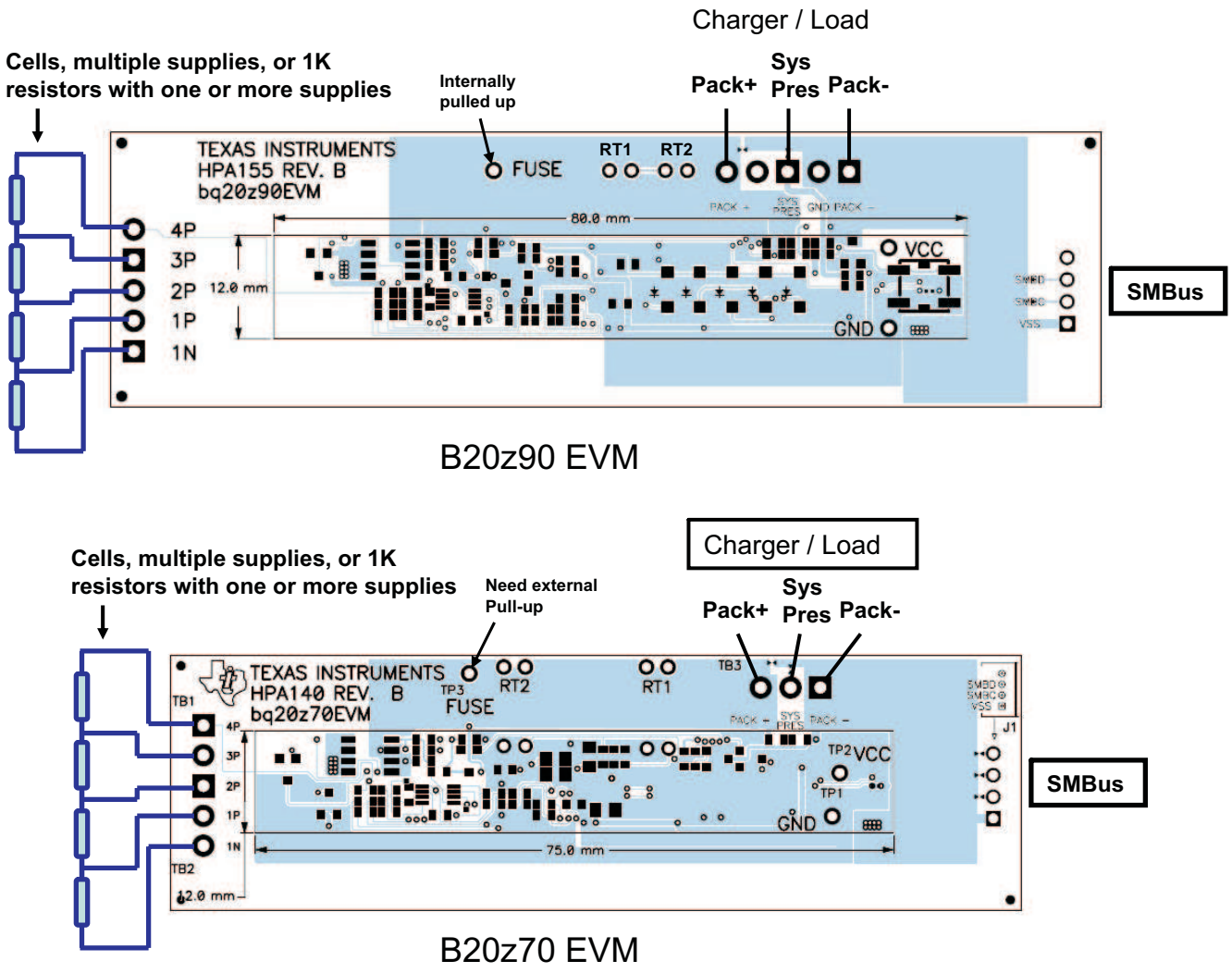


Figure 7. bq20z90 EVM Connections

Cells, Resistors, or Power Supplies?

For quick evaluation of the bq20z70/90 safety features, using real cells can be a burden. Therefore, substitute a string of 1-kΩ resistors fed with a single laboratory power supply. The supply can be varied quickly to investigate pack voltage protection. An additional floating supply can be connected across one of the resistors to simulate cell over- and undervoltages.

However, be aware that the Impedance Track™ algorithm, which relies on measuring the actual cell impedance, does not operate correctly without real cells.

Where is the Fuse?

The EVM does not include the chemical fuse that is employed in many battery pack applications. This eliminates the need for fuse replacement when running fault tests. Instead, the signal on the fuse test point is the control signal that would blow the fuse. It requires an external pullup resistor to the battery voltage in order to monitor its state on a scope or meter

System Present and Pack Connections

The Pack+ and Pack– connections are used to connect the load and charger. It may be convenient to simultaneously connect a laboratory power supply and an electronic load in parallel. Most electronic loads have a load on/off switch and adjusting the constant current limit control to zero can disable the laboratory power supply.

Simulating Current

If using a string of resistors to simulate cells, it is difficult to apply an actual charge current. The solution is to connect a floating laboratory power supply between Pack– and Battery– (1N). Putting the floating supply in current limit provides a simulated charge current that is forced through the sense resistor. Depending on the laboratory power supplies available, this configuration can be useful for load current by reversing the polarity of the current source connections. Use this configuration to quickly test various overcurrent safety features or to validate coulomb counting accuracy. However, be aware that this method bypasses the protection FETs, and fault conditions will not interrupt the charge or load current.

Simulating Temperature

Because the temperature measurement works by measuring the voltage on the thermistor pin, a temperature chamber for safety evaluation is unnecessary. Just connect a laboratory power supply across the RT1 terminals with polarity as shown in Figure 7 (see the EVM schematic located at the end of this document). In this case, this power supply does not have to be isolated from the supply used to simulate a charger/load because the return side of the thermistor is the same as Pack–. Forcing 0 V ~ 2 V across the thermistor allows testing the safety features over the full temperature range.

5.2 Scanning the SBS Registers

With the battery connections made, start the evaluation software. When first connected, the circuitry may be in shutdown mode. This normally requires applying a charging source across the Pack+ and Pack– terminals. If a charger voltage is not connected, briefly connect the positive battery voltage to Pack+.

Setting the Scan Interval

By default, the SBS register scanning is off. Put a check in the *Keep Scanning* box to get the scanning started. A periodic update of all the SBS registers should appear. Note the blue progress bar at the bottom. The interval between scans can be set in the Options | Set Scan Interval menu. The program remembers this setting and uses it each time the program is launched.

Adjusting the View

With some screen resolutions, it may not be possible to see all of the register displays simultaneously. In some cases, this can be improved by making the top buttons invisible. Use the View | Display Buttons menu to remove these objects from the screen (see Figure 8).

The Evaluation Software, EVSW, has the flexibility to allow multiple views. Two or three screens can be tiled onto the display at once. After opening any of the SBS, Data Flash, or Pro screens, use the Window menu to tile them either vertically or horizontally. Figure 9 shows a vertically tiled view of all three.

Figure 8. All Flags and Status Bits Are Visible on a 1024x768 Screen if the Top Display Buttons Are Hidden

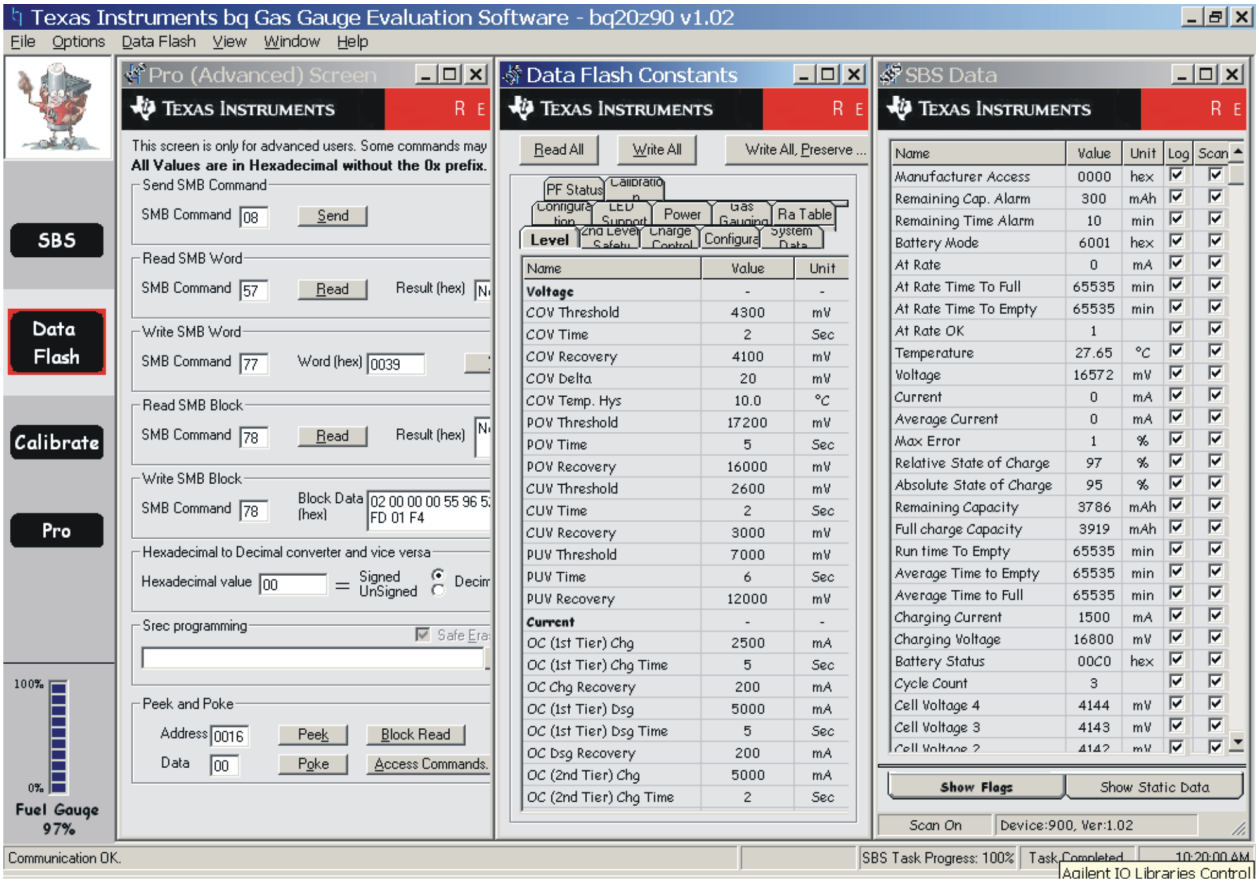


Figure 9. Vertically Tiled View of SBS, Data Flash, and Pro Screen

Flags/Status Bits

The flags and status bit displays are bit expansions of the various status, alert, and battery mode registers. The red bit cells are asserted, whereas the green cells are not. The displayed mnemonics are an improvement compared to decoding hexadecimal digits, but consult the data sheet to learn the full definition for each bit.

5.3 Logging the SBS Registers

Due to the long time associated with battery testing, it is common to data-log complete charge and discharge cycles for later analysis. When evaluating a new cell type, or a new gas gauge device, logs provide a convenient and effective way to understand the process.

Configuring the Log File

The log file can be configured to record any combination of the displayed SBS and extended registers. Simply check or uncheck the items to log. Select or deselect all of them quickly using the Options menu. It is usually a good idea to deselect the registers that are not relevant to the experiment being performed in order to simplify the process of reading the log later and to reduce the size of the log file.

The logging interval is also configured from a dialog box available in the options menu. Consider the purpose for the log when choosing an interval. If you expect to see several events during a short period, or are looking for a transient phenomenon, then a short interval, such as 1000 milliseconds can be used. This produces a huge file when run overnight, so decrease the resolution if it is not really necessary.

Start and stop the logging process with the buttons near the top of the screen. The state of the Start Logging and Stop Logging buttons immediately reveal if the program is logging or not.

Using Excel for Log File Evaluation

The log file is written as records of tab delimited ASCII. This file format can be imported into Microsoft™ Excel without any extra steps. Just right-click on the file name, and select Open With | Microsoft Excel for Windows™. However, one problem that can arise is with columns containing hexadecimal values. If the data contains an "e", Excel interprets this as scientific notation by default. If this situation occurs, use the import function in Excel, and modify the column type for the target column to be "text."

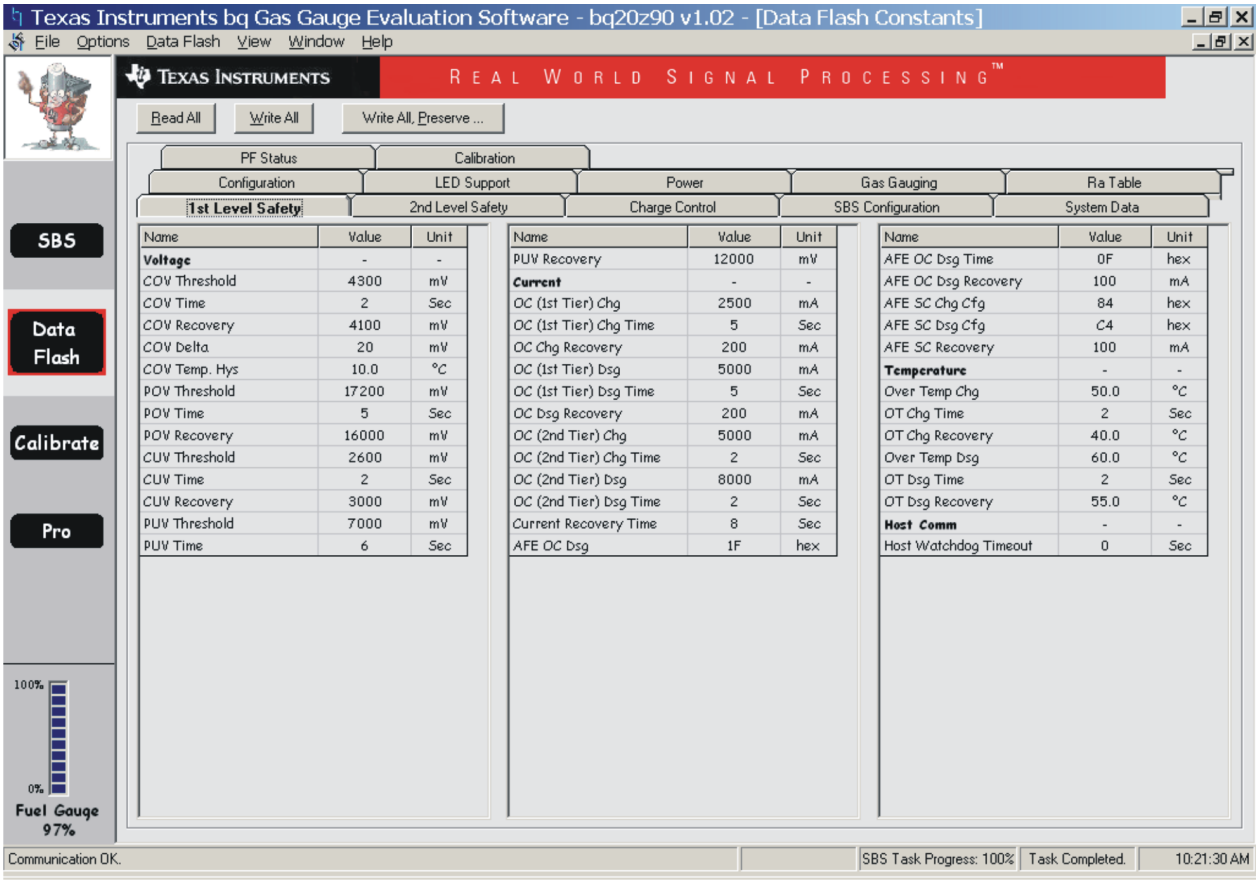
Microsoft Excel has a function in its Window menu called Freeze Panes, which is extremely helpful for reviewing long lists of records. Highlight the first row of data, under the heading row, and choose Freeze Panes from the Window menu. Now you can scroll through the entire log and still see the heading for each column. Sometimes, it is more convenient to delete the header information in lines 1 through 11.

5.4 Editing the Data Flash

The data flash screen displays the classes and subclasses used to categorize the data flash constants. The classes are on the index tabs at the top. Select a tab to activate the display for all the constants within that class. The 12 data flash constant classes are 1st Level Safety, 2nd Level Safety, Charge Control, Gas Gauging, SBS Configuration, Ra Table, Pf Status, Calibration, System Data, Configuration, LED Support, and Power. Help text for each constant is available by right-clicking the mouse when the cursor is over the name.

Navigating the Data Flash – Classes and Subclasses

The classes of constants are selected with the tabs; under each class are also subclass groupings . For example, click on the 1st Level Safety Tab. Shown in the grids are the various data flash constants with subclass indicators in bold type. In this case, the subclasses are Voltage, Current, Temperature, and Host Comm.



Name	Value	Unit
Voltage	-	-
COV Threshold	4300	mV
COV Time	2	Sec
COV Recovery	4100	mV
COV Delta	20	mV
COV Temp. Hys	10.0	°C
POV Threshold	17200	mV
POV Time	5	Sec
POV Recovery	16000	mV
CUV Threshold	2600	mV
CUV Time	2	Sec
CUV Recovery	3000	mV
PUV Threshold	7000	mV
PUV Time	6	Sec

Name	Value	Unit
PUV Recovery	12000	mV
Current	-	-
OC (1st Tier) Chg	2500	mA
OC (1st Tier) Chg Time	5	Sec
OC Chg Recovery	200	mA
OC (1st Tier) Dsg	5000	mA
OC (1st Tier) Dsg Time	5	Sec
OC Dsg Recovery	200	mA
OC (2nd Tier) Chg	5000	mA
OC (2nd Tier) Chg Time	2	Sec
OC (2nd Tier) Dsg	8000	mA
OC (2nd Tier) Dsg Time	2	Sec
Current Recovery Time	8	Sec
AFE OC Dsg	1F	hex

Name	Value	Unit
AFE OC Dsg Time	0F	hex
AFE OC Dsg Recovery	100	mA
AFE SC Chg Cfg	84	hex
AFE SC Dsg Cfg	C4	hex
AFE SC Recovery	100	mA
Temperature	-	-
Over Temp Chg	50.0	°C
OT Chg Time	2	Sec
OT Chg Recovery	40.0	°C
Over Temp Dsg	60.0	°C
OT Dsg Time	2	Sec
OT Dsg Recovery	55.0	°C
Host Comm	-	-
Host Watchdog Timeout	0	Sec

Figure 10. Example of bq20z70/90 Data Flash Organization. 1st Level Safety Class of Data Flash Constants. Subclasses are Voltage, Current, Temperature, and Host Comm.

Reading and Editing Data Flash

Use the Read All button initially to populate the grids. Make a change to any constant in the value column, and press Enter to write the new value into the device data flash. Note that data cannot be written to the device if it is sealed or in a permanent fail state.

Exporting and Auto Export

A list of all the data flash values may be stored to a text file with a .gg extension. The format of this file includes the class, subclass, name, and value for each data flash location. For example:

- [Voltage(1st Level Safety)]
- COV Threshold = 4350
- COV Time = 2
- COV Recovery = 3900
- COV Delta = 20
- COV Temp. Hys = 100
- POV Threshold = 13000
- POV Time = 2
- POV Recovery = 12600
- CUV Threshold = 2500
- CUV Time = 2
- CUV Recovery = 3000
- PUV Threshold = 8200
- PUV Time = 2
- PUV Recovery = 9000

Note that the constants are grouped under subclass and class which are identified with a line of text in the format: [Subclass(Class)].

These files can be generated automatically at programmed intervals using the AutoExport feature. Use the Options menu to set the interval and the file name. Then, start the feature with the AutoExport menu command. At each programmed interval, a new .gg file is written, with an index number appended to the file name. This feature is useful for tracking data flash values that may change over time, such as the resistance values for each cell in the Ra Table.

Importing and Writing All

The .gg file can be saved and then imported into another device. Use the File | Import menu to select a .gg file. Doing this brings the data into the data flash grids, where it can be reviewed and edited. To transfer all the data into the bq20z70/90 gas gauge, push the Write All button.

5.5 Calibrating the bq20z70/90

The calibration screen provides a flexible platform for device calibration of offsets, voltage, current, and temperature. The common calibration functions and an optional pack voltage calibration function are available.

CC Offset Calibration

The coulomb current offset calibration is a prerequisite for voltage, temperature, and current gain calibrations, because a gain calibration with an offset present is not accurate. By default, this is a quick version of the offset calibration. A full calibration occurs each time the bq20z70/90 enters sleep mode. Although the various gain calibrations may be performed independently, the CC offset calibration must be performed at least once prior to use in order to correct for any CC offset error.

Voltage and Temperature Calibration

Enter the known value of voltage and temperature. Select the number of cells in the application. Select the type of temperature sensors used in the application.

Current Calibration

Enter the applied current, which should be approximately 2 A.

Pack Voltage Calibration

Pack voltage calibration is not generally necessary. This is used to calibrate a separate measurement path, which only detects if a charger is present.

Board Offset Calibration

Board offset calibration must be performed with the ICs powered only from the cells with no load current or charger connected.

5.6 The Pro Screen

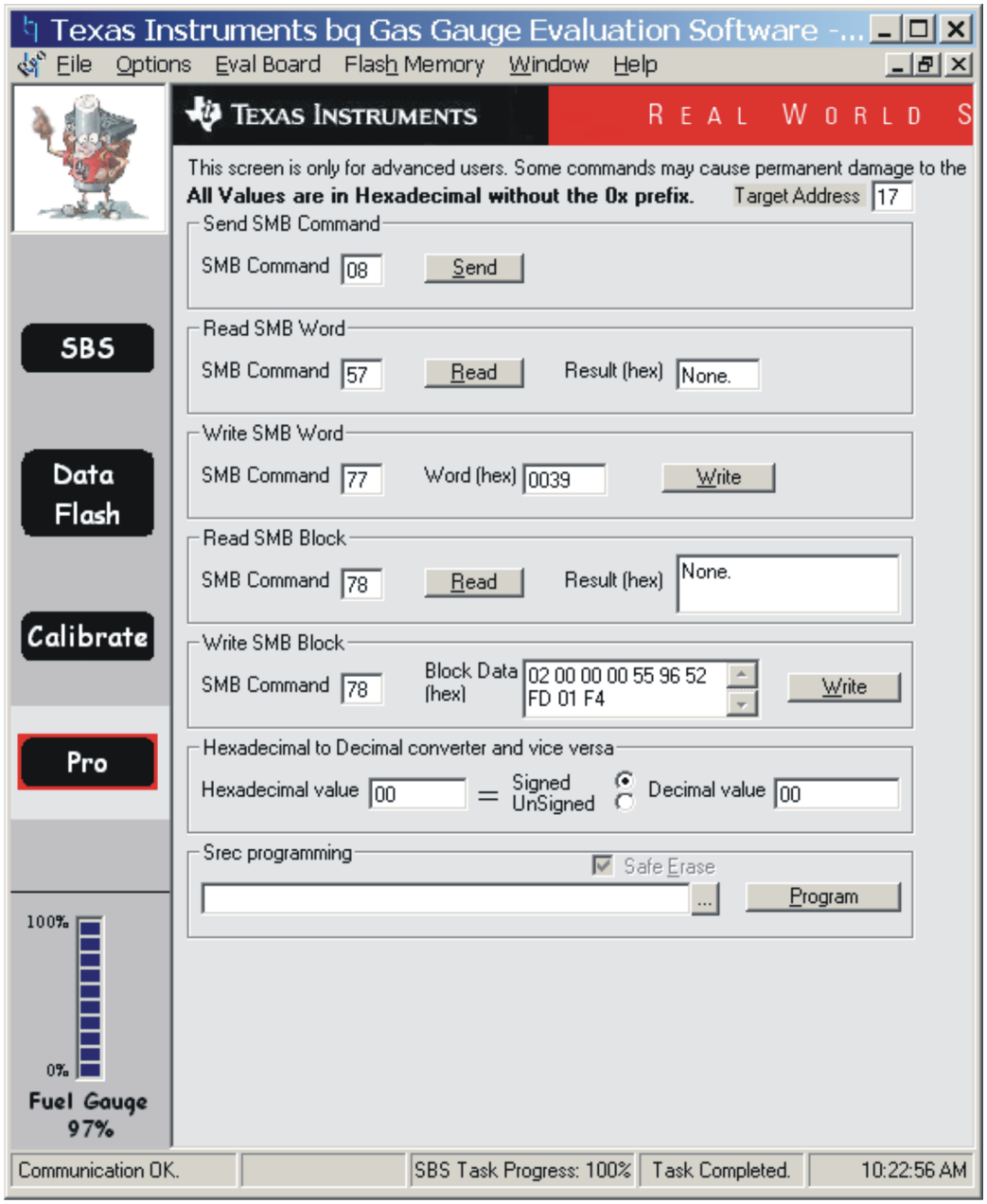


Figure 11. Pro Screen

The Pro screen can be used to read and write low-level SMBus command, word, and block transactions(see Figure 11). There is also the ability to reprogram the bq20z70/90 flash memory. The write operations should not be done without understanding the implications.

SMB Commands, Words, and Blocks

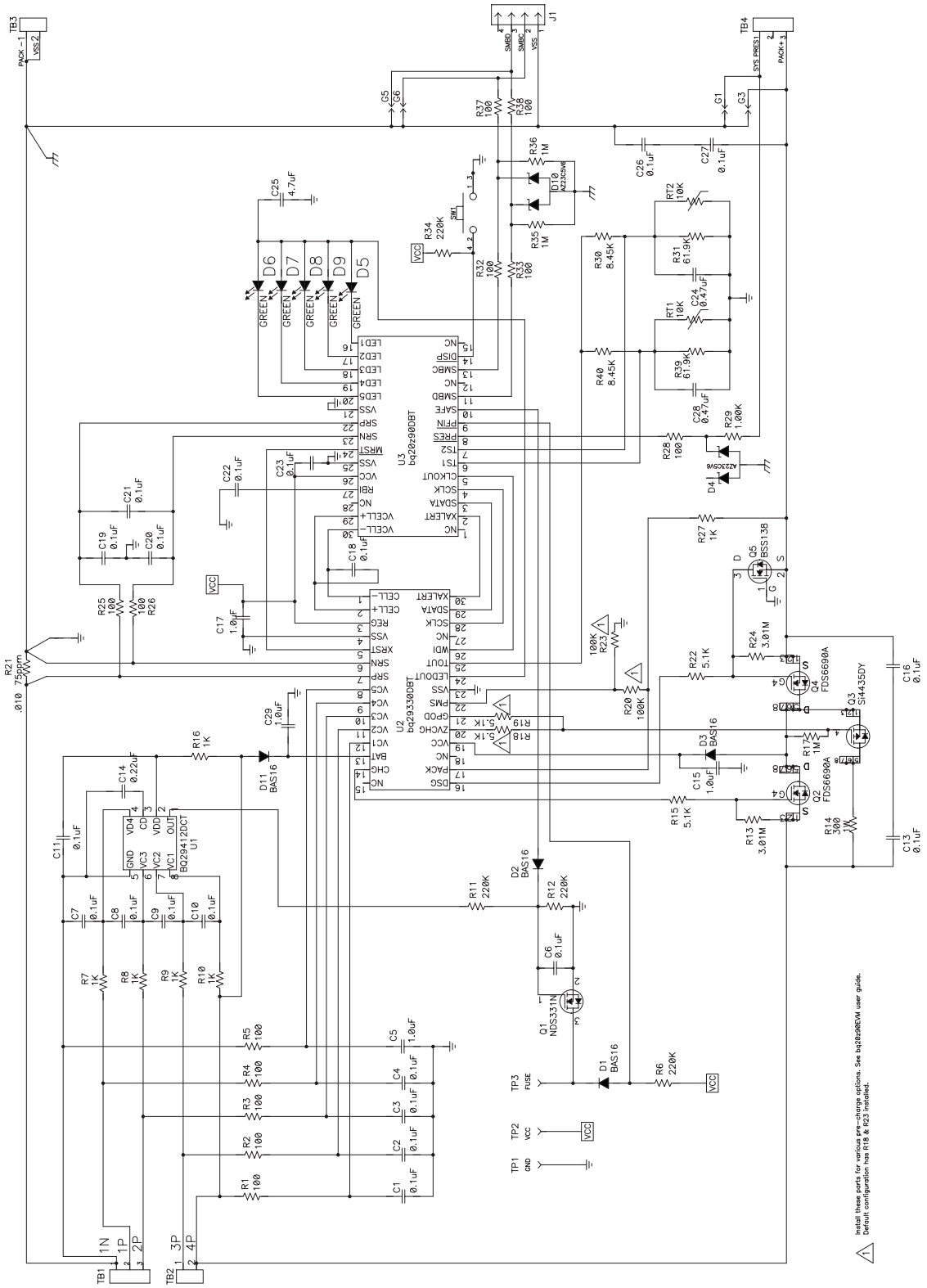
SMBus commands, words, and blocks can be easily read or written on the Pro screen. The most common use of this facility is to send 0x0021 to SMB command 0x00 (Manufacturer Access) in order to start the Impedance Track™ algorithm.

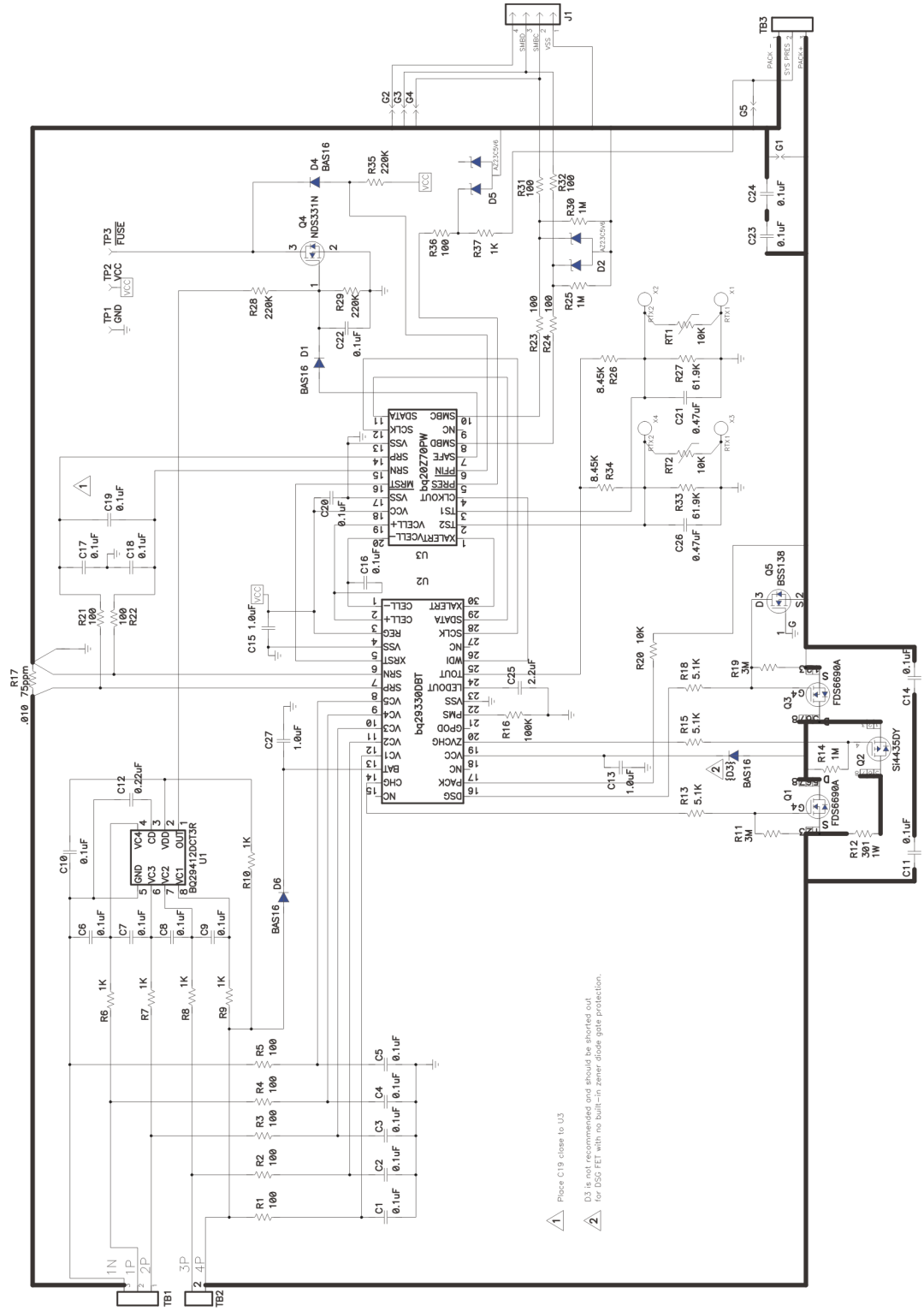
SREC Programming

Programming or *Re-flashing* the bq20z70/90 is also an advanced topic, which can be useful in certain circumstances. The object files used to program the device have the extension *.senc* which refers to an encrypted s-record.

5.7 EVM Schematic

The schematics for the HPA059 and the HPA155 follow.




J1
TB3
G1
G2
G3
G4
G5
C24 0.1uF
C23 0.1uF
D4 BAS16
R35 220K
Q4 NDS331N
TP3 FUSE
TP2 VCC
TP1 GND
R28 220K
R29 220K
C22 0.1uF
D1 BAS16
R36 100
R37 1K
D5
R31 100
R32 100
R30 1M
D2
R23 100
R24 100
R25 1M
RT1 10K
R27 61.9K
R26 8.45K
C21 0.47uF
RT2 10K
R33 61.9K
R34 8.45K
C26 0.47uF
U3 bq20Z70PW
U2 bq29330DBT
C19 0.1uF
C17 0.1uF
C18 0.1uF
C20 0.1uF
C16 0.1uF
C15 1.0uF
R21 100
R22 100
R17 75ppm .010
Q5 BSS138
D3
R20 10K
R18 5.1K
R19 3M
R15 5.1K
R16 100K
C25 2.2uF
C27 1.0uF
C13 1.0uF
R13 5.1K
R14 1M
Q2 Si4435DY
Q3 FDS6690A
Q1 FDS6690A
R11 3M
R12 301 1W
C14 0.1uF
C11 0.1uF
C12 0.22uF
U1 BQ29412DCT3R
C10 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
R10 1K
D6 BAS16
R6 1K
R7 1K
R8 1K
R9 1K
R5 100
R4 100
R3 100
R2 100
R1 100
C5 0.1uF
C4 0.1uF
C3 0.1uF
C2 0.1uF
C1 0.1uF
TB1
TB2
1N
1P
2P
3P
4P
1 Place C19 close to U3
2 D3 is not recommended and should be shorted out for DSG FET with no built-in zener diode gate protection.

Theory and Implementation of Impedance Track™ Battery Fuel-Gauging Algorithm in bq20zxx Product Family

PMP Portable Power

ABSTRACT

In fuel gauge solutions, current integration and voltage correlation algorithms suffer from a decrease in accuracy with battery aging and also require extensive data collection. This application report outlines the theory of Impedance Track™ (IT) technology that overcomes these problems. Implementing the IT algorithm in the Texas Instruments bq20z8x family is reviewed and setting the data flash constants associated with the fuel-gauging algorithm is described in detail.

6.1 Summary of the Algorithm Operation

The Impedance Track™ gas gauge algorithm(1) uses three types of information to calculate remaining capacity (*SBS.RemainingCapacity( )*) and full charge capacity (*SBS.FullChargeCapacity( )*).

1. Chemical: depth of discharge (DOD), and total chemical capacity Q_{max}
2. Electrical: internal battery resistance dependence on DOD
3. External: load, temperature

SBS.FullChargeCapacity( ) is defined as the amount of charge passed from a fully charged state until the voltage defined in *DF:Terminate Voltage* flash constant is reached at a given rate of discharge, after subtracting the reserve capacity (*DF:Reserve Capacity*).

Note that it depends on the rate of discharge and is lower at higher rates and low temperatures because the cell I x R drop causes the Terminate Voltage threshold to be reached earlier.

(1) Impedance Track algorithm is protected by US Patents US6832171, US6789026, and US6892148.

6.2 Detailed Description of Parameters Updated by the Gas Gauge Algorithm

Modes of Algorithm Operation

The algorithm differentiates between *charge*, *discharge*, and *relaxation* modes of operation. During *charge* mode, the SBS.OperationStatus( ) [DSG] bit is cleared, and during *discharge* and *relaxation* mode, it is set. Entry and exit of each mode is controlled by Data Flash (DF) parameters in the subclass Gas Gauging: Current Thresholds section as illustrated in Figure 12. Charge mode is exited, relaxation mode is entered when *SBS.Current( )* goes below *DF:Quit Current* and after a *DF:Chg Relax Time* period. Discharge mode is entered when *SBS.Current( )* goes below *DF:Dsg Current Threshold*. Discharge mode is exited, relaxation mode is entered when *SBS.Current( )* goes above *—DF:Quit Current* threshold and after a *DF:Dsg Relax Time* period. Charge mode is entered when *SBS.Current( )* goes above *DF:Chg Current Threshold*.

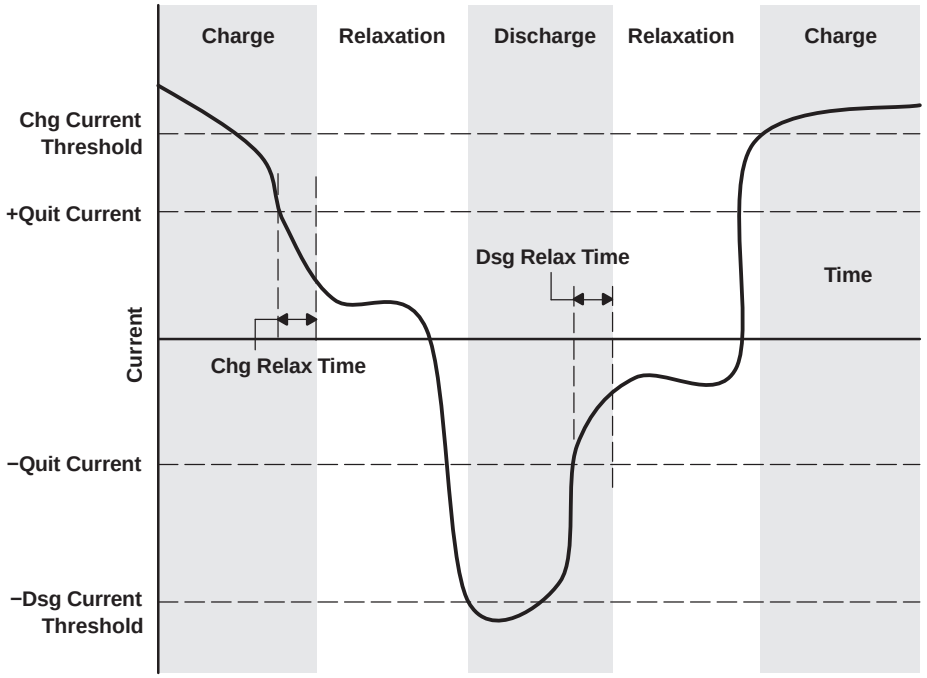


Figure 12. Example of the Algorithm Operation Mode Changes With Varying *SBS.Current( )*

Update of Chemical Depth of Discharge (DOD)

The gas gauge updates information on the chemical depth of discharge (DOD_0) based on open-circuit voltage (OCV) readings when in a relaxed state. This is done for each cell separately. DOD is found by correlating DOD with OCV using a predefined table DOD(OCV,T) stored as reserved data flash parameters. The table is specific for a particular chemistry such as $LiCoO_2$/carbon (default settings), $LiMn_2O_4$/carbon, etc., and can be identified by reading the chemistry ID through sending SBS.ManufacturerAccess( ) command 0008, then reading SBS.ManufacturerAccess().The gas gauge can be set up for a particular chemistry by using the relevant firmware file (*.senc) that can be downloaded from the bq20zXX production folder on power.ti.com. See *Support of Multiple Chemistries* (SLUA384) for more details.

Figure 13 shows the timing of parameter updates during the relaxation mode. First, OCV readings and DOD_0 calculations are taken after a 30-minute relaxation period has passed. Then, OCV readings continue to be taken every 100 seconds. DOD is calculated based on each measured OCV reading using the linear interpolation DOD = f(OCV,T). Integrated PassedCharge is set to zero at each DOD_0 update.

If the current during the OCV reading is non-zero, then an IR correction is done. The first iteration of DOD is found from the uncorrected OCV reading; then the resistance value is found from the R(DOD) table and used to correct the OCV value as OCV′= OCV - I x R. Then, the corrected DOD is found from OCV′. This method achieves the best accuracy if the current during relaxation mode is below the C/20 rate. This is why it is recommended that the DF.Quit Current not exceed C/20.

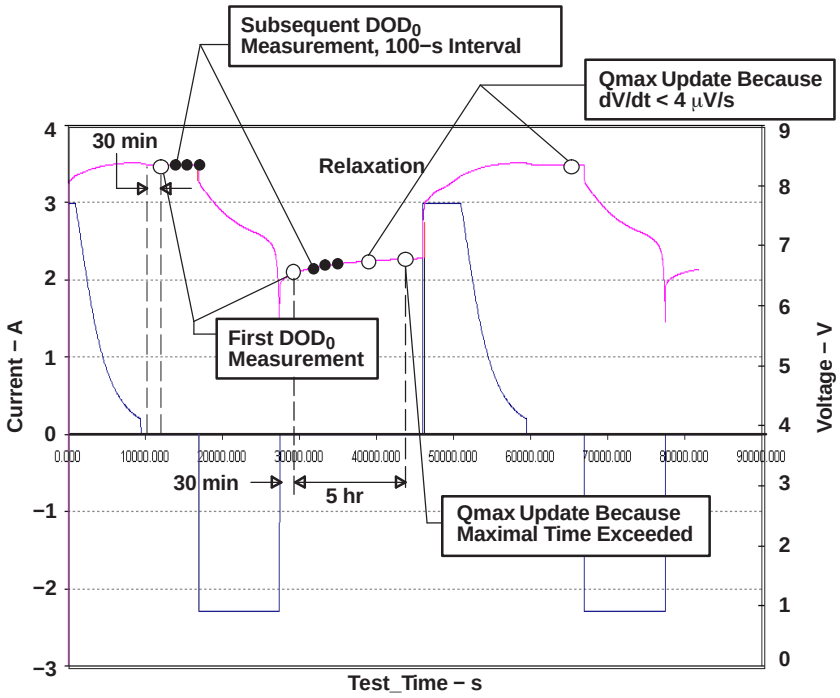


Figure 13. Timing of DOD_0 and Qmax Updates During Relaxation Mode

If no DOD_0 has been measured until the relaxation state is exited, the previous DOD_0 is used along with the PassedCharge integrated since the last DOD reading.

During charge and discharge modes, the *present* DOD is recalculated every second as DOD = DOD_0 + PassedCharge/Qmax. DOD is used for determining when a resistance update needs to occur, as well as the starting point for a Remaining Capacity (and FCC) calculation. Remaining capacity calculations occur immediately after discharge onset, at every resistance update, and after entering relaxation mode.

Update of Qmax

Maximal chemical capacity Q_{max} for each serial cell is stored in Data Flash as *DF:QmaxX*, where X=0, 1, 2, or 3, the cell serial number.

The GG updates Q_{max} based on two DOD readings made before and after charge or discharge, for each serial cell separately. For example, DOD_1 is taken during relaxation, then discharge mode starts, and PassedCharge is integrated. Following this, another relaxation mode is entered, and DOD_2 is taken.

DOD1 and DOD2 are calculated from OCV readings in a well-relaxed state, as exemplified in Figure 13. A well-relaxed state is detected if dV/dt < 4 μV/s or maximal waiting time of 5 hours is exceeded. The first condition is satisfied in typical batteries after about 1 hour if DOD is between 0% and 80%, and 3–4 hours if DOD is above 80%. At a low temperature, relaxation takes a longer time.

In order to ensure high accuracy of DOD measurement, Qmax calculation do not occur if the temperature is above 40°C or below 10°C. It also does not occur if at least one of voltage measurements for DOD_1 or DOD_2 was taken in the cell voltage range between 3737 mV and 3800 mV because of flat OCV(DOD) dependence in this range. These limits are chemistry dependent and will be specified separately for different chemistries.

Qmax is calculated as Qmax = PassedCharge / (DOD_2– DOD_1).

The data flash constant *DF.Update Status* increments by 1 when the first Qmax update takes place (e.g., from 4 to 5 if no resistance updates were made, or from 5 to 6 if a resistance update was made). *SBS.Max Error( )* becomes 5% in the first case and 1% in the second case

PassedCharge has to be more than 37% of *DF:Design Capacity* for an update to occur. For the first cycle (with *DF:Update Status* = 4), 90% of *DF:Design Capacity* is required because this cycle takes place in the factory settings and Qmax is learned for the first time.

In order to prevent Qmax fluctuations, a first-order smoothing filter is applied to all Qmax readings except in the first cycle. Readings with lower PassedCharge are assigned lower weights in the smoothing.

Update of Resistance

Resistance is updated during discharge, as summarized in Figure 14. The first resistance update happens after 500 seconds, to prevent distortion from transients after load onset.

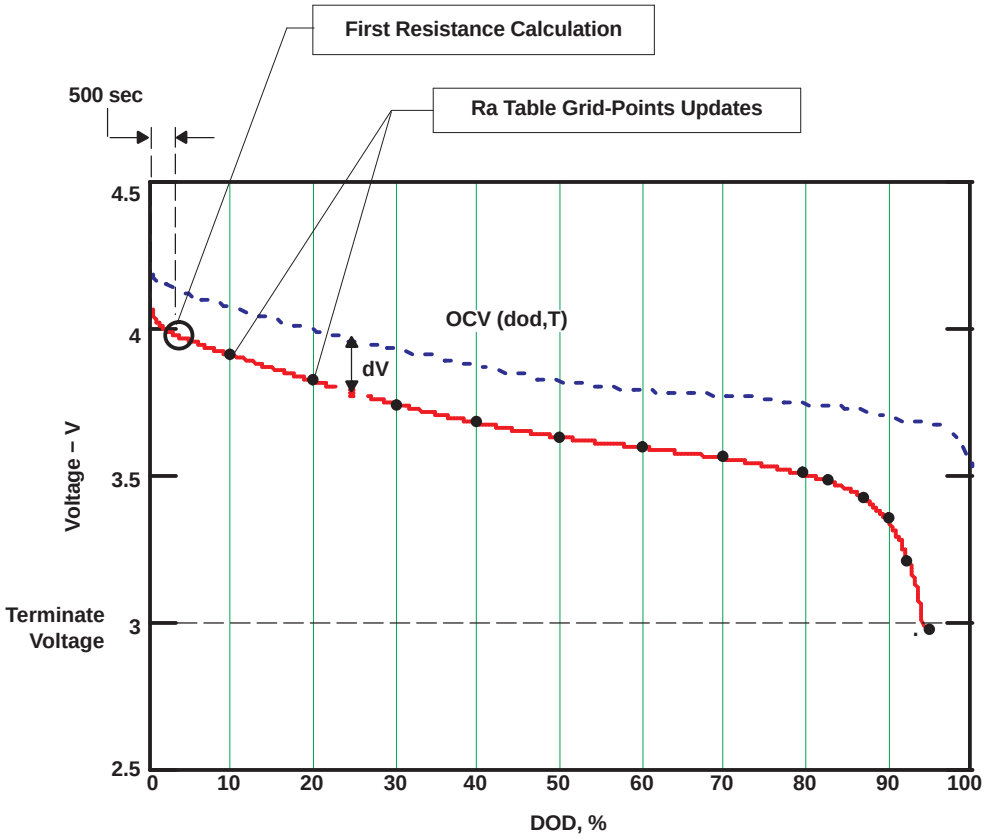


Figure 14. Impedance Updates

Calculation is performed by comparing the measured voltage with the OCV value at the same DOD, that is taken from the OCV(DOD,T) table:

dV = V – OCV(DOD,T)

R(DOD) = dV/I

Resistance measurements are taken continuously and stored in RAM.

Resistance is updated in the Data Flash (in *DF:Ra Table*) after each 11.1% of DOD charge (1/9th increment) is exceeded (DOD charge is PassedCharge/Qmax). When DOD reaches 77.7%, resistance is updated after each 3.2%. The final resistance update is made after discharge is terminated.

The constant *DF.Update Status* increments by 1 when the first grid-point resistance update takes place (e.g., from 4 to 5 if no Qmax updates were made before, or from 5 to 6 if Qmax updates were made before).

Before storage to Data Flash, resistance values are normalized to 0°C as Ra[dod] = R[dod]/exp(Rb[dod] x T) where R is the measured resistance value at a given DOD, Rb[DOD] is the value of temperature coefficient of impedance change at a given DOD stored as a reserved data-flash table, and T is temperature in °C. Note that values of resistance normalized to 0°C are somewhat larger than values at room temperature and so cannot be directly compared with R=dV/I values.

Resistance values for the grid points with a higher DOD than presently updated are scaled by the same factor as the present grid-point change, e.g., by factor Ra_new/Ra_old. In this way, faster convergence of the resistance profile is achieved.

Values in *DF.Ra Table* are stored in mΩ units, in the format CellX Ra N where X is a cell serial number from 0 to 3, and N is grid-point number from 0 to 14 that corresponds to 11.1% increments of DOD until 77.7%, and then 3.2% increments of DOD. The CellX flag and xCellX flag are used for interchanging the data-flash column usage for reducing the number of DF writes. A flag value of 55 indicates the presently used data column; 00 indicates the presently unused data column.

If during resistance update, the DOD exceeds 100%, or resistance appears negative, which are both indications of a too-small DF.QmaxX initial guess, DF.QmaxX increments by 10% and all resistances are recalculated. This is normal behavior during the first *learning* cycle. However, if the initial guess of DF.QmaxX was too far from the correct value, the second cycle might be needed to achieve full resistance accuracy. To avoid this, set DF.QmaxX to a value specified by the cell manufacturer, multiplied by the number of parallel cells.

Update of Temperature Model

Because temperature changes significantly during the course of a discharge, the algorithm needs to be able to predict the future temperature. This is needed for temperature correction of battery impedance R = Ra x exp(Rb x T)) during voltage simulation near the end of a discharge. To achieve this, the algorithm collects T(t)-dependence data during discharge. It is used to update parameters of a simple thermal model including a heat exchange coefficient and a thermal time constant. These parameters are updated at the same time as resistances. The algorithm also records the outside temperature (T_out) during relaxation periods. These parameters are used to define a function T(t, T_start) that calculates a temperature profile starting from present temperature, T_start, and continuing until the end of discharge.

Update of Remaining Capacity (RM) and Full Charge Capacity (FCC)

Update of RM and FCC takes place after each resistance grid-point update, at the end of discharge, and at the exit of relaxation mode.

FCC consists of 3 parts:

$$SBS.FullChargeCapacity( ) = Q_{start} + PassedCharge + RM$$

Components of FCC are indicated in an example in Figure 15.

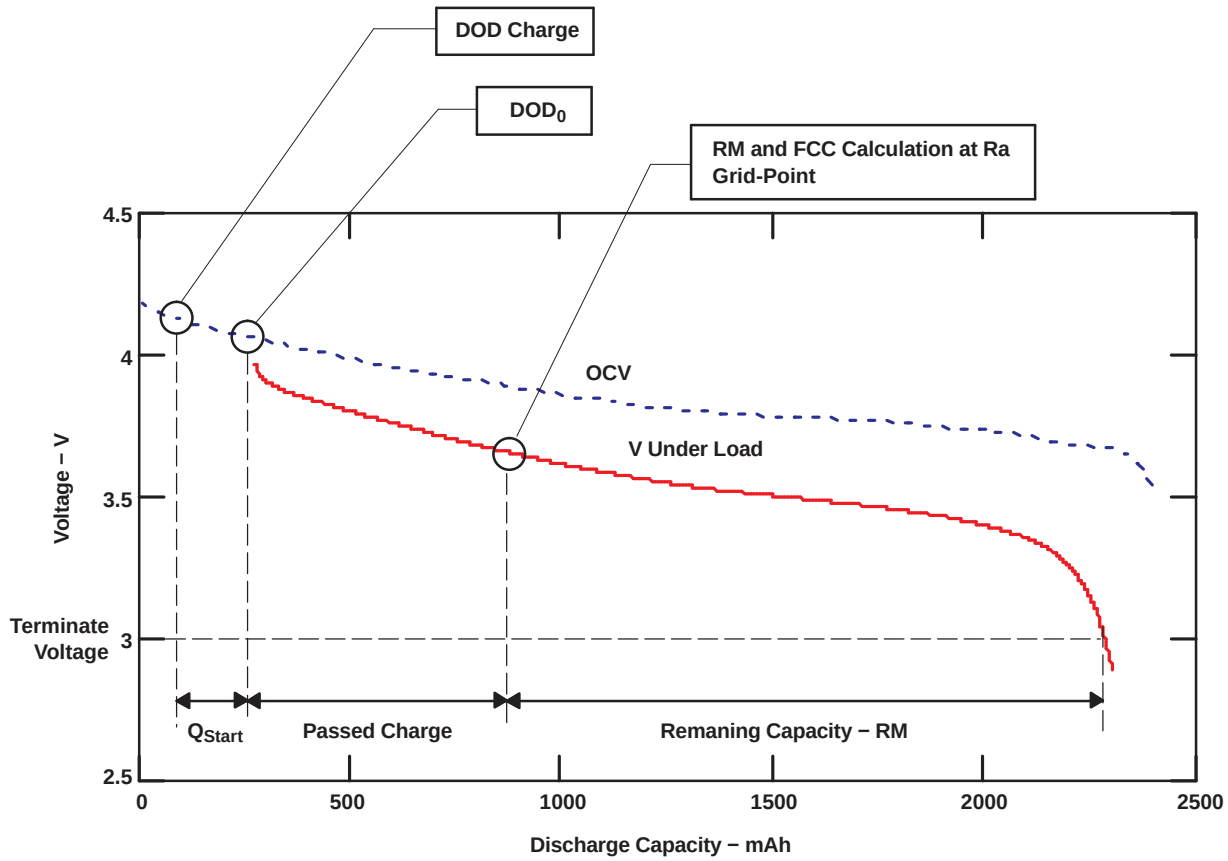


Figure 15. Components of SBS.FullChargeCapacity( ) Value

1. Q_{start} is the charge that would have passed to make DOD = DOD_0 from a fully charged state (DODcharge). For a fully charged battery, Q_{start}= 0. Q_{start} is recalculated at the exit of the relaxation mode. In the case of constant current, it is simply $Q_{start} = Q_{max} \times$ (DOD0 – DODcharge), but for the constant power case a voltage simulation is run. DODcharge is assigned equal to DOD_0 at first DOD_0 update, after charge termination by taper current. Note that DODcharge is somewhat higher than 0 because chargers typically do not charge a battery to full.
2. PassedCharge is the coulomb count integrated during the present discharge or charge, and set to zero at every DOD_0 update.
3. Remaining capacity is calculated after each resistance grid-point update and at the end of discharge.

SBS.RemainingCapacity( ) (RM) is calculated using a voltage simulation. The GG starts a simulation at the present DODstart = DOD_0 + PassedCharge/Qmax and continue calculating voltage V(DODx,T) = OCV(DODx,T) + I x R(DODx,T) by incrementing DOD with dDOD increment of 4%. DOD[i]=DODstart + dDOD x I. This incrementing is continued until the simulated voltage V(DOD[i]) becomes less than *DF.Terminate Voltage*. Once that happens, the final DOD *SBS.RemainingCapacity( )* = (DODfin-DODstart) x Q_{max} is detected. Note that Q_{max} for the lowest capacity cell is used.

Current that is used in the simulation is the average current during the present discharge (several types of averaging can be selected using *DF:Load Select* data flash constant). A simulation can run in constant current mode (*DF:Load Mode* = 0) or constant power mode (*DF:Load Mode* = 1).

Update of SBS.Remaining Capacity( ) and SBS.RemainingStateOfCharge( ) Values

Although *SBS.FullChargeCapacity( )* is only updated at a few points during a discharge as previously described, the *SBS.RemainingCapacity( )* is updated continuously (every 1 second) based on the integrated charge. *SBS.RemainingCapacity( )* = RM – Q_integrated where Q_integrated is charge passed since the last RM calculation. The value of *SBS.RemainingCapacity( )* is also used to update *SBS.RelativeStateOfCharge( )* every second as *SBS.RelativeStateOfCharge( )* = *SBS.RemainingCapacity( )* x 100/*SBS.FullChargeCapacity( )*.

The same value is used to calculate the run-time to empty as *SBS.RunTimeToEmpty( )* = *SBS.RemainingCapacity( )* / *SBS.AverageCurrent( )*.

Note that even if a simulation of RM is run in constant power mode (*DF:Load Mode* = 1), the reporting of *SBS.RemainingCapacity( )* and *SBS.RemainingRunTime( )* can be done either based on mAh or in 10mWh values. The mAh or mWh reporting depends on the setting of *SBS.BatteryMode( ) [CAPACITY_MODE]* bit (0=mAh, 1=10mWh). In case of a second setting, the run-time-to-empty is calculated as SBS.RunTimeToEmpty( ) = SBS.RemainingEnergy( ) / SBS.AveragePower( ) and is generally more accurate for most devices because of increased power consumption at low voltages.

Update of SBS.Max Error()

SBS.Max Error() is an estimate of maximal error of SBS.RSOC. Initially, it is set to 100% because the fuel gauge has no information about the battery. After Qmax is learned, or resistance is learned (as indicated by DF.Update Status = 5), SBS.Max Error changes to 5%. After the second part of the database (resistance or Qmax) is learned (Update Status = 6), SBS.Max Error changes to 1%. SBS.Max Error( ) is increased to reflect the number of cycles since the last Qmax. This is achieved by storing the cycle number when Qmax was last updated in an internal variable Qmax_cycle. SBS.Max Error is then calculated as Max Error + (SBS.Cycle Count() – Qmax_cycle) x 0.05. This means that SBS.Max Error increases by 1% in 20 cycles, e.g., only occasionally is a Qmax update needed to maintain high accuracy.

bq20zxx EVM Data Flash Settings for Number of Serial Cells and Pack Capacity

PMP Portable Power

ABSTRACT

This application report describes the configuration changes in the data flash constants in the Texas Instruments bq20z80 Gas Gauging Evaluation Software required for a variety of battery-pack configurations.

The factors affecting the settings include the number of cells in series and the pack capacity. The pack capacity is determined by the cell capacity and the number of cells are in parallel.

Configurations are described (for example) as 3s2p, which stands for 3 cells in series and 2 in parallel. All changes must be done before enabling the Impedance Track™ feature in the bq20z80.

Section 1 describes the changes required when changing series-cell count, and Section 2 explains settings for varying the pack capacity. Illustrations are provided showing the specific locations in the data flash screens of the evaluation software.

7.1 Changes to Default 4-Series Cell Configuration

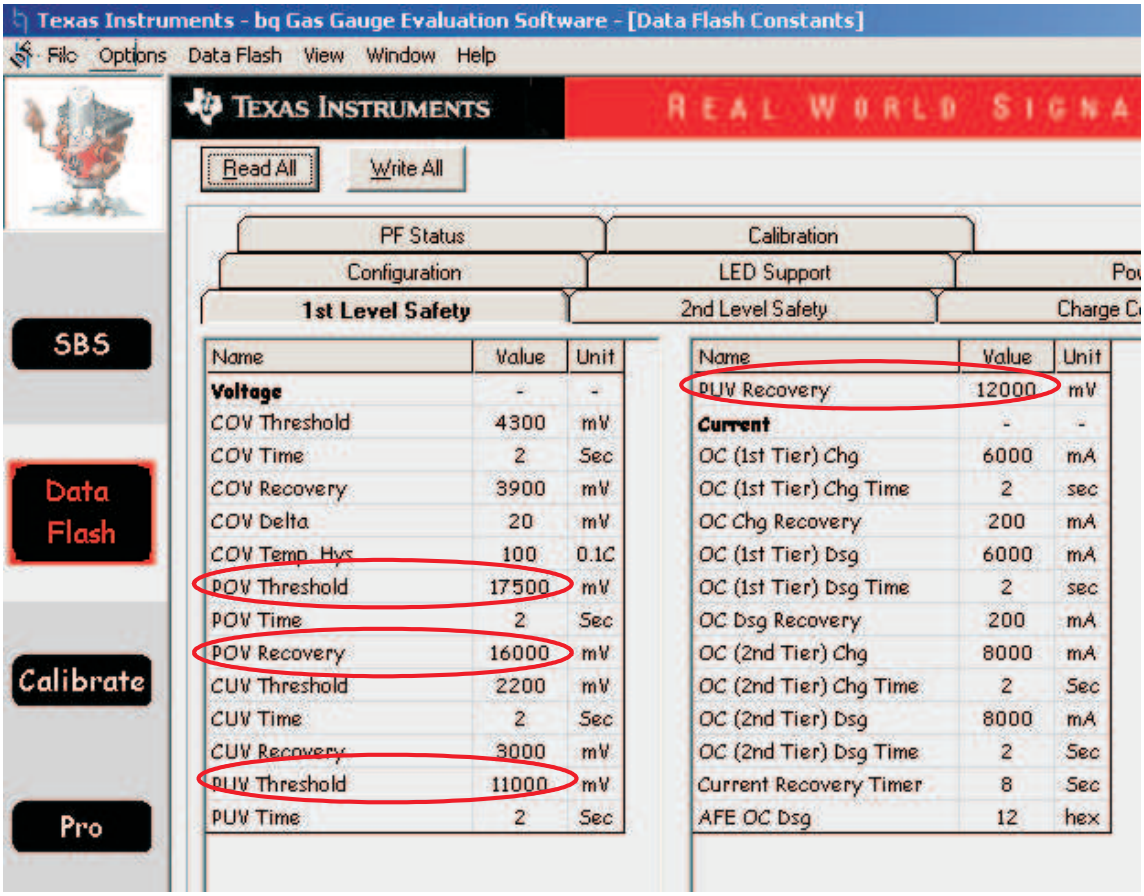
The following changes from the default settings must be made to enable a 2-series or 3-series cell pack before enabling the Impedance Track™ feature in the EVM. If a 4-series cell pack is connected, the EVM can be used in the default setting.

In addition to the serial configuration, the design capacity of the cells must be considered. This information is found on the cell-manufacturer data sheet and must be set in the data flash. This is described in Section 2 of this application note.

Table 31. First Level Safety

Setting[1]	2-Cell	3-Cell	4-Cell (Default)
POV Threshold	8700	13000	17500
POV Recovery	8400	12600	16000
PUV Threshold	5400	8100	11000
PUV Recovery	5700	8500	12000

(1) This section does not apply to bq20z70.



This and other illustrations contain some parameters that are absent in the bq20z70.

Table 32. Second Level Safety

Setting	2-Cell	3-Cell	4-Cell (Default)
SOV Threshold	9000	13500	18000

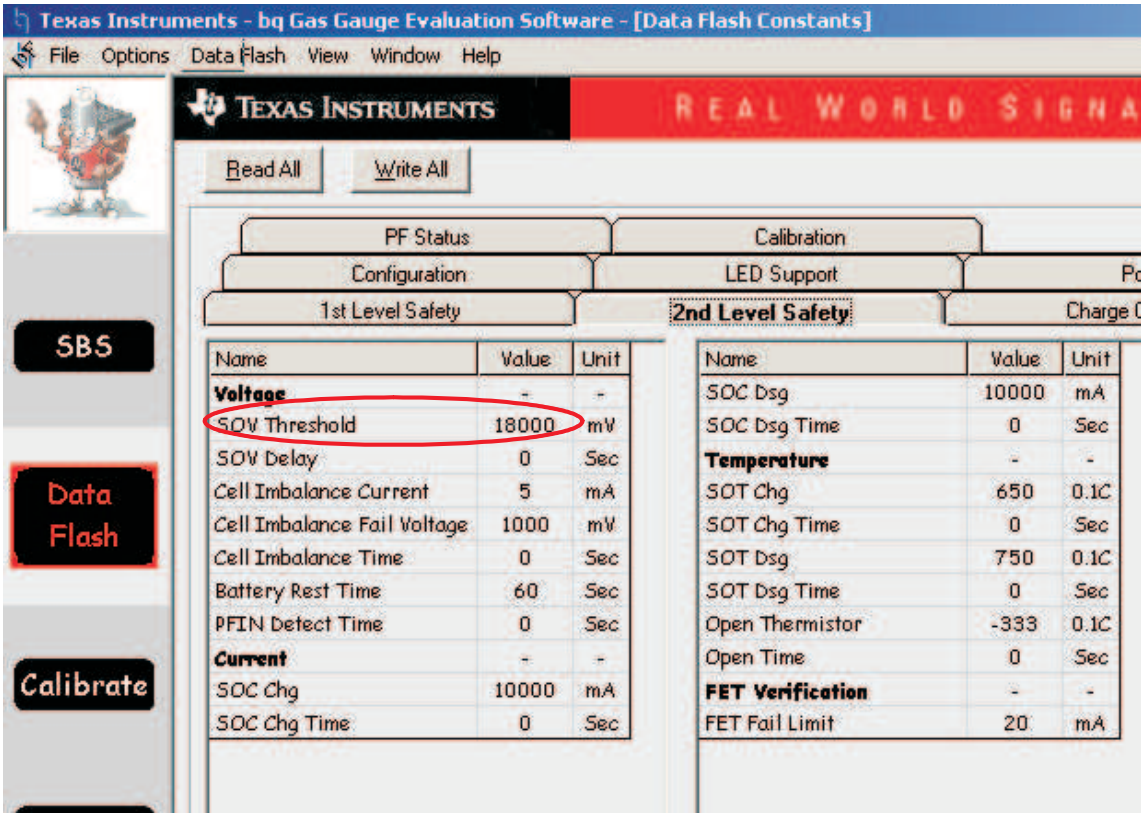


Table 33. Charge Control

Setting	2-Cell	3-Cell	4-Cell (Default)
Charging voltage	8400	12600	16800
Depleted voltage	5000	8000	11000
Deepleted recovery	5500	8500	11500

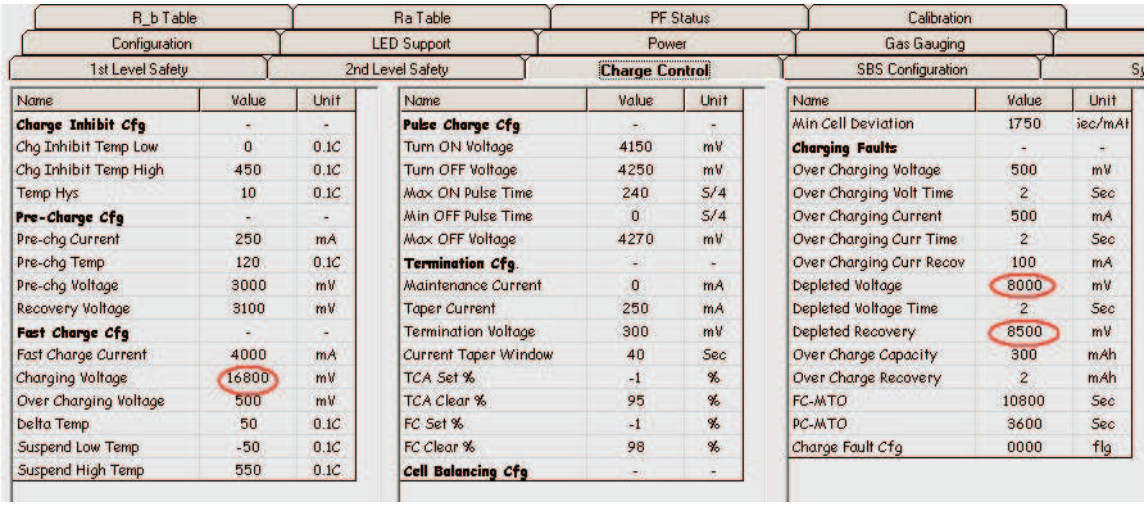


Table 34. SBS Configuration

Setting	2-Cell	3-Cell	4-Cell (Default)
Design voltage	7200	10800	14400

Also see the description of the Design Energy setting in Section 2.

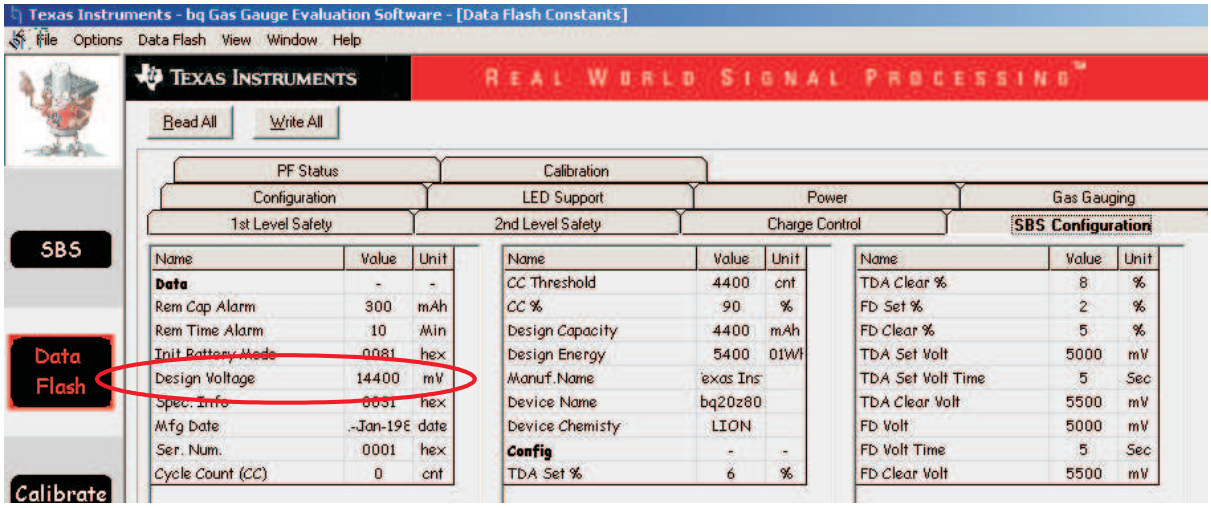


Table 35. Typical Configuration Settings for bq20z80 and bq20z90

Setting	2-Cell	3-Cell	4-Cell (Default)
Operation CfgA	2d29	2e29	2f29
CC1	0	1	1
CC0	1	0	1

Number of serial cells is defined in CC1 and CC0 bits in Operation CfgA, bit mask 0x0300.

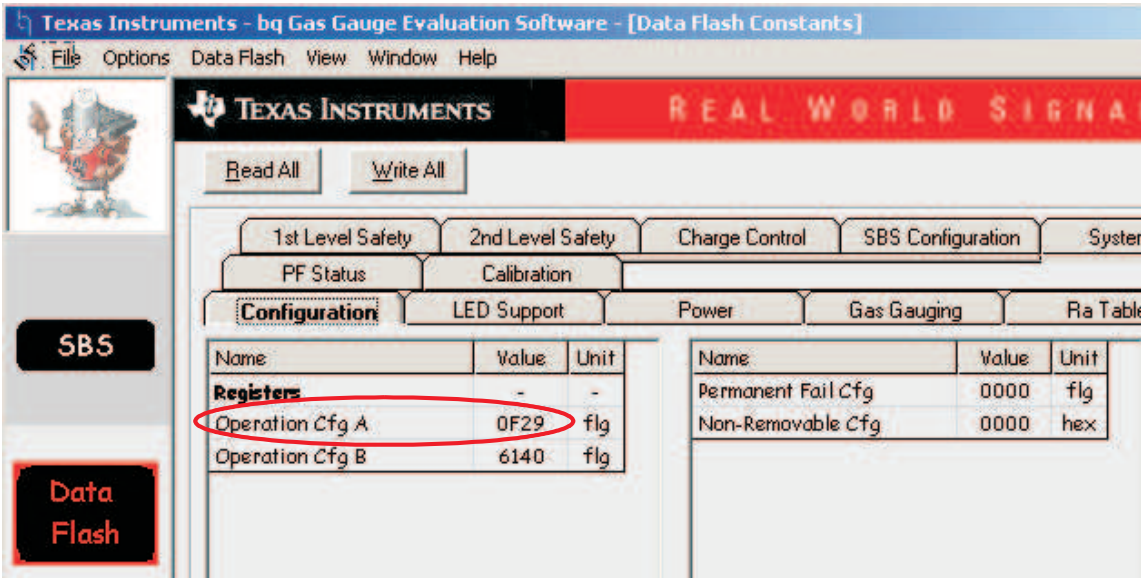


Table 36. Typical Configuration Settings for bq20z70

Setting	2-Cell	3-Cell	4-Cell (Default)
Operation CfgA	0129	0229	0329

Table 37. Power

Setting	2-Cell	3-Cell	4-Cell (Default)
Flash Update OK Voltage	6000	7500	7500
Charger Present Threshold	3000	3000	3000
Shut Down Voltage	5000	7000	7000

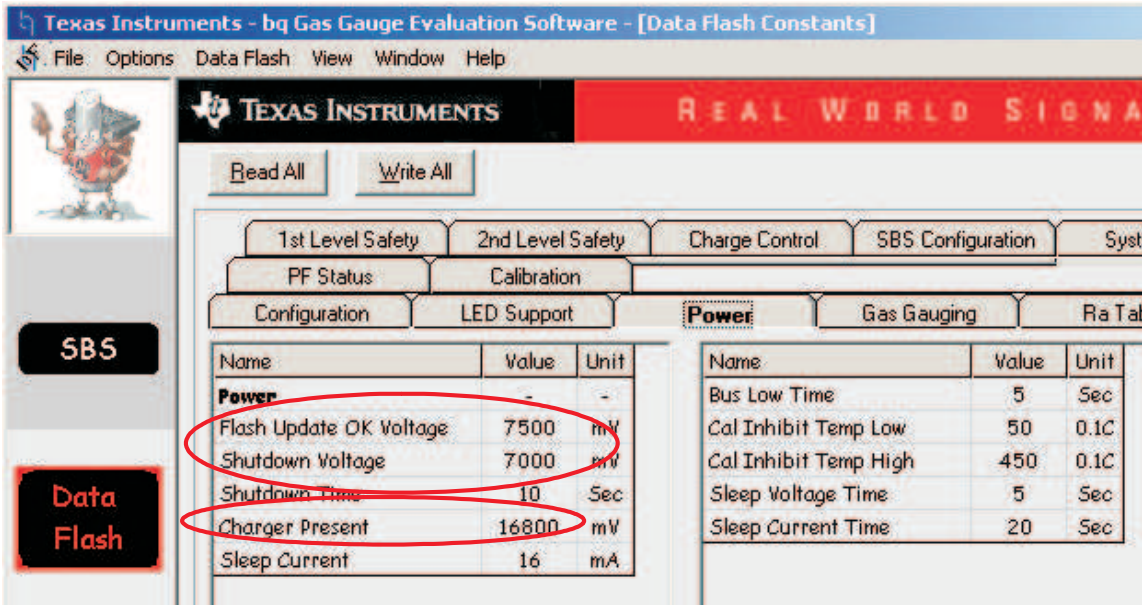
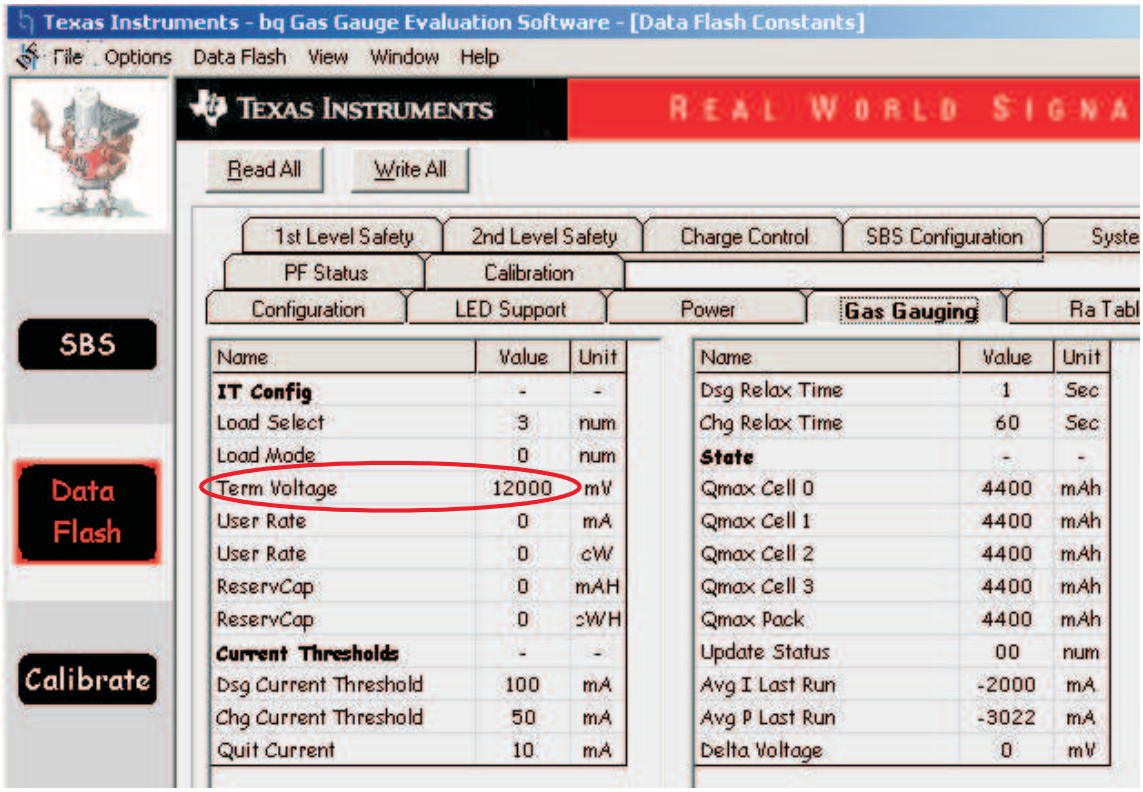


Table 38. Gas Gauging

Setting	2-Cell	3-Cell	4-Cell (Default)
Term Voltage	6000	9000	12000



7.2 Changes to Capacity Settings

The pack capacity depends on the individual cell capacity and on the number of parallel cells. The cell-capacity value found in the cell-manufacturer data sheet is used only as an initial estimate for the gas-gauging algorithm, and is updated during operation.

Gas Gauging

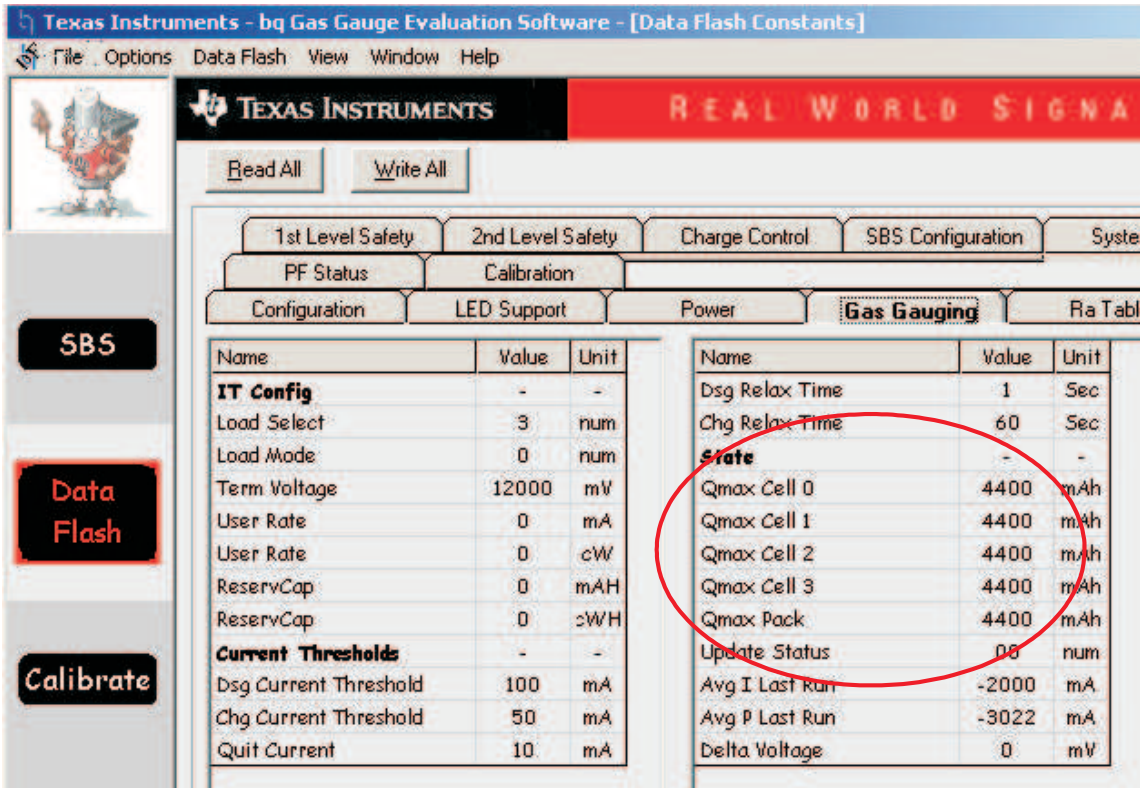
The Qmax of all serial cells (Qmax Cell 0 to 3) is set initially to equal values. The same value is assigned to Qmax Pack. The value to be assigned is calculated as

Qmax = Data sheet Cell Capacity × Number_parallel_cells.

Example: The default assumes 2200-mAh cells Following are the required changes to the 4s2p default values if 2400-mAh cells are actually used..

Table 39. Gas Gauging

Setting	1p with 2400 mAh	2p with 2200 mAH (Default)	3p with 2400 mAH
Qmax Cell 0	2400	4400	7200
Qmax Cell 1	2400	4400	7200
Qmax Cell 2	2400	4400	7200
Qmax Cell 3	2400	4400	7200
Qmax Pack	2400	4400	7200



SBS Configuration

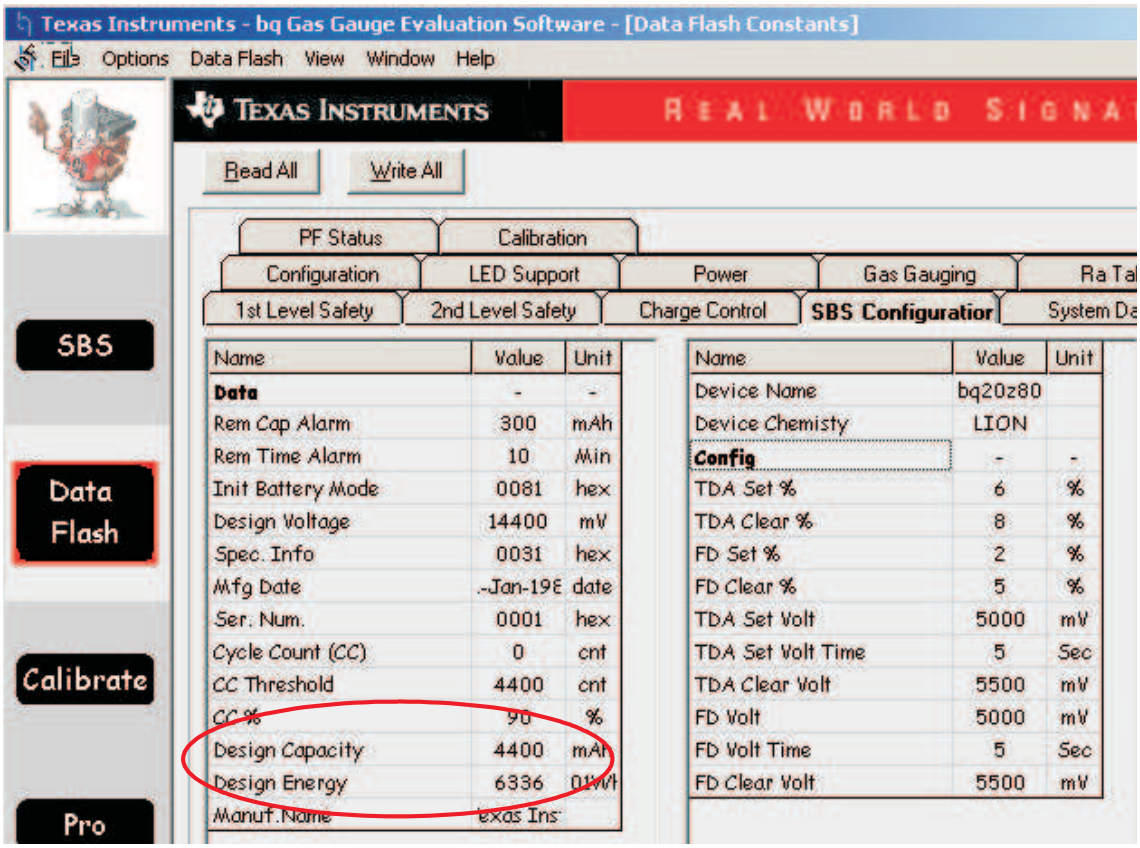
Design Capacity is set to the same number as Qmax or lower. Design energy (centi-Watt) is calculated as

Design Energy = Design Capacity × Number_Serial_Cells × 3.6 V ÷ 10

Example: The default assumes 2200-mAh cells. Following are the required changes to the 4s2p default if 2400-mAh cells are actually used.

Table 40. Gas Gauging

Setting	1p with 2400 mAh	2p with 2200 mAH (Default)	3p with 2400 mAH
Design Capacity	2400	4400	7200
Design Energy	3456	6336	10368



Design Capacity is used to calculate the amount of discharge that is sufficient for a Qmax update. Therefore, it should be set to less than or equal to Qmax. Design Energy is not used in the gas-gauging algorithm, except for reporting absolute state of charge (ASOC) and state of health; so, it does not influence gas-gauging accuracy. Actual capacity depends on the rate of discharge. If a more-accurate setting of design capacity and energy is desired, it should be measured at a discharge rate typical for the target application. The learned FCC value from gas-gauging of a new battery pack at a typical rate can be used as a good estimate of design capacity.

Data Flash Programming Using the EV Software

This document applies to users that require a small quantity of battery packs for evaluation. For mass production methods, see *Using the BQTester Software* (SLUA352) and *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* (SLUA355).

Values of data-flash parameters are determined based on bq20z80 data sheet (SLUS625). In most cases, the default settings are sufficient, while the most commonly changed values are described in *bq20z80 EVM Data Flash Settings for Num of Serial Cells/Pack Cap* (SLVA208).

8.1 Manually changing a value of data-flash constant

1. Apply voltage of about 16 V between Pack+ and Pack- pins to power up the PCB.
2. Connect the EV2300 board, and start the EV Software.
3. Go to the "Data flash" screen.
4. Find the class containing the required data-flash parameter, for example "1st Level Safety".
5. Find the required parameter in the class, for example “POV Threshold”.
6. Type the new value directly into the table, and press enter.
7. Repeat with other constants if needed.

8.2 Saving the data-flash for use with other packs

1. While in the data-flash screen, use the File-→ Export menu to save the data-flash to a (*.gg) file

8.3 Loading previously saved data-flash constants from a file

1. While in the data-flash screen, use File-→ Import menu to load the data-flash from a (*.gg) file into program memory.
2. Push the “write all” button to write all values into the bq20z80 data-flash.
3. If existing calibration values in bq20z80 are to be preserved rather than overwritten with the values from the file, use the “Write All, Preserve”→ Calibration button instead.
4. Go to the “SBS Screen” and send the “Reset” command (Manufacturer Access 0041) to be sure that all settings go into effect.

Calibration of bq20z70/z90 Using EV Software

This document applies to users that require a small quantity of battery packs for evaluation. For mass production methods, see *Battery Pack Production Flow With bq20zXX* (SLUA391).

The procedure for calibration is different for PCBs and PCBs with cells attached. Calibration before cells are attached is recommended because this method is much faster. When cell are attached, long relaxation periods between the steps are needed to avoid errors with gas-gauging.

9.1 Calibration of the board if cells are not attached

Before calibration:

- Make all the necessary data flash settings to configure the pack. Send the “Reset” command (Manufacturer Access 0041).
- Do NOT send the “IT enable” command 0021 before the calibration, because it starts the gas-gauging algorithm with an uncalibrated pack.

1. Connect 1N (lowest cell (-)), 1P, 2P, 3P and 4P (highest cell (+)) terminals with 470 Ω, 1% resistors to emulate the cells. Apply voltage in the 16 V range between 1N and 4P.
2. Momentary short 4P and Pack+ pins to wake-up the gas-gauge from shut-down mode. Connect the EV2300 to the board and start the EV Software.
3. Current Offset Calibration
   - Enter the “Calibrate” screen.
   - Check the “CC Offset calibration” (uncheck all other boxes).
   - Push the “Calibrate part as indicated below” button.
   - Note that when SMB lines are disconnected, current offset is auto-calibrated to a more accurate value.
4. Voltage Calibration
   - Use a digital volt meter with better than 1-mV accuracy to measure voltage between the 1N and 4P pins. Do not rely on the accuracy of the applied voltage, accurate measurement of the "actual_voltage" is critical.
   - Enter the measured value into the “Enter actual voltage” text-box in the Voltage Calibration section of the “Calibrate” screen.
   - Enter the correct serial cell count (for example 3)
   - Check the “Voltage calibration” check box (uncheck all other boxes)
   - Check the “FET Control”→ OFF radio-button.
   - Push the “Calibrate part as indicated below” button.
   - Note that due to digital filter settling time, full accuracy of reported voltage are reached 5 minutes after calibration. Only after passing this time, comparisons between requested and reported voltage should be done to evaluate calibration accuracy.
5. Pack Voltage calibration
   - This step is optional and is usually not necessary. Make sure the "Voltage Calibration" has been performed. The default pack voltage calibration accuracy is sufficient for the purposes of raw pack voltage estimation.
   - Push the “Pack Voltage Calibration” button. Make sure DF:Calibration/Data/AFE Pack Gain is not zero after this calibration. If it is, it is recommended to short 4P to Pack+ before going through this step.
6. Temperature Calibration

- Measure the temperature using an external temperature measurement means.
- Enter the measured value into the “Enter actual temperature” text box.
- Check the “Temperature calibration” check box (uncheck all other boxes).
- Push the “Calibrate part as indicated below” button.

7. Current Gain Calibration
   - Connect a power supply in series with a digital ammeter with better than 1-mA accuracy between the 1N and Pack- (e.g. across the sense resistor). Set the voltage so that current is 2 A.
   - Take the actual current reading from the ammeter.
   - Enter the actual current reading into “Enter actual current” text box.
   - Check the “Pack current calibration” check box (uncheck all other boxes).
   - Make sure that in the “FET Control” selection group, “OFF (bypassed)” is selected.
   - Push the “Calibrate part as indicated below” button.
   - Note that after calibration is finished, FETs turn OFF
8. CC Board Offset calibration

   Ensure that no current is flowing and push "Software Board offset calibration" button. Note that the sample time right above this button should be set to at least 2 seconds.

9.2 Calibration if cells are attached

Making calibrations after cells are attached is not recommended because it is more complex and requires a longer time for providing sufficient cell relaxation after disturbance by current. However, if it cannot be avoided, calibration on assembled pack is done as follows:

1. Before calibration
   - Make all the necessary data flash settings to configure the pack. Send the “Reset” command (Manufacturer Access 0041).
   - Do NOT send the “IT enable” command 0021 before the calibration, because it starts the gas-gauging algorithm with uncalibrated pack.
2. Remove any external power.

   Remove any external power connected to Pack+ and Pack-. There should be no charge or discharge current flow to battery for at least 30 minutes prior to calibration because the cell voltage has a long relaxation period after such events. For the same reason, the Current Gain calibration should be done as the last calibration step.
3. Current Offset Calibration
   - Enter the “Calibrate” screen.
   - Check the “CC Offset calibration” (uncheck all other boxes).
   - Push the “Calibrate part as indicated below” button.
   - Note that when the SMB lines are disconnected, the current offset is recalibrated.
4. Voltage Calibration
   - If there is physical access to the Cell+ and Cell- terminals, turn ON the FETs to make voltage measurements. If physical access is available, skip this step

     To enable charge and discharge FETs, in the “Pro” screen, use the “Write SMB Word”, command 46, Word: 0006.
     - Use a volt meter with better than 1-mV accuracy to measure voltage between Pack+ and Pack- terminal.
     - Enter the measured value into “Enter actual voltage” text-box in the Voltage Calibration section.
     - Enter the correct serial cell count (for example 3).
     - Check the “Voltage calibration” check box (uncheck all other boxes).
     - Push the “Calibrate part as indicated below” button.
     - Note that due to digital filter settling time, full accuracy of reported voltage is reached 5 minutes after calibration. Only after passing this time, comparisons between requested and reported voltage should be done to evaluate the calibration accuracy.
5. Pack Voltage calibration
   - This step is optional and is usually not necessary. Make sure the "Voltage Calibration" has been performed. The default pack voltage calibration accuracy is sufficient for the purposes of raw pack voltage estimation.

- Push the “Pack Voltage Calibration” button.

6. Temperature Calibration
   - Measure the temperature using an external temperature measurement means.
   - Enter the measured value into “Enter actual temperature” text box.
   - Check the “Temperature calibration” check box (uncheck all other boxes).
   - Push the “Calibrate part as indicated below” button.
7. Current Gain Calibration
   - Enter the “Pro” screen in the EV Software, enable charge and discharge FETs using the “Write SMB Word”, command 46, Word: 0006
   - Use electronic load to apply discharge current of 2 A through the 1-mA accurate amperometer attached in series between Pack+ and Pack-.
   - Take the actual current reading from the amperometer.
   - Enter the actual current reading into the “Enter actual current” text box.
   - Enter the actual current reading into the “Enter actual current” text box.
   - Check the “Pack current calibration” check box (uncheck all other boxes).
   - Make sure that in the “FET Control” selection group, the “ON (External Load) is selected.
   - Push the “Calibrate part as indicated below” button.
   - Note that after calibration is finished, FETs turn OFF
8. CC Board Offset calibration

   Ensure that no current is flowing and push "Software Board offset calibration" button. Note that the sample time right above this button should be set to at least 2 seconds.
9. Calibration is complete

   Wait 30 minutes to let cells relax after being disturbed by the current during “Current Gain Calibration” and send the Manufacturer Access Command 0021 to enable the gas-gauging and turn-on FETs

Pack Assembly and The bq20zxx

Yevgen Barsukov *Battery Management*

This application report describes a recommended assembly sequence for a bq20zxx-based battery pack. This procedure results in the most time-efficient setup of the battery pack. Following are the steps for connecting a 4-series cell battery to the bq20zxxEVM board. Review the application report *bq20zxx EVM Data Flash Settings for Number of Serial Cells and Pack Capacity*, SLVA208, for further details on 2- and 3-series cell arrangements.

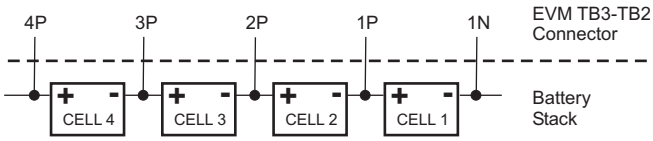


Figure 1. Connection Sequence

1. Connect the most negative terminal (– terminal of cell 1) of the serially-connected, 4-cell battery stack to the 1N PIN of the TB3–TB2 connector as shown in Figure 1.
2. Connect the positive terminal of cell 1 to 1P.
3. Connect the positive terminal of cell 2 to 2P.
4. Connect the positive terminal of cell 3 to 3P.
5. Connect the positive terminal of the battery stack (+) to 4P.
6. Connect external power (from 6 to 16.8V) to the Pack+ and Pack– terminals on connectors TB1 and TB4 to wake up the EVM from shutdown mode. External power does not need to remain connected once the bq20zxx has exited Shutdown Mode.
7. Connect the SMBus connector (J1) to the EV2300 adapter and start the EV software.
8. Navigate to the *Flash Screen*. Change the flash constants that correspond to the specific parameters of your application (refer to the data sheet or other application reports). For the first evaluation, the default values may be used.
9. Navigate to the *Calibration screen*. Select the check-box for *CC Offset Calibration*. Click the *calibrate part* button. It should show OK.
10. Uncheck previously-selected boxes. Select the check-box for voltage near *Measured voltage* field. Measure the actual pack voltage between pins 1N and 4P, and enter the value into the *Enter actual voltage* field. Click the *calibrate part* button.
11. To start fuel-gauging, navigate to the *Pro screen* in the EV software. Make sure that the *Write SMB Word* section reads: "SMB Command: 00 Word (hex): 0021" as shown in Figure 2, and click the *Write* button.

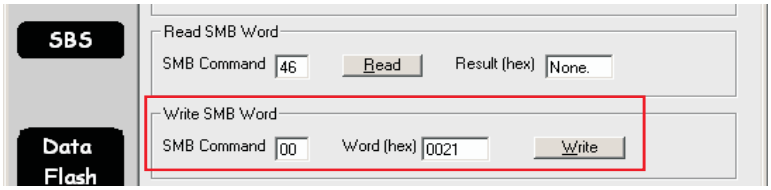


Figure 2. Fuel Gauging Command

12. Navigate to the SMB Screen and be sure that the QEN bit in Operation Status is set (red). The *Relative State of Charge* value is now updated to the correct value that corresponding to the state of charge of the attached cells.

13. Now the pack is ready. Simulate insertion into a system by shorting between the *Sys Pres* (System Present) and the *VSS* pins on the TB1–TB4 connector. At this point, the discharge and charge FETs are ON (as indicated by value of 0006 in the *FET Status* field in the SMB Screen of the EV software), and charge/discharge tests can be conducted. This step in not needed if the NR bit (nonremovable pack) is enabled in Operation Cfg B register.

Chapter 11

Preparing Optimized Default Flash Constants for Specific Battery Types

PMP Portable Power

ABSTRACT

Impedance Track™ technology allows bq20zxx fuel gauge ICs to automatically acquire and maintain parameters for battery modeling needed for continuous fuel-gauge accuracy, regardless of battery model or manufacturer. This application report discusses how to prepare optimized default flash constants for specific battery types.

11.1 Introduction

Impedance Track™ technology allows the bq20zxx fuel gauge to automatically acquire and maintain parameters for battery modeling needed for continuous fuel-gauge accuracy, regardless of battery model or manufacturer. The ICs are delivered pre-programmed with default values for these parameters. During daily use (charged, discharged, or left unused), new parameters specific for a given battery are collected by the algorithm.

The default parameters that are used for fuel gauging prior to discharge activity provide a high level of gas gauge accuracy. However, to maximize the accuracy and reach a 99% or better level, a full update of parameters is required. Therefore, before the first discharge cycle, the accuracy of the gas gauge is less than the 99% accuracy that is achieved after parameter acquisition. A full set of parameters is acquired when the battery completes two full discharge cycles with relaxations following charge and discharge.

If it is desirable to have maximal accuracy in the battery packs coming from the production line, even before any discharge activity occurs, it is useful to make a discharge cycle on one battery pack (let it acquire optimized parameters), save the configuration file with optimized parameters, and then program it into all battery packs coming from the production line where the cells are from the same supplier. The following steps are required to create a configuration file with optimized parameters and program them into battery packs during production.

In addition to improved accuracy, having pre-learned parameters increases the algorithm robustness in a field environment because, after learning occurs, the magnitude of the resistance change per update is limited to up to 3 times by the algorithm.

11.2 Creating Pre-Learned Defaults

The test setup procedure is described in the following steps.

1. If chemistry is not the default, program the .senc file for the corresponding chemical ID.
2. Set the appropriate data-flash constants.
3. Calibrate the board.
4. Attache the cells, and assemble the battery pack.

The accuracy of resistance values depends on the accuracy of the Qmax value. Therefore, if the approximate value of the actual Qmax is unknown, Qmax needs to be learned prior to resistance learning. However, if a close Qmax initial guess is known, resistance learning can proceed immediately. These two methods are addressed in the following steps.

When no close Qmax value is known:

1. Even though accurate capacity is unknown, set Qmax and design capacity to the cell capacity shown in the data sheet. Do not send IT enable command 0021.
2. Send SMB command 46, word 0006 to turn on the FETs.
3. Discharge the pack down to termination voltage at a C/5 rate.
4. Let it relax for 5 hours or more.
5. Send the IT enable command (0021). Bits QEN and VOK in Operation Status are set.
6. Charge pack to full capacity until the taper current is reached and the FC bit is set.
7. Let it relax for 2 hours. Qmax is learned at this point; this can be verified by MaxError changing to 3% and Update Status to 5%.
8. Discharge the pack down to terminate voltage at the typical low rate of your application. For laptops, it is usually C/5. The MaxError changes to 1%, and the Update Status changes to 6%.
9. Repeat steps 4 and 6 to 8 one more time to verify the gas-gauging accuracy.

When a close Qmax value is known:

1. Set an initial guess of Qmax (as found from previous IT tests or by discharging the battery at a C/20 rate).
2. Enable IT (command 0021).
3. Charge the pack to full.
4. Let it relax for 2 hours.
5. Discharge the pack to minimal device acceptable voltage (also set as Term Voltage flash constant) at a typical low rate (usually C/5) of your target application. The exact rate is noncritical. MaxError will change to 5%.
6. Let it relax for 5 hours. Qmax will update, MaxError will change to 1%, and the Update Status will change to 6%.
7. Repeat the foregoing steps 4 through 6 one more time to achieve the best resistance accuracy. (The accuracy after the first cycle can be affected by the inaccurate initial guess of the Qmax value.)
8. If the Operation Status bit R_DIS is set during this test, the Qmax initial guess was not accurate enough and so learning needs to be made using the previous procedure or after reloading the default settings and using the newly learned Qmax value as an initial guess.

11.3 Final Steps Before Exporting bqTester Binary Data-Flash Image (*.ROM File)

1. Start the EV Software for the bq20zxx.
2. Enter the Data Flash window, and push the Read Flash button.
3. In the File menu, click Export, and choose a *.gg filename for saving the pre-learned defaults, e.g., optimized.gg.
4. Open the saved file in a text editor such as Notepad, and change the value of Update Status from 06 to 02, which indicates that the parameters are learned but IT is disabled (as it should be in a new pack before calibration). Also, the cycle number in the SBS Configuration can be changed to 0.
5. Write a .senc file with the correct chemical ID to clear the hidden data-flash constants.
6. Write the gg file that you have modified back into the device.
7. You are now ready to export the data-flash image (*.ROM) file to be used in production.

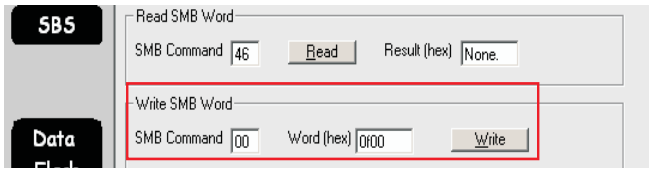
Updating Firmware With The bq20zxx and EVM

Garry Elder *Battery Management*

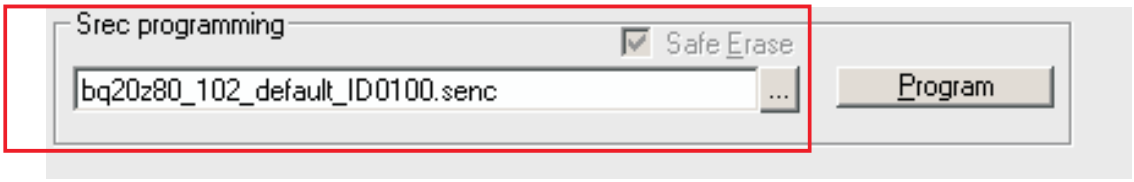
The following the steps are used to update the bq20zxx firmware in the EVM:

1. Power up the EVM by applying 16 V between Pack+ and Pack-. This step is not necessary if the cells are already attached.
2. Start the EV Software. Ignore the wrong-version warning about (press OK)

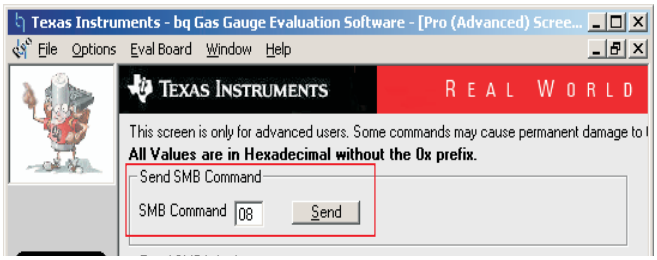
3. Navigate to the *Pro* screen.
4. Enter ROM mode by setting the *Write SMB Word* section to read: "SMB Command: 00 Word (hex): 0f00", and click the *Write* button.



5. In the *Srec programming* screen enter the path and file name for the new firmware file (*.senc). If needed, click the (…) button to browse for the file location.



6. Click the *Program* button to program the firmware. All flash-constants information including calibration will be lost, so it should be exported beforehand into a (*.gg) file.
7. Once programming is finished, execute the program by sending SMB command 08. Navigate to the *Send SMB command* screen, enter 08 in the *SMB Command* box, and push the Send button.



8. Restart the EV Software so the new version of firmware is recognized.

Using SHA-1 in bq20zxx Family of Gas Gauges

Travis Neely *PMP Portable Power*

ABSTRACT

The bq20zxx Impedance Track™ family of gas gauge ICs includes a highly sophisticated authentication algorithm, known as SHA-1, which requires little setup and development time and provides an effective, secure battery design.

13.1 Introduction

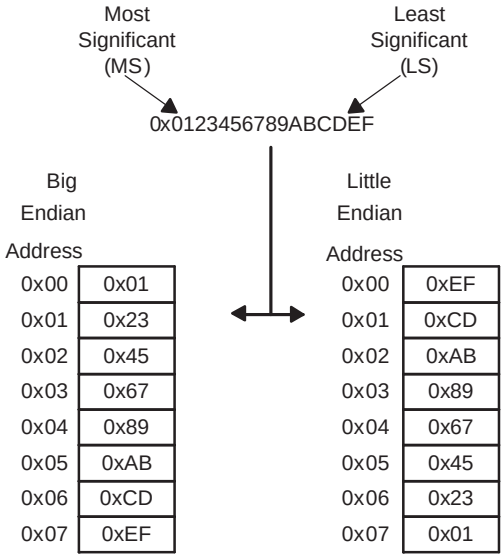
Battery counterfeiting is a major problem confronting original equipment manufacturers (OEM) today. One of the most effective methods to counter this issue is with the use of SHA-1 authentication routines in battery designs. Using this approach ensures that the OEM can track the suppliers for battery replacements. With this anti-counterfeiting algorithm, only battery packs manufactured by authorized subcontractors using the bq20zxx Impedance Track™ gas gauge IC with the SHA-1 can be integrated into OEM system designs. The SHA-1 authentication key in the bq20zxx can be regulated and tracked by the OEM. Multiple subcontractors can be supplied with different authentication keys for even greater security and regulation

13.2 Explaining Little Endian

The SHA-1 features of the bq20zxx use SMBus string reads and writes. Because SMBus communications is based on the Little Endian scheme of byte ordering, an understanding of Little Endian can reduce the complexity of the development process.

Two, byte-ordering schemes are used when storing multibyte data in memory: Little Endian and Big Endian. In Big Endian ordering, the most significant byte (MSB) is stored at the lowest possible memory address. This ordering method is most routinely used in Motorola processors.

In Little Endian ordering, the least significant byte (LSB) is stored first in memory at the lowest address. Little Endian is used in Intel processors. It is also used by the SMBus data transfer method for multibyte data transfers. In other words, SMBus always transfers the LSB first.



What is SHA-1?

This document describes the SHA-1 functions only as they are used with the bq20zxx gas gauge IC. More complete explanations of the SHA-1 algorithm are available in many articles and books. For example, see www.faqs.org/rfcs/rfc3174.html for an excellent description of the SHA-1 algorithm and some C-code examples of how to implement it.

Three primary bq20zxx functions are used to implement the SHA-1 security feature in a system design. The first function is the SHA-1 challenge. The challenge is a 20-byte (160-bit) string sent to the bq20zxx by the host. The SHA-1 algorithm in the bq20zxx then is required to send back a response. The 20-byte challenge, located at SMBus command 0x2f is a 20-byte SMBus string write. As with the rest of the SHA-1 function, this challenge string is Little Endian.

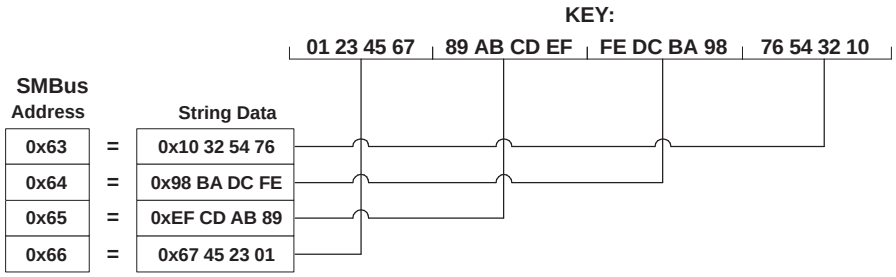
The second bq20zxx function used to implement the SHA-1 feature is the SHA-1 response. The response is a 20-byte string read. Once a challenge is given and the bq20zxx is given time to compute the response, it is available in the same SMBus command as the challenge (command 0x2f).

The third function is the SHA-1 authentication key. The authentication key is the primary function of the SHA-1 algorithm. The key is input during production only by using the *Gold Data Flash File* methodology explained in a later section entitled *How to Set Up for Production*. Once the key is written and the part sealed, it is completely inaccessible. It must be kept secret. With the key unknown, it is virtually impossible for the challenge/response pattern to be decoded. If the key is compromised, the authentication is no longer effective.

How to Use SHA-1 in the bq20zxx

The following two steps are used to implement the SHA-1 algorithm in the bq20zxx.

1. **Create a unique authentication key, and write it to the part during assembly: The authentication key resides in the SMBus addresses 0x63-0x66 in 4-byte strings. The four strings are read/write accessible until the bq20zxx is sealed. When written using an SMBus string write command, they are retained permanently in flash memory and can only be changed when the bq20zxx is unsealed. They are stored in Little Endian format as shown in the following diagram. The SHA-1 authentication key defaults to *0123456789abcdeffedcba9876543210* in the bq20zxx. This is a default and is not intended for production. It should be changed to a unique key prior to production to ensure that security is not compromised.**



2. **Implement SHA-1 in the OEM host system.**
   a. **The host has to know the SHA-1 authentication key:**
   The host must know the key defined in step 1. This key is used in the host system to determine what the response should be.
   b. **The host has to issue a random challenge:**
   The host sends a challenge using a 20-byte string write to SMBus command 0x2f in Little Endian format. It is important that the challenge be random every time to ensure security. Here is an example of a challenge and writing it in Little Endian:

   Using the example of:

0x20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 3E 2F 30 31 32 33

   Must be written in Little Endian as follows:

0x33 32 31 30 2F 2E 2D 2C 2B 2A 29 28 27 26 25 24 23 22 21 20

   c. **The host computes the response:**
   With the known SHA-1 authentication key and random challenge, the host computes the anticipated response from the bq20zxx.

d. **Bq20zxx computes the response:**
The bq20zxx computes the response at the same time that the host is computing it. The bq20zxx should be given greater than 100 ms to compute the response and put it into memory for retrieval.

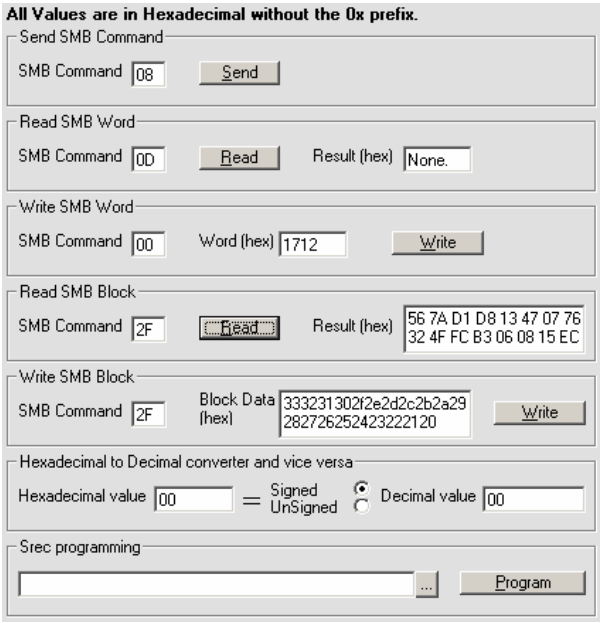
e. **The host has to read the response:**
The host reads a response from the same command (0x2f) to which the challenge was written. The response is a 20-byte string read in Little Endian format.

f. **The host must validate the response:**
The host must compare the response read from command 0x2f in the bq20zxx to what was computed in step *2c*.

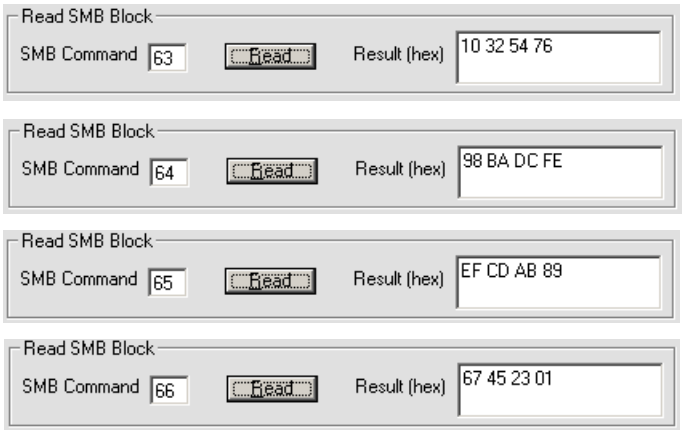
g. **If the response is validated, then the battery is authorized. Otherwise, the host can reject the battery pack.**

Experimenting With the bq20zxx Evaluation Software:

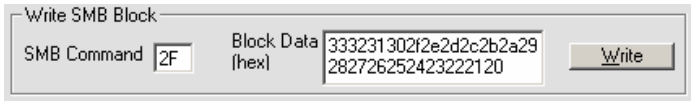
The PRO screen of the bq20zxx Evaluation software can be used to experiment with the SHA-1 features. This screen includes the SMBus read and write block functions that are required for SHA-1. Use the procedure described in the preceding section entitled *How to Use SHA-1 in the bq20zxx* with the following functions:



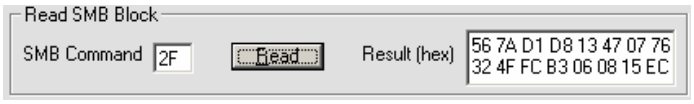
1. **Use the Read SMB Block frame to verify that the key is written to the desired value using the four reads to SMBus commands 0x63-66. They should read as follows by default. Notice that they report in Little Endian.**



2. **If the authentication key needs to be changed, it can be modified with an SMBus write to the same SMBus commands 0x63-66 in Little Endian.**
3. **Now, write the challenge in Little Endian to the bq20zxx using the Write SMB Block Frame:**



4. **Then, use the Read SMB Block Frame to read the Response from the bq20zxx:**



5. **Notice that only 16 bytes fit in the Read SMB Block Frame. The entire response is in the Result window but not wholly visible. Select and highlight the Result data and paste it into a text editor to see the entire result as follows:**

56 7A D1 D8 13 47 07 76 32 4F FC B3 06 08 15 EC 23 5C AB FE

How to Set Up for Production:

Setting up the SHA-1 for production assembly is simple using the BqTester *Gold Data Flash File* methodology for testing production modules. See *Using the bqTester Software* (SLUA352) application report or *bqMulti-Site Tester* user guide at www.ti.com for more information.

Using the bq20zxx EV software, set up the module as required for the application. Many of the TI documents in the corresponding bq20zxx IC product folder at www.ti.com can assist the user in setting up the module. As an example, for the bq20z80, these include:

- *Preparing Optimized Default Flash Constants For Specific Battery Types* application report (SLUA334)
- *bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity* application report (SLVA208)
- *Pack Assembly and the bq20z80* application report (SLUA335)
- *Exploring the bq20z80 Impedance Track Evaluation Kit* application report (SLUA351)
- *Pack Assembly and the bq20z80* application report (SLUA335)

Once a module is configured as required for the particular application, the desired SHA-1 authentication key needs to be saved into the bq20zxx module as explained in the previous section *How to Use SHA-1 in the bq20zxx*. With this completed, the SHA-1 key is stored, and the data flash meets the requirements for the *Gold Data Flash File*.

As explained in *Using the bqTester Software* application report or the *bqMulti-Site Tester* user guide, create the *Gold Data Flash File*. Use this file with bqTester or bqMulti-Site Tester Software for module testing in production. Be sure to seal the bq20zxx as explained in the corresponding bq20zxx data sheet. All modules produced with this *Gold Data Flash File* and bqTester or bqMulti-Site Tester will have the same hidden SHA-1 key and be ready for use.

bq20z90 (v110) Change List

Battery Management

ABSTRACT

This document describes the changes being made to the previously released bq20z90 (v102) design.

14.1 Introduction

The new bq20z90 (v110) firmware upgrade has been released in order to address the following requests and new feature additions:

- Manufacturer Info is now 20 bytes.
- The operation of the Zero Voltage Charge function has been corrected. Previously, this feature was not functioning correctly.
- The optional 99% RSOC hold-off option has been improved. If the *[RSOCL]* Bit = 1, then the 99% RSOC hold feature is activated. This means that *SBS.RSOC* stays at 99% *during charging* until a valid charge termination.

The following new orderable part numbers will be released to support this new device.

bq20z90DBT-V110

bq20z90DBTR-V110

Note that the latest version of the evaluation software is required to be able to read and write all the data flash configuration locations.

14.2 Summary

These changes are provided in order to enhance the functionality of the previous generation firmware.

bq20z70 (v110) Change List

Battery Management

ABSTRACT

This document describes the changes being made to the previously released bq20z70 (v101) design.

15.1 Introduction

The new bq20z70 (v110) firmware upgrade has been released in order to address the following requests and new feature additions:

- Manufacturer Info is now 20 bytes.
- Over Charge Configuration is now user programmable such that on occurrence of a charging fault, if the *[OCHGI]* bit in *Charge Fault Cfg* is set, then the CHG FET is turned OFF.
- The operation of the Zero Voltage Charge function has been corrected. Previously, this feature was not functioning correctly.
- The optional 99% RSOC hold-off option has been improved. If the *[RSOCL]* Bit =1, then the 99% RSOC hold feature is activated. This means that *SBS.RSOC* stays at 99% *during charging* until a valid charge termination.

The following new orderable part numbers will be released to support this new device.

bq20z70PW-V110

bq20z70PWR-V110

Note that the latest version of the evaluation software is required to be able to read and write all the data flash configuration locations.

15.2 Summary

These changes are provided in order to enhance the functionality of the previous generation firmware.

Thermistor Coefficient Calculator for TI Advanced Fuel Gauges

Doug Williams *Battery Management*

ABSTRACT

TI advanced fuel-gauge battery-management ICs use a polynomial model to translate the voltage measured across the thermistor terminals into a temperature value. While the recommended Semitec AT103 is readily available, some customers prefer to use an alternate device. This report describes the use of a companion Excel® spreadsheet that automates coefficient calculation for a given thermistor.

16.1 Introduction

The firmware algorithm in TI advanced fuel gauge battery management ICs uses a polynomial model to translate voltage measured across the thermistor terminals into temperature. While the recommended Semitec AT103 is readily available in various shapes, some customers prefer to use an alternate device. This report describes the use of a companion Excel spreadsheet that automates the calculation of coefficients for a given thermistor.

The Thermistor Coefficient Calculator is a Microsoft® Excel spreadsheet, which is available as a zip file in the same location as this report. It can be used for various advanced fuel gauge ICs such as the bq2084, bq20z70, bq20z80, bq20z90, etc.

16.2 Theory of Operation

Solver, an add-in tool for Excel, which is part of the standard installation, is used in this case to find a solution to a set of 3rd order polynomials. Given a few points on an unknown curve, it finds the coefficients of a cubic polynomial equation that best fits the available data. The fuel-gauge device firmware uses the cubic polynomial along with the dataflash-based coefficients at 1-s intervals when converting the A/D reading from the thermistor into a temperature value.

Solver's job is to minimize the value in cell B33 (see Figure 1), which is the sum of the norms for each known data point. The norms are simply the square of the difference between what you want and what you get. Solver updates the polynomial coefficients in E25 ~ E28 for the best overall fit. You can, of course, change the coefficients manually to see what happens. The values in E31 ~ E36 should be programmed into the respective fuel gauge dataflash locations.

	A	B	Calculation of A/D Count	Data Flash Thermistor Constants	E	F	G	H I	J	K	L
1	Temperature	Resistance	Calculation of A/D Count	Calculation of best-fit (using 3rd order polynomial)	Norm		Instructions		Partial Result Bounds Check		
2	-20	67770	25982	-19.55338015	0.199469		1. Insert Temperature and Resistance values in colums A&B		10248.5197	-3774.69	
3	-15	53410	25309	-15.13893104	0.019302		2. Verify A/D count value in cell C2 does not exceed 27000		10557.1208	-3760.757	
4	-10	42470	24537	-10.40258881	0.162078		If necessary, raise value of R1 in cell B24 to a higher standard		10911.1179	-3752.579	
5	-5	33900	23646	-5.334192226	0.111684		resistor value so that C2 is under 27000.		11319.6818	-3753.509	
6	0	27280	22657	-0.155141665	0.024069		3. Select Solver from Tools menu. Use Add-Ins menu if not available.		11773.1833	-3767.55	
7	5	22050	21562	5.103094832	0.010629		4. Set Target Cell to $B$33		12275.2905	-3799.063	
8	10	17960	20391	10.26512627	0.070292		5. Choose Equal to: Value Of 0 (choose "Value Of", enter 0		12812.2472	-3851.329	
9	15	14690	19143	15.35518484	0.126156		6. Set "By Changing Cells" to $E$25:$E$28		13384.5119	-3928.155	
10	20	12090	17853	20.30002249	0.090013		7. Press Solve button - Accept the solution, even though not "feasible"		13976.0355	-4030.476	
11	25	10000	16537	25.1540882	0.023743		8. Compare columns A and D to evaluate the accuracy		14579.4813	-4158.854	
12	30	8313	15220	29.96452929	0.001258		A lower number in B33 indicates a better fit		15183.3856	-4311.593	
13	35	6940	13920	34.80931675	0.03636		9. Linearity may be improved by changing R2 in some cases		15779.4947	-4486.165	
14	40	5827	12668	39.69777558	0.09134		10. Insure none of the values in columns J or K exceed +/- 32767		16353.5936	-4676.647	
15	45	4911	11469	44.70168577	0.088991				16903.3895	-4879.628	
16	50	4160	10344	49.78340483	0.046913				17419.2531	-5088.375	
17	55	3536	9293	54.9514734	0.002355				17901.1844	-5299.392	
18	60	3020	8328	60.11969589	0.014327				18343.6807	-5506.755	
19	65	2588	7445	65.25409511	0.064564				18748.5763	-5707.915	
20	70	2228	6648	70.25884332	0.067				19114.0371	-5898.852	
21	75	1924	5927	75.11718798	0.013733				19444.6483	-6079.239	
22	80	1668	5283	79.74269257	0.066207				19739.9516	-6246.513	
23											
24	R1	8450									
25	R2	61900									
26	Vref	3.3									
27	Vadref	3.3									
28	ADres	0.000100708									
29	Vadmax	2.64									
30	Rs	7435.03909									
31	Vs	2.903624733									
32											
33	Sum of Norms:	1.330484661									
34											
35											
36											
37											

Polynomial coefficients	Value
A0	4032.48
A1	-7837.818
A2	22162.45
A3	-30050.77

Data Flash Thermistor Constants	
A0 (** Coefficient 4)	4032
A1 (** Coefficient 3)	-7838
A2 (** Coefficient 2)	22162
A3 (** Coefficient 1)	-30051
Min A/D	0
Max Temp (K)	4032

** The polynomial coefficients have alternate names in some fuel gauges

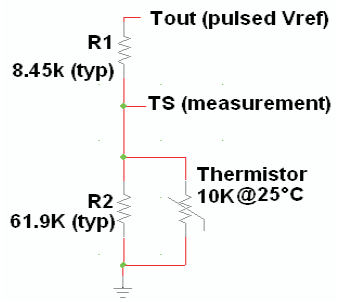


Figure 1. Thermistor Coefficient Calculator Spreadsheet

16.3 Thermistor Tables

Enter the data for the desired thermistor into cells B2 ~ B22 which correspond to the temperatures in column A. Some vendors include resistance tables in their catalog; others provide a calculator for you to generate them. If a given vendor only supplies a small table with multiples of 10°C, then use it as-is in the spreadsheet, but include some of the degree-resistance pairs twice to fill up the table of 21 pairs.

16.4 Circuit Modifications

For maximum accuracy, the voltage input voltage to the A/D converter in the fuel gauge should be limited to around 82% of the reference voltage, which is the same as V_{CC} in this case. Looking at it another way, the A/D count should not exceed 27000 (82% of full scale 32767) counts for low temperature readings that must be accurate. Column C displays the expected A/D count for a given temperature. Measurements between 27000 and 32767 will be degraded somewhat, but still useful.

The recommended thermistor circuit, where R1 = 8.45 kΩ, R2 = 61.9 kΩ and Thermistor = 10 kΩ at 25°C, should satisfy the above requirement in most cases. However, if a 10-kΩ thermistor cannot be used, the fixed resistors should be modified in cells B24 and B25 to optimize the measurement. B25 is used to linearize the thermistor curve somewhat, enhancing the polynomial curve-fitting accuracy.

Chapter 17

bq20z70/90 Gas Gauge Circuit Design

Doug Williams *Battery Management*

ABSTRACT

Components in the bq20z70/90 chipset reference design are explained in this application report. Design analysis and suggested tradeoffs are provided, where appropriate.

17.1 Introduction

The bq20z90 Advanced Gas Gauge chipset has approximately 85 components in the reference design for a 2-thermistor, 4-cell application with 5 LEDs. The bq20z70, with no LEDs has approximately 78 components. For clarity, these chipsets are grouped into the following classifications: High-Current Path, Gas Gauge Circuit, AFE/Secondary-Current Protection, and Secondary-Voltage Protection.

The discussion is based on the 4-cell reference design for the bq20z90/bq29330/bq29412 chipset. The complete schematic is available on the last page of this document.

17.2 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, the sense resistor, and then returns to the PACK– terminal (see the reference design schematic at the end of this document). In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

Protection FETs

The N-channel charge and discharge FETs should be selected for a given application. Most portable battery applications are a good match for the FDS6690A or equivalent. The P-channel precharge FET can usually be implemented with a smaller, less expensive device depending on the desired amount of precharge current.

The Fairchild FDS6690A is an 11-A, 30-V device with Rds(on) of 12.5 mΩ when the gate drive voltage is 10 V.

If a precharge FET is used, R38 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to (Vcharger – Vbat) / R38 and maximum power dissipation is $(Vcharger - Vbat)^2 / R38$.

The gates of all protection FETs are pulled to the source with a high-value resistor between gate and source to ensure that they are turned off if the gate drive is open.

Capacitors C27 and C28 help to protect the FETs during an ESD event. The use of two devices ensures normal operation if one of them becomes shorted. In order to have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C27 and C28 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

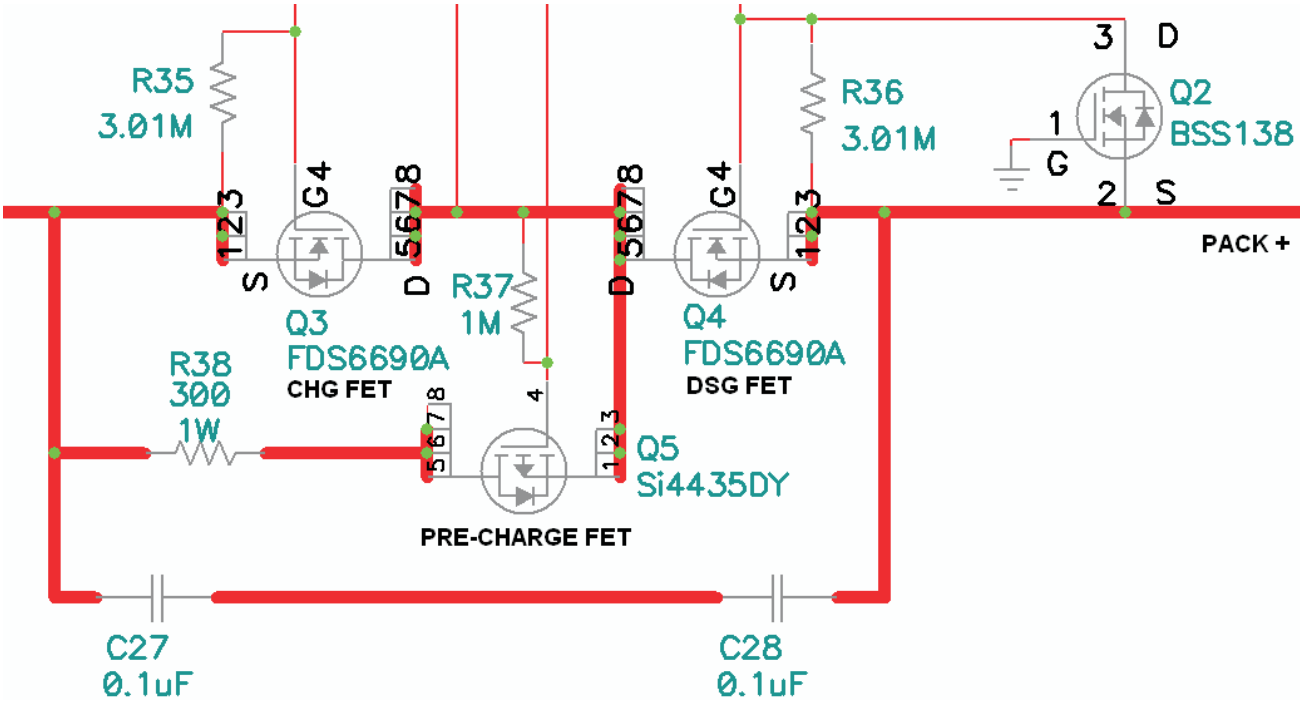


Figure 1. Protection FETs

Chemical Fuse

The chemical fuse (Sony Chemical, Uchihashi, etc) is ignited under command from either the bq29412 secondary voltage protection IC or from the SAFE pin of the gas gauge. Either of these events applies a positive voltage to the gate of Q1 in Figure 2, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Ensure that the proper voltage, current, and Rds(on) ratings are used for this device. The fuse control circuit is discussed in detail in the Gas Gauge Circuit section of this document under the heading *Safe Circuitry*.

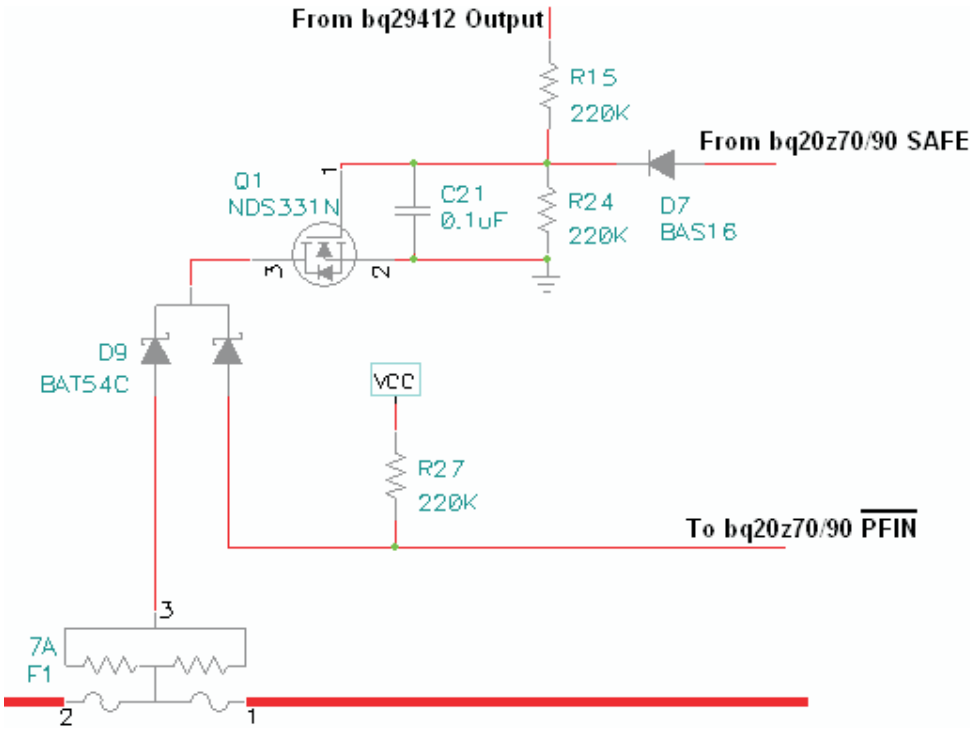


Figure 2. Chemical Fuse

Lithium-Ion Cell Connections

The important thing to remember about the cell connections is that high current flows through the top and bottom connections, and therefore the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. This is critical for gauging accuracy in the Impedance Track™ gauges. The location marked 4P in Figure 3 indicates the Kelvin connection of the most positive battery node. The connection marked 1N is equally important.

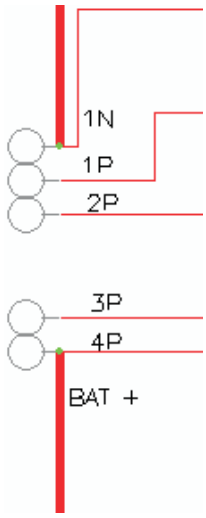


Figure 3. Lithium Ion Cell Connections

Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. Not only the sense lines, but the single-point connection to the low-current ground system must be made here in a careful manner.

The sense resistor should have a temperature coefficient no greater than 75 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq29330. (See relevant tables in the data sheet). Select the smallest value possible in order to minimize the negative voltage generated on the bq29330 pin 8 (VC5) node during a short circuit. This pin has an absolute minimum of –0.3 V. For a pack with two parallel cylindrical cells, 10 mΩ is generally ideal . Parallel resistors can be used as long as good Kelvin sensing is ensured.

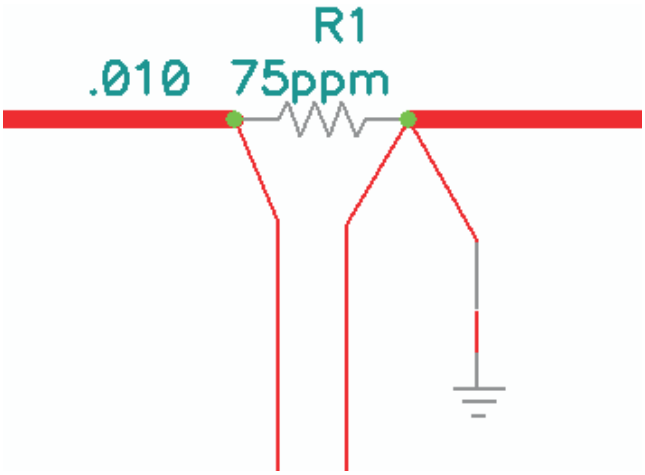


Figure 4. Sense Resistor

ESD Mitigation

A pair of series 0.1-µF ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors should become shorted.

Optionally, a tranzorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

17.3 Gas Gauge Circuit

The Gas Gauge Circuit includes the bq20z70/bq20z90 and its peripheral components. These components are divided into the following groups: LEDs, Differential Low Pass Filter, Power Supply Decoupling/ RBI/Master Reset, System Present, SMBus Communication, and SAFE circuit.

LEDs

The LEDs do not need current-limiting resistors because the bq20z90 LED pins have programmable current sink to simplify the design. The display switch pulls the bq20z90 pin 14 to ground to generate an interrupt. It is pulled up to 2.5 V with a 220-kΩ resistor. However, if your packaging is arranged such that an ESD may hit the switch, you may want to insert a clamping diode, and/or RC damping here also.

The 3.3-V output of the bq29330 at the LEDOUT pin powers the LEDs. Note that a 4.7-µF ceramic capacitor is required on the LED output for loop stability.

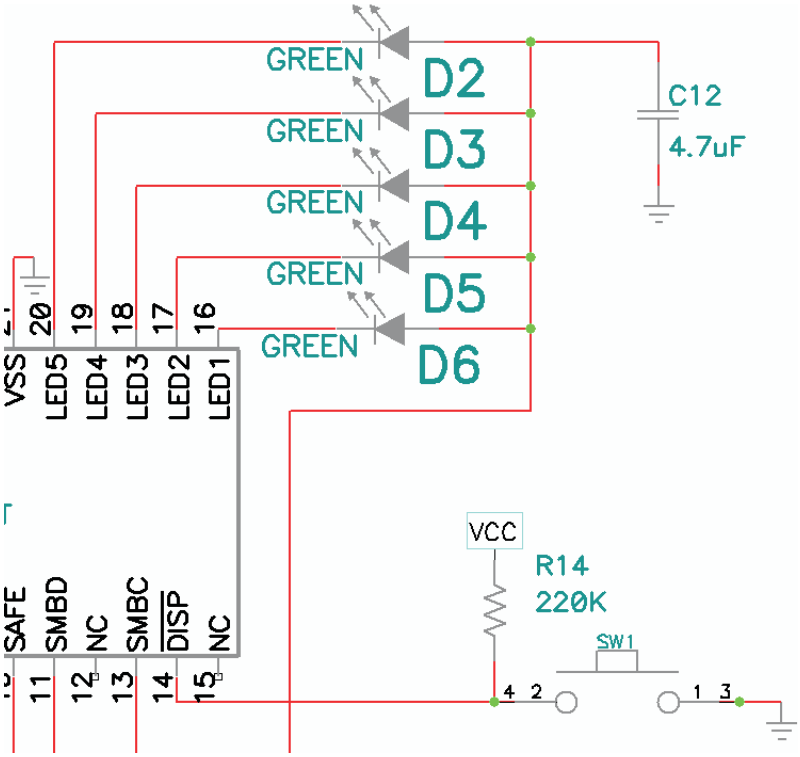


Figure 5. LEDs and Display Switch

Differential Low Pass Filter

As shown in Figure 6, a differential filter should precede the current sense inputs of the gas gauge. This filter eliminates the effect of unwanted digital noise, which could cause offset in the measured current. Even the best differential amplifier has less common-mode rejection at high frequencies. Without a filter, the amplifier input stage may rectify a strong RF signal, which then may appear as a dc offset error.

Five percent tolerance of the components is adequate because capacitor C6 shunts C3/C7 and reduces AC common-mode arising from component mismatch. It is important to locate C6 as close as possible to the gas gauge pins. The other components also should be relatively close to the IC. The ground connection of C3 and C7 should be close to the IC.

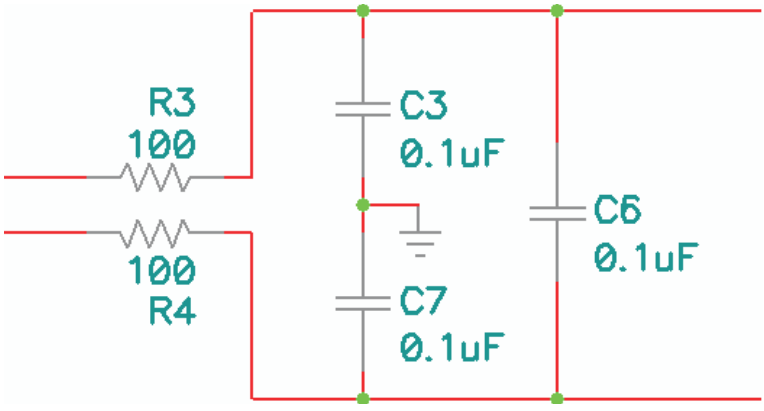


Figure 6. Differential Filter

Power Supply Decoupling, RBI, and Master Reset

Power supply decoupling is important for optimal operation of the bq20z70 and bq20z90 advanced gas gauges. As shown in Figure 7, a single 0.1-µF ceramic decoupling capacitor from V_{CC} to V_{SS} must be placed adjacent to the IC pins.

The RBI pin is used to supply backup RAM voltage during brief transient power outages. The partial reset mechanism makes use of the RAM to restore the critical CPU registers following a temporary loss of power. A standard 0.1-µF ceramic capacitor is connected from the RBI pin to ground as shown in Figure 7.

XRST (bq29330) and ~MRST (bq20z70/90) are connected to allow the AFE to control the gas gauge reset state. The connection between these pins must be as short as possible in order to avoid any incoming noise. With the recommended orientation of the two ICs, direct interconnection does not cause a problem. If unwanted resets are found, one or more of the following solutions may be effective:

- Add a 0.1-µF ceramic capacitor between MRST and ground.
- Provide a 1-kΩ pullup resistor to 2.5 V at MRST.
- Surround the entire circuit with a ground pattern.

Again, these steps are not normally required if the ICs are located close together. If a test pin is added at MRST, it should be provided with a 10-kΩ series resistor.

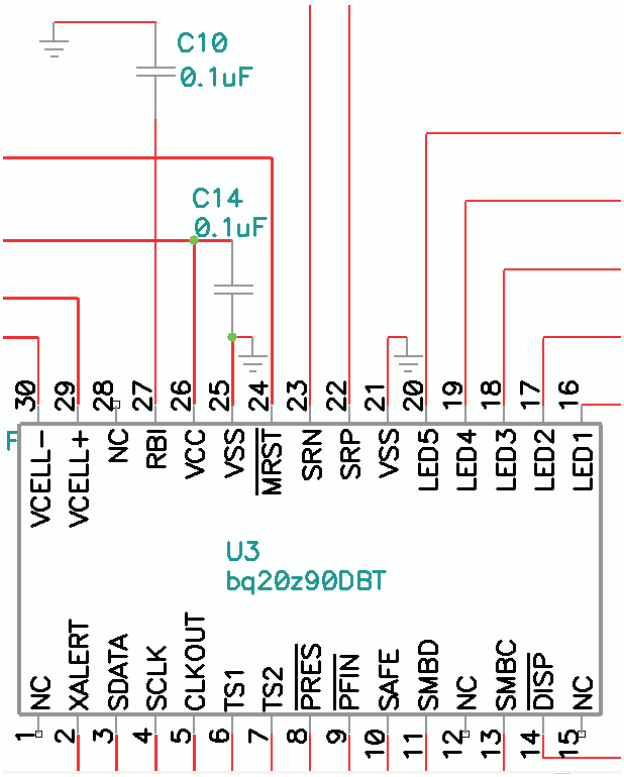


Figure 7. Power Supply Decoupling

System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The $\overline{\text{PRES}}$ pin of the bq20z70/bq20z90 is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a brief 4-µs sampling pulse once per second.

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. R34 and the 4.7-V Zener diode D10 protect against positive ESD pulses and an inadvertent short to PACK+. R28 limits the current that would flow out of the IC in parallel with the current through D10 for negative ESD pulses. Observe the voltage rating of D10 in order to maintain signal integrity and avoid electrical stress to the IC.

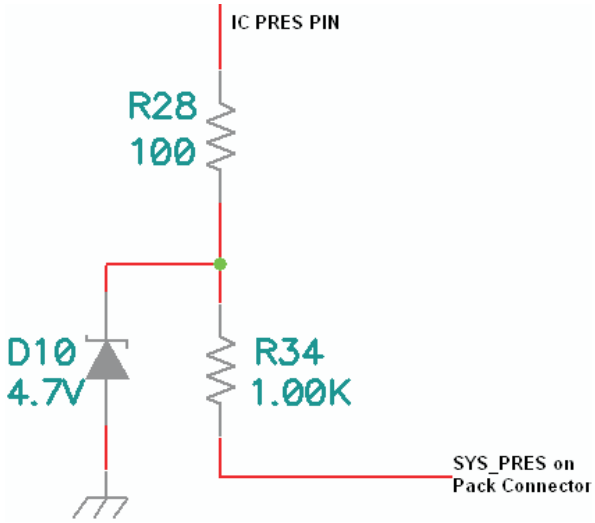


Figure 8. System Present ESD and Short Protection

SMBus Communication

As with the System Present pin, the SMBus clock and data signals interface to the outside world on the pack connector. Each signal employs an ESD protection scheme similar to that previously described for System Present (see Figure 9). It should be noted, however, that the 5.6-V Zener diode must have nominal capacitance below 100 pF in order to meet the SMBus specifications. The AZ23C5V6 is a recommended device. Also, the resistor on the pack side is only 100 Ω to maintain signal integrity. Note that the Zener diode will not survive a long-term short to a high voltage. If it is desirable to provide increased protection with a larger input resistor and/or Zener diode; carefully investigate the signal quality of the SMBus signals under worst-case communication conditions.

Resistors R22 and R23 provide pulldown for the communication lines. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto offset calibration and then goes into sleep mode to conserve power.

ESD protection operates the same as with the System Present network previously described. For the SMB clock signal, R19 and part of D8 provide clamping for positive ESD pulses, while R18 limits the current coming out of the IC (in parallel with the current through D8) for negative ESD pulses.

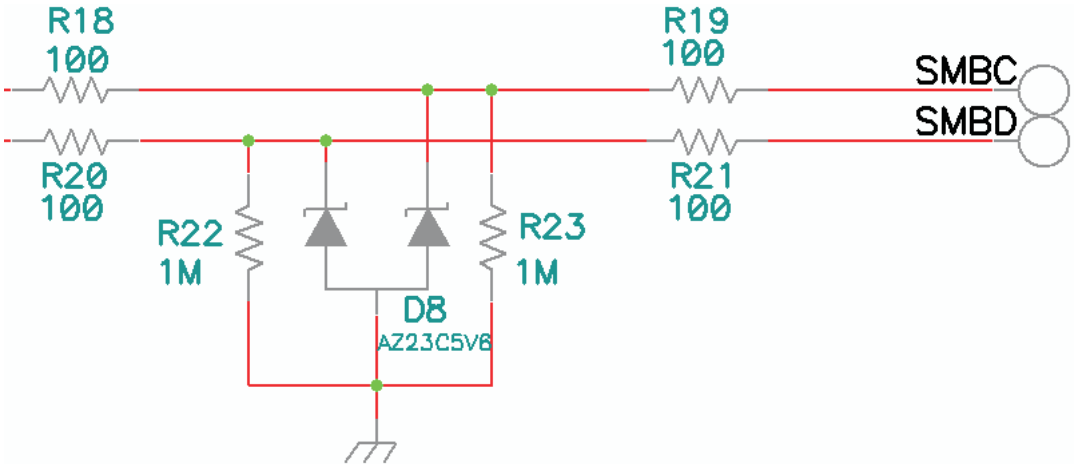


Figure 9. ESD Protection for SMB Communication

SAFE Circuitry

The SAFE output of the bq20z70/90 is designed to ignite the chemical fuse if one of the various safety criteria is violated. The PFIN input is used to monitor the state of the secondary-voltage protection IC. Q1 ignites the chemical fuse when its gate is high. R15, R24, and D7 form a logical OR gate, which enables the Q1 gate if either the SAFE signal or the output of the bq29412 device go to the high state. The 7-V output of the bq29412 is divided in half by R15 and R24, which provides adequate gate drive for Q1 while guarding against excessive back current into the bq29412 from D7 if the SAFE signal is high.

The use of C21 is generally good practice, especially for RFI immunity, but may be removed if desired because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that may come from the SAFE output during the cell connection process.

The combination of D7, C21, and the gate capacitance form a peak detector with R15 and R24 as a discharge path. It is important to note that this network rectifies strong RF signals and produces a positive DC level on the gate of the FET. This potential issue can be avoided by ensuring that the trace on the anode side of D7 is kept short or is shielded by ground on both sides.

When the fuse is commanded to ignite, the right side of D9 becomes forward-biased, which notifies the gas gauge of the situation. In this manner, the output of Q1 can be recorded for future fault analysis. The left side of D9 blocks any unwanted current through the FET body diode in the case of a reverse-connected charger.

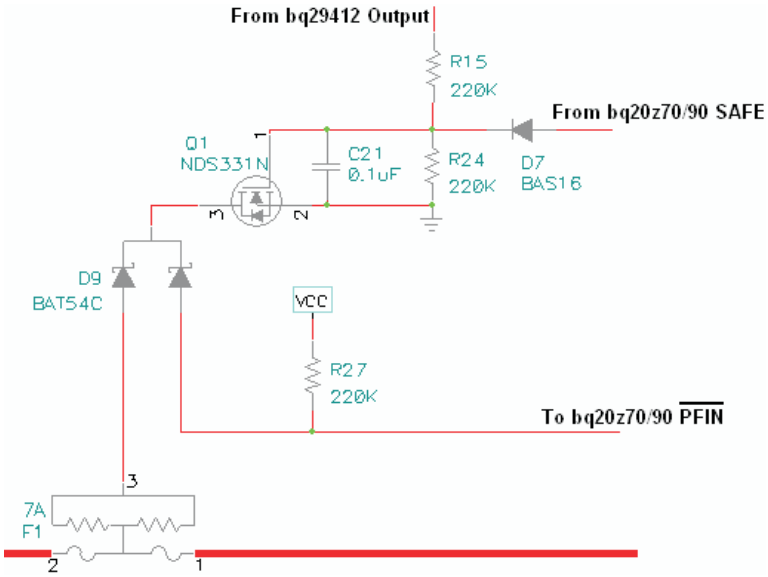


Figure 10. SAFE Circuit

For proper safety protection, It is extremely important to be certain that the fuse ignites when commanded. If alternate components are selected, an analysis such as the following must be made.

The fuse drive can be modeled as a high (~2.5 V) output from the SAFE pin, driving current through a signal diode (BAS16) into a load of approximately 110 kΩ. The minimum voltage at the SAFE pin is a function of the 2.5-V LDO in the bq29330 AFE, which has a guaranteed minimum of 2.41 V from –40°C to 110°C. With the 110-kΩ load, the output current is 23 mA. At this current, the drop from V_{CC} to the SAFE pin is specified to be less than 1.5 mV over temperature.

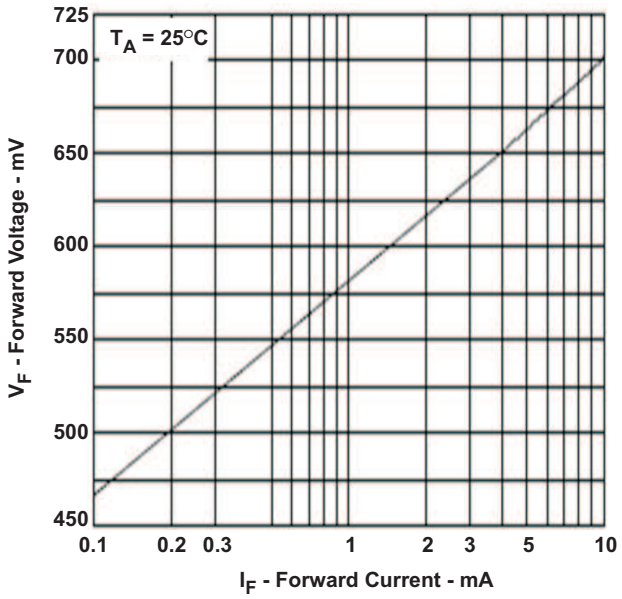


Figure 11. BAS16 Diode Forward Voltage Drop

Figure 11 is the forward voltage drop as a function of forward current from the diode data sheet. Extrapolating down to 23 mA shows diode forward voltage to be ~400 mV at 25°C. With a 50°C change in temperature, the diode drop could be as much as 400 mV + 1.6 mv × 50°C = 480 mV at –25°C.

Worst-case minimum voltage at the gate of the NDS331N is given as:

+25°C Vgs = 2.41 V – 0.0015 V – 0.400 V = 2.0085 V

+75°C Vgs = 2.41 V – 0.0015 V – 0.320 V = 2.0885 V

–25°C Vgs = 2.41 V – 0.0015 V – 0.480 V = 1.9285 V

In this case, the temperature effects of the diode and the FET work together to advantage. The worst-case gate-source voltage allows approximately 3 A to flow in the drain at all expected battery temperatures (see Figure 12). Therefore, it can be concluded that there is ample margin to ensure ignition of the chemical fuse.

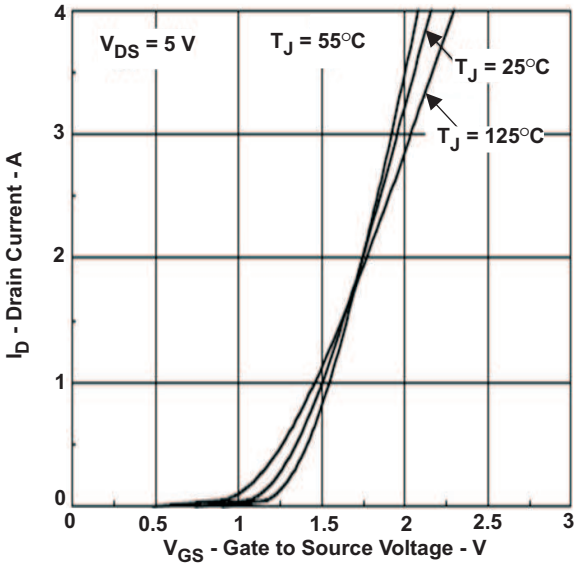


Figure 12. NDS331N FET Turnon Characteristic

17.4 AFE/Secondary-Current Protection

The bq29330 analog front end (AFE) provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, voltage translation, and the low dropout 2.5-V and 3.3-V regulators for the gas gauge and LEDs. The following discussion examines Cell and Battery Inputs, Pack, VCC, PMS Inputs and FET Control, Regulator Outputs, Temperature Output, and Cell Voltage Output.

Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter with a time constant of at least 10 µs. This filter provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some tradeoff for cell balancing versus safety protection.

Internal FETs in the bq29330 provide about a 400-Ω resistance, which can be used to bypass charge current in individual cells that may be overcharged with respect to the others. (Of course, this is not done during the low duty cycle voltage measurement phase) If the filter is built with 1-kΩ resistors and 0.01-µF capacitors, the cell-balancing feature is not effective because the total bypass resistance across a cell is 1000 + 1000 + 400 = 2400 Ω; therefore, the bypassing current is too small. As the reference design indicates, TI recommends 100-Ω resistors and 0.1-µF capacitors. Values between 200 Ω and 470 Ω can provide limited cell-balancing functionality.

The BAT input uses a diode (D1) and 1-µF ceramic capacitor (C13) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

Also, as described previously in the High Current Path section, the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a drop in the high-current PCB copper.

Some designers prefer to specify the 100-Ω cell input resistors as the fusible type, for protection in the event of a short inside U2. This is one of those tradeoffs where the benefit may or may not be valuable and may depend on corporate policy.

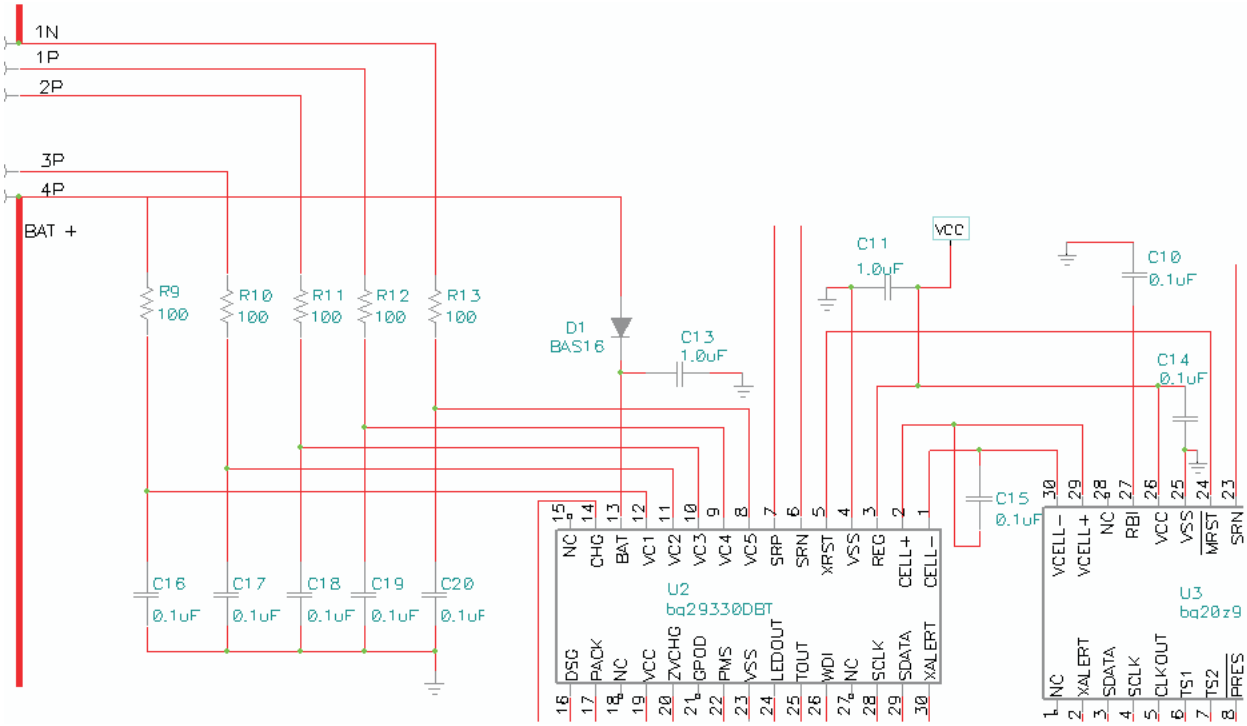


Figure 13. Cell and BAT Inputs

PACK, VCC, PMS Inputs, and FET Control

The PACK and VCC inputs provide power to the AFE from the charger. The PACK input also provides a method to measure and detect the presence of a charger. The PACK input uses a 1-kΩ resistor, whereas the VCC input uses a 1-µF ceramic capacitor (C26) to decouple it from the PACK+ input. This guards against input transients and prevents misoperation of the gate driver during short-circuit events. Ensure that the voltage rating of C26 is adequate to withstand the full-system voltage.

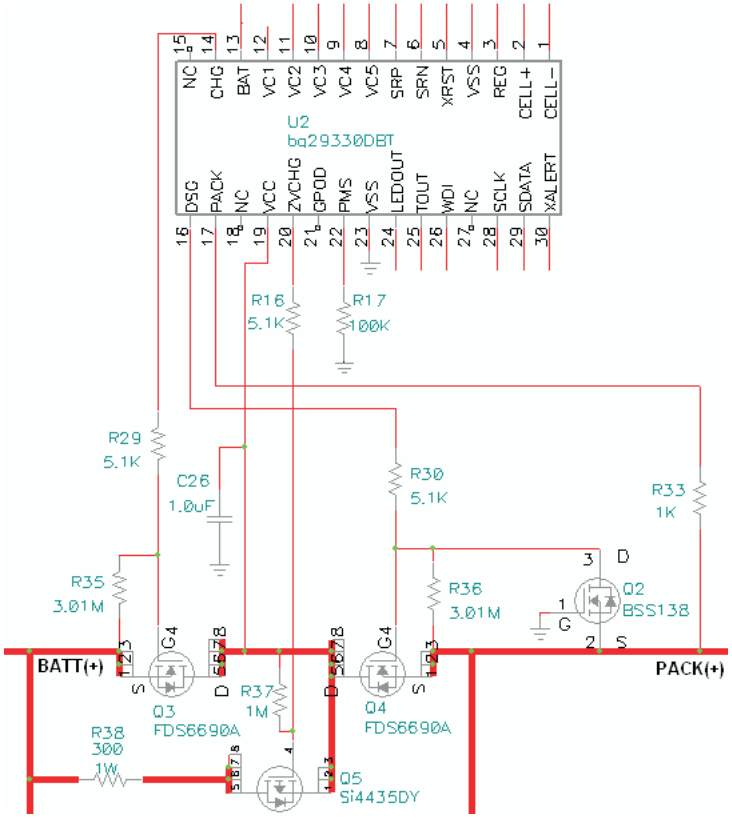


Figure 14. PACK, VCC, PMS Inputs, and FET Control

The N-channel charge and discharge FETS are controlled with 5-kΩ series gate resistors, which provide a switching time constant of a few microseconds. The 3-MΩ resistors ensure that the FETs are off in the event of an open connection to the FET drivers. The precharge FET, if used, is a P-channel device.

Q2 is provided to protect the discharge FET (Q4) in the event of a reverse-connected charger. Without Q2, Q4 can be driven into its linear region and suffer severe damage if the PACK+ input becomes slightly negative. Q2 turns on in that case to protect Q4 by shorting its gate to source. To use the simple ground gate circuit, the FET must have a low gate turnon threshold. If it is desired to use a more standard device, such as the 2N7000, the gate should be biased up to 3.3 V with a high-value resistor.

The PMS pin, depending on the desired precharge operating mode, should be tied to ground or PACK through a 100-kΩ resistor.

Regulator Outputs

Two low dropout regulators within the bq29330 require capacitive compensation on their outputs. The 2.5V REG output should have a 1-µF ceramic capacitor placed close to the IC terminal. The LED output requires a ceramic capacitor, even if no LEDs are used in the application. Use a 2.2-µF capacitor for a no-LED design and a 4.7-µF capacitor if LEDs are used.

Temperature Output

TOUT (pin 25) provides thermistor drive under program control. The reference design includes two 10-kΩ thermistors, RT1 and RT2. The 1% resistors are optimized for the recommended Semitec NTC103AT, or equivalent thermistor. Because these thermistors are normally external to the board, the ceramic capacitors are provided for ESD protection and measurement smoothing.

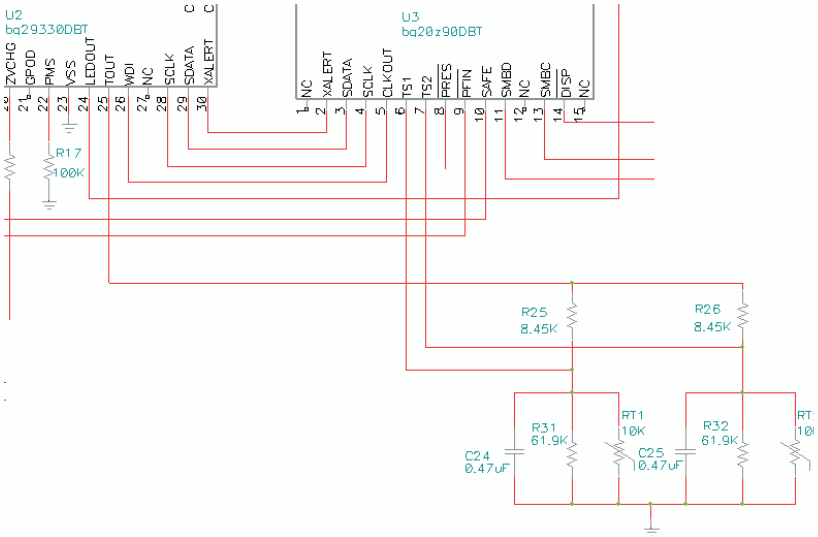


Figure 15. Thermistor Drive

Cell Voltage Output

The differential CELL+ and CELL– outputs require a 0.1-µF ceramic capacitor to stabilize the output amplifier in the bq29330 and provide the required filtering for the switched capacitor input of the gas gauge A/D converter.

17.5 Secondary-Voltage Protection

The bq29412 provides secondary-overvoltage protection and commands the chemical fuse to ignite if any cell exceeds the internally referenced threshold. The peripheral components are Cell Inputs and Time Delay Capacitor.

Cell Inputs

An input filter is provided for each cell input. This is comprised of resistors R2, R5, R6, and R8 along with capacitors C2, C4, C8, and C9. Note that this input network is completely independent of the filter network used as input to the bq29330. To ensure independent safety functionality, the two devices must have separate input filters.

Note that because the filter capacitors are implemented differentially, a low-voltage device can be used in each case.

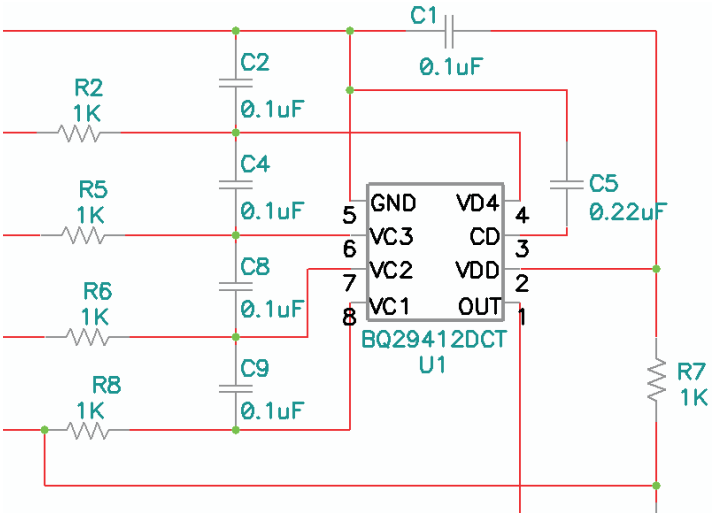
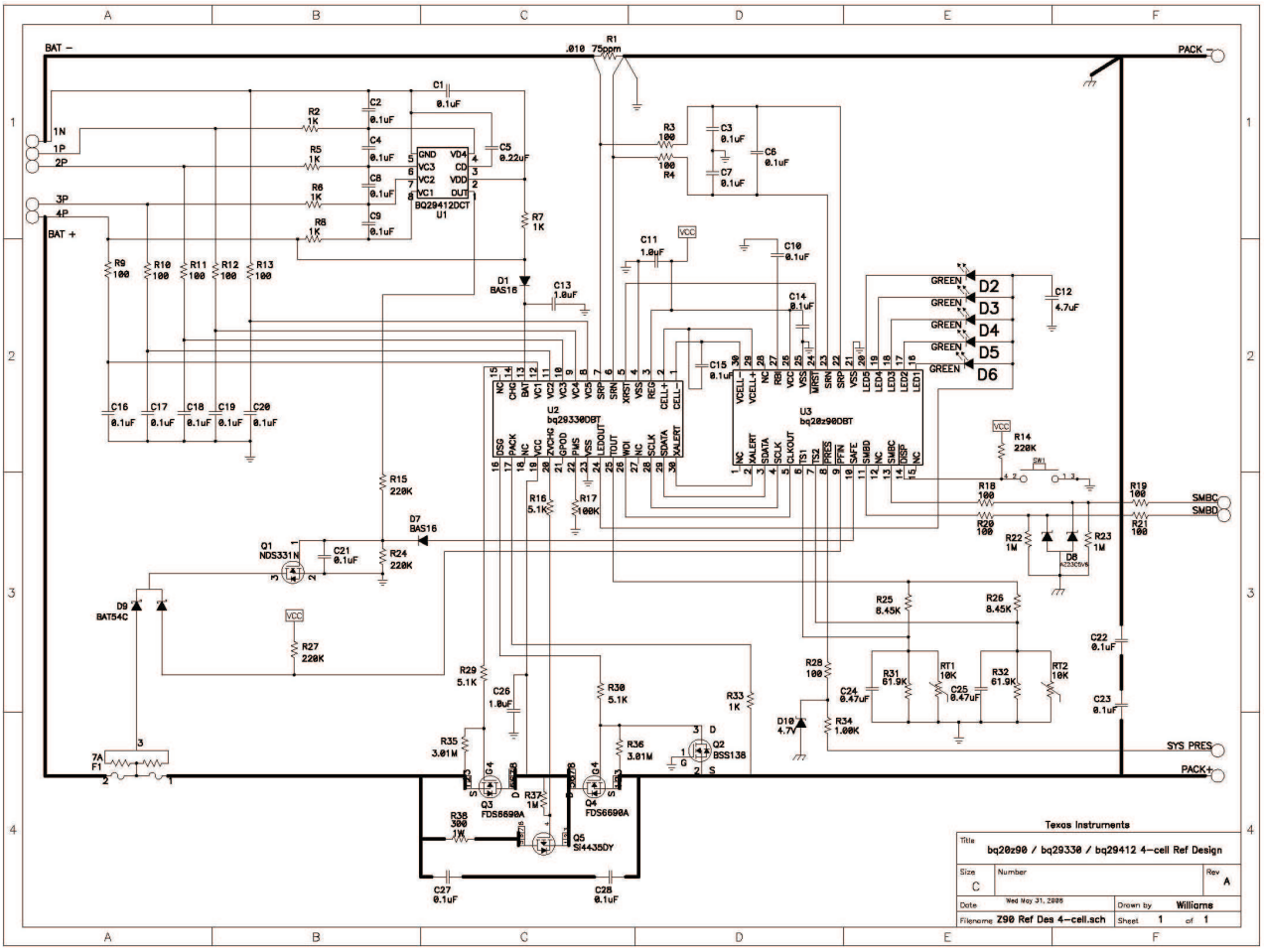


Figure 16. bq29412 Cell Inputs and Time-Delay Capacitor

Time-Delay Capacitor

C5 sets the time delay for activation of the output after any cell exceeds the threshold voltage. The time delay is calculated as td = 1.2 V × DelayCap(μF) / 0.18 μA.

17.6 Reference Design Schematic



Avoiding ESD and EMI Problems in bq20zxx Battery Pack Electronics

Doug Williams *Battery Management*

ABSTRACT

In an increasingly wireless world, electrostatic discharge and electromagnetic interference are both potential issues for portable battery packs. This application report discusses the causes of ESD and EMI issues in battery pack designs and offers solutions for mitigation.

18.1 Introduction

Electrostatic discharge (ESD) and electromagnetic interference (EMI) are both potential issues for portable battery packs in an increasingly wireless world. The bq20zxx Impedance Track™ advanced gas gauge family chipsets are based on a low-power microcontroller, which must be protected from severe outside disturbances. For a robust design, careful PCB layout and various mitigation techniques are necessary considerations.

18.2 Watery Grave

In the June 23, 2005 edition of EDN magazine, Howard Johnson, Ph.D., wrote an article entitled *Watery Grave*. In the article, he presented the scenario of a person on a lake, in an aluminum canoe, as a terrible thunderstorm was approaching. Given the following three choices, the reader was asked to select the one that would afford the best chance for survival (assuming there would not be a direct hit, which would be fatal in any case).

1. Stay in the canoe
2. Swim to shore
3. Invert the canoe and dive under it for protection (it becomes a Faraday shield)

The correct answer, of course, is to stay in the canoe because the hull of the boat would divert the current around the person. The same strategy could be used to protect integrated circuits inside a battery pack from the miniature lightning of an ESD hit. If the pack could be fitted with a metal case, the solution would be clear. Although the solution with the standard plastic case is not quite so obvious, the method is still the same — the current must be diverted around the unit to be protected.

For an EMI attack, the analogy holds also. RF energy can arrive by either radiation or conduction. Using shielding or bypass techniques, the energy must be diverted around the vulnerable semiconductor structures which can rectify the RF into lower frequency signals able to interfere with system operation.

18.3 Follow The Electrons

Figure 1 represents the general model for battery pack cells, electronics, and the pack connector. The BMU, or *battery management unit*, is comprised of various integrated circuits and peripheral components in the fuel gauge and safety circuitry design. This model is used to trace the flow of current during an ESD hit and an attack by heavy RF field intensity.

The Li-ion cells, protection FETs, sense resistor, and the pack connector surround the BMU. The single RC filter to the left of the BMU represents one of several connections, which monitor the voltage of each cell. The connections below the BMU represent various connections from the electronics to the common ground point, which is usually located on the PACK— side of the sense resistor. The resistors and zener diode to the right of the BMU represent the typical protection network for one of the communication lines.

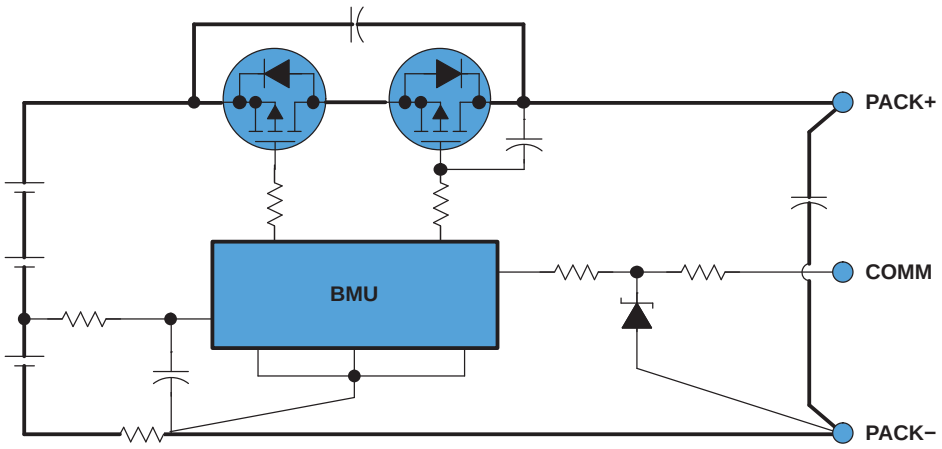


Figure 1. Basic Battery Pack Block Diagram

During an electrostatic discharge from a human body onto the battery pack connector, the current from the charged source tends to flow into the largest available capacitance, which is that of the cells themselves with respect to ground. Naturally, most of the current tends to take the path with the lowest impedance. Wide copper traces, with their low resistance and inductance, become the *diverters*— able to protect the sensitive electronics from grave danger.

In Figure 2 and Figure 3 can be seen the preferred diverting path for a zap to Pack+ and Pack–.

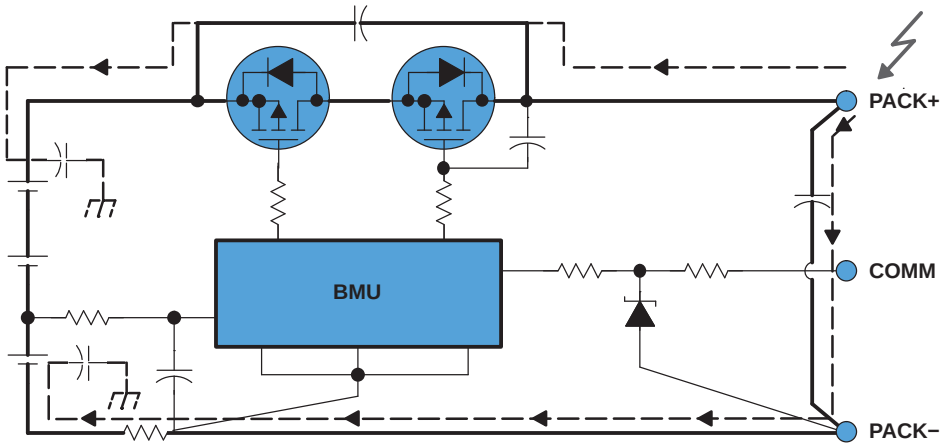


Figure 2. ESD Hit to PACK+ Connector Pin

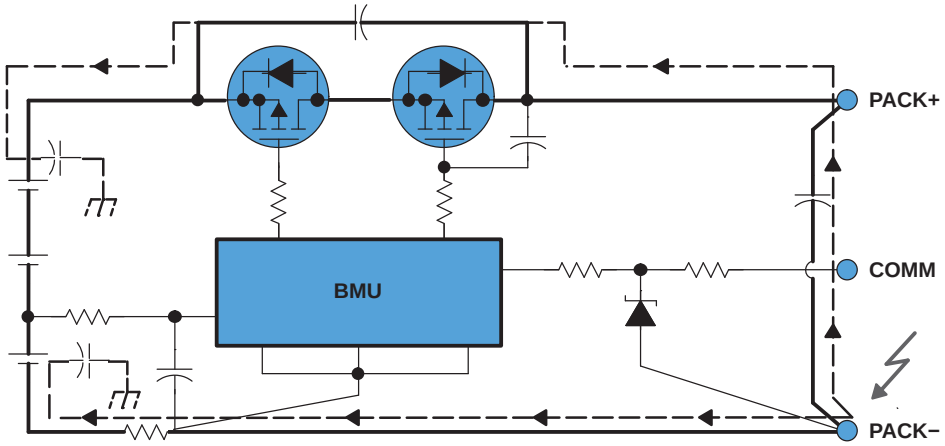


Figure 3. ESD Hit to PACK– Connector Pin

In both cases, the preferred path is similar. The copper to the FETS is wide, but then what? The capacitor (usually two in series in the event that one shorts) across the FETS helps to protect them. But this can only be realized if the copper traces to the capacitor are also wide enough to offer the required low resistance and inductance.

The capacitor (again, usually two in series) between Pack+ and Pack– is equally critical. It is desirable that current from a hit to Pack+ be diverted, as much as possible, away from the FETS and their associated nodes, which lead into the electronics. The copper between the pack connections and the capacitor(s) must be short and thick.

For a zap to a communications pin, again it is desirable to provide a low impedance path to the cell capacitance. In Figure 4, it can be seen that the desired current path is through the first series resistor, through the capacitance of the zener diode, then on to the wide PACK– copper trace. Keeping the zener close to the pack connector and using sufficient copper width ensures that the BMU is protected. In the case of a negative polarity zap, current flows out of the BMU in parallel with current through the zener. The resistor on the BMU side limits the ESD current to a safe level.

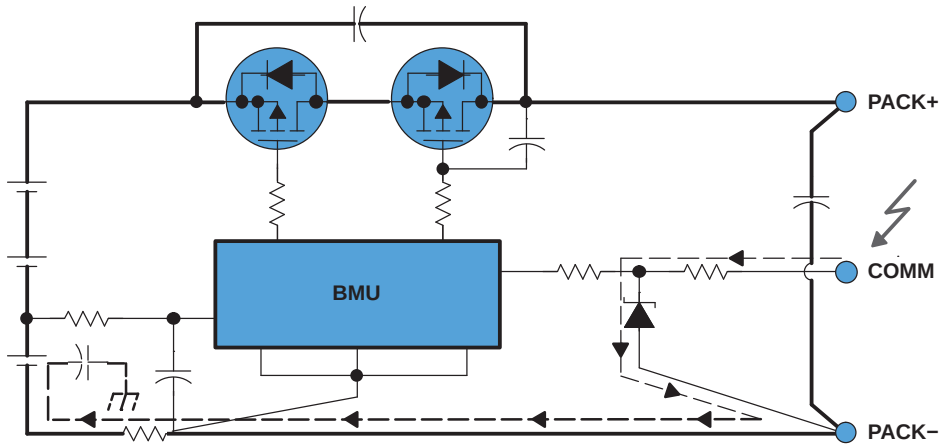


Figure 4. ESD Hit to the CLOCK or DATA Connector Pin

18.4 Keep ICs Off the Electron Highway

Whereas wide traces help to lower the inductance of copper traces, they still appear quite inductive at ESD pulse frequencies. At high frequencies, the diverting path can act as the primary of a current transformer, injecting unwanted and potentially disruptive currents into adjacent copper loops which feed into sensitive (ultralow power!) electronics.

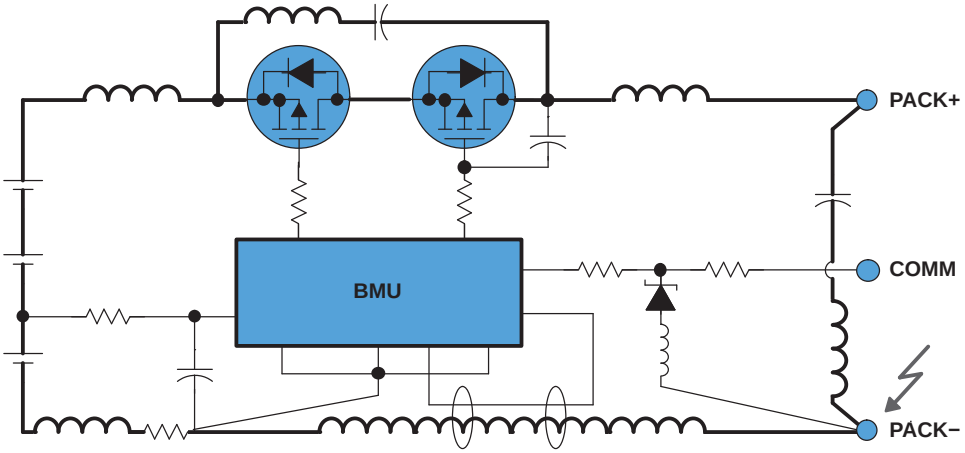


Figure 5. High-Frequency Currents From ESD or Inrush Can Be Inductively Coupled

The best defense against this sort of assault is to physically separate the high-current path from the sensitive electronics. Although this may not be feasible in many battery pack designs, it is an ideal goal for rugged design. High-current inrush pulses and ESD pulses do not mix well with ultralow power electronics. Both inductive and capacitive coupling must be considered in the layout.

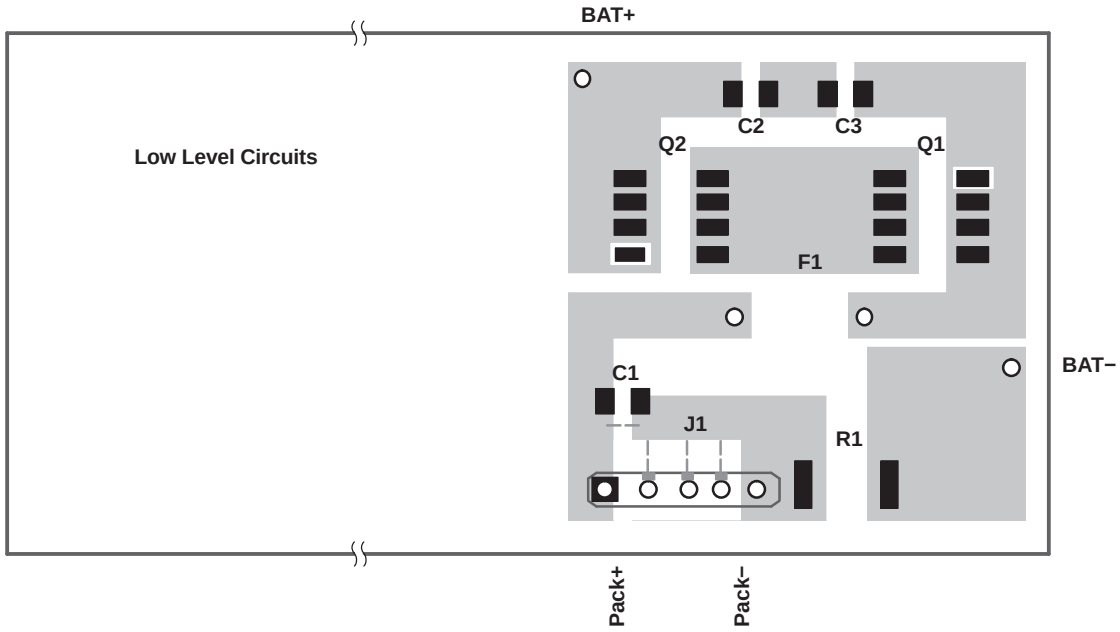


Figure 6. The Ideal Layout Separates the High-Current Path From the Low-Current Electronics

18.5 Separate Low-Level Ground Systems

Because e = L di/dt, and the derivative of the current is still quite large, significant voltages can be generated along the diverting current path. This is one of the reasons for using a separate low-level ground system with a single-point connection at the sense resistor. This avoids damage to the integrated circuits from circulating currents in the ground system during an ESD event . See Figure 7 and Figure 8.

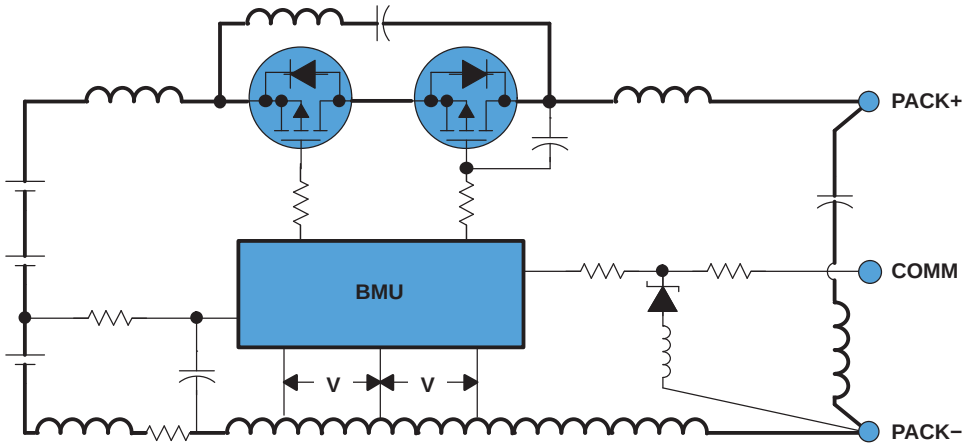


Figure 7. BMU Electronics Can Be Disrupted and Damaged From Circulating Ground Currents

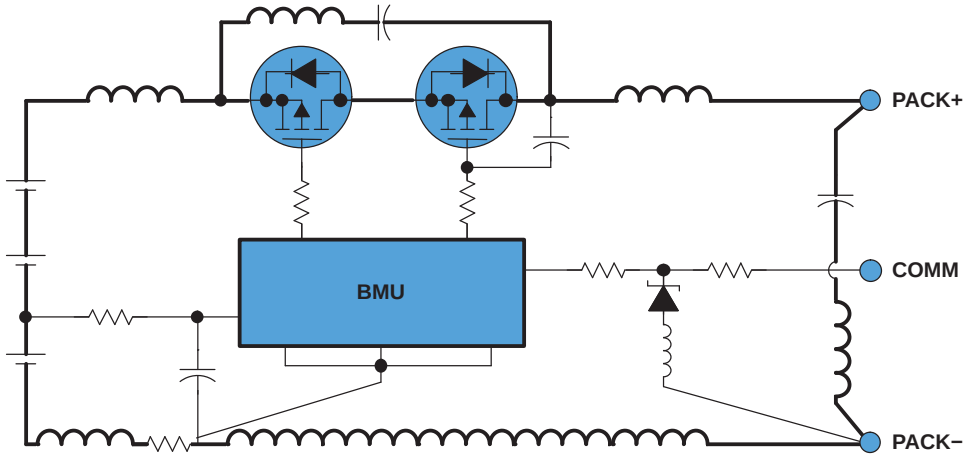


Figure 8. Correct BMU Grounding Is Separated From PACK– Except at the Single Connection at the Sense Resistor

18.6 Spark Gaps

Spark gaps are quite effective, especially for protecting the communication lines from ESD hits. Use the pattern as shown in the figure below, with a 10-mil (0,2-mm) gap. This provides a voltage breakdown at sea level of about 1500 V. For maximum effectiveness, the spark gaps must be on an outer layer of the PC board and should not be coated with any protective covering.

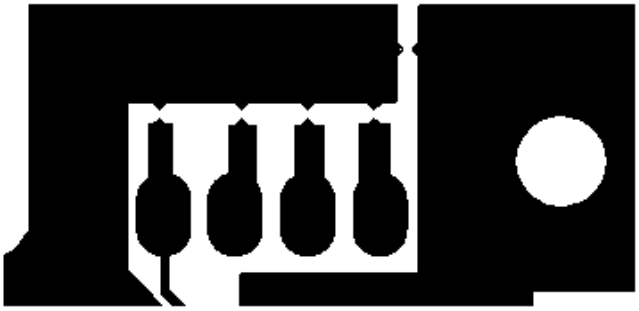


Figure 9. Recommended Spark Gap pattern on Battery Pack Connector

18.7 RF Bypassing

Perhaps the best way to understand RF interference is with the *crystal set* analogy. All semiconductors behave as diodes and rectify RF signals as with the simple demodulation of AM radio and TV picture transmission. The RF energy can be transported into a battery pack by either radiation or conduction. The cells and their leads can act as an antenna, or copper traces on the PC board itself can be the receiving antenna. Antennas are most effective at multiples of their length. A cell phone operating at 1800 MHz has a fundamental wavelength of 16.7 centimeters. A nice half-wave antenna would be 8.3 cm, while an effective quarter-wave antenna is only 4.2 cm. For this reason, RF testing of a new battery pack design is highly recommended to ensure its dependability in common RF environments, such as cell phones and other two-way radios.

Rectified RF can cause a number of problems including voltage, temperature, and current measurement errors. Also, microcontroller mis-operation and unintended fuse blowing are possible.

If any of these effects are observed during testing, it may be relatively easy to bypass the receiving semiconductor input with one or more small ceramic capacitors. Capacitors in the 68-pF to ~100-pF range have a low shunt impedance at VHF and UHF radio frequencies.

bq20z70/90 Printed-Circuit Board Layout Guide

Doug Williams *Battery Management*

ABSTRACT

Attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that can be challenging to solve. This application report presents guidelines to ensure a stable and well-performing project.

19.1 Introduction

Attention to layout is critical to the success of any battery management circuit board. The mixture of high-current paths with an ultralow-current microcontroller creates the potential for design issues that are not always trivial to solve. Careful placement and routing with regard to the principles described in the following text can ensure success.

19.2 IC Orientation

The design of the pinouts has been improved to simplify the printed-circuit board layout. The recommended orientation of the two ICs is shown in Figure 1. With this technique, a board that required four layers with previous chipsets of bq20z80/bq29312 or bq208x/bq29312 can often be designed on only two layers.

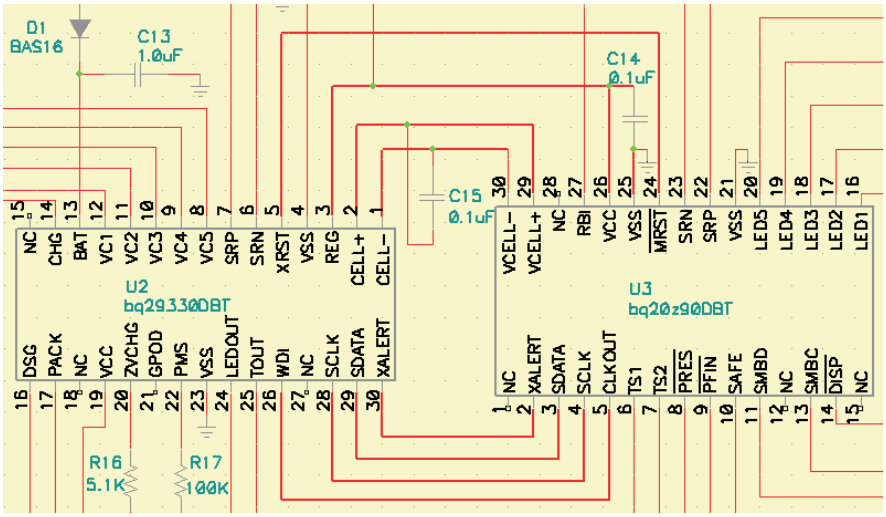


Figure 1. Orient the Chipset to Take Advantage of Easy Interconnection

19.3 bq20z70/90 Power Supply Decoupling Capacitor

Power supply decoupling from V_{CC} to ground is important for optimal operation of the bq20z70/90 advanced gas gauge. To keep the loop area small, place this capacitor next to the IC and use the shortest possible traces. A large-loop area renders the capacitor useless and forms a small-loop antenna for noise pickup.

Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSS pin to a ground plane layer.

Placement of the RBI capacitor is not as critical. It can be placed further away from the IC as shown in Figure 2.

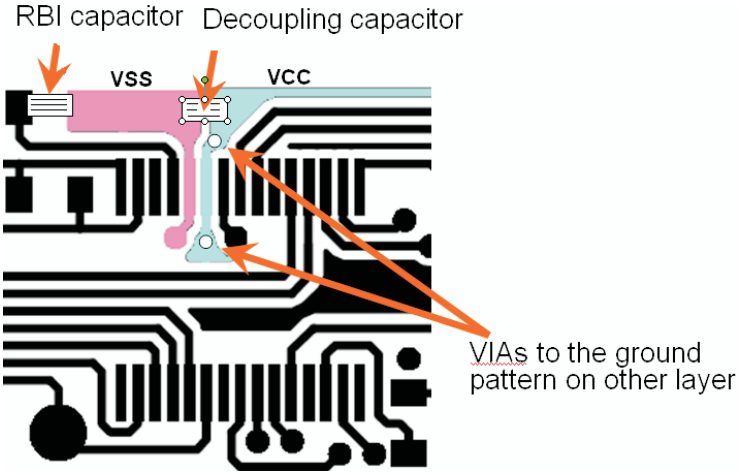


Figure 2. Recommended Placement of Decoupling and RBI Capacitors

19.4 bq29330 AFE Capacitors

Power supply decoupling for the bq29330 requires a pair of 1-µF ceramic capacitors from pin 13 (BAT) and pin 19 (VCC). These should be placed reasonably close to the IC, without using long traces back to VSS on pin 23.

The 3.3-V LED output requires a 4.7-µF ceramic capacitor when LEDs are used, but still requires 2.2-µF for loop stability when LEDs are not used, as with the bq20z70. This capacitor also should be placed as close as is practical to the IC.

The LDO voltage regulator within the bq29330 requires a 1-µF ceramic capacitor to be placed fairly close to the REG pin. This capacitor is for amplifier loop stabilization as well as an energy well for the 2.5-V supply.

Unwanted ESD hits to the AFE can have undesirable effects. Although the bq20z70/90 firmware has built-in routines to repair unwanted alteration of the internal registers, it is not easy to protect against an unwanted LDO shutdown, which would require application of the charger to restart the gas gauge. It has been experimentally determined that the placement of the capacitor on the REG pin can be helpful in diverting ESD current away from the AFE. The idea is to place the ground of the REG capacitor between the device ground and PACK(–) as shown in Figure 3. With this method, the capacitor absorbs an ESD hit to PACK plus, preventing unwanted LDO turnoff. The layout of Figure 4 is not recommended.

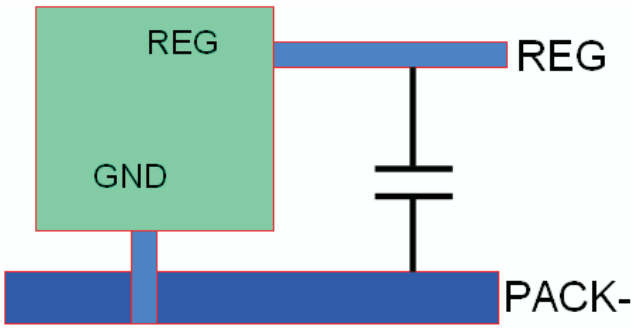


Figure 3. Preferred Method. Capacitor Absorbs Incoming ESD From PACK(–)

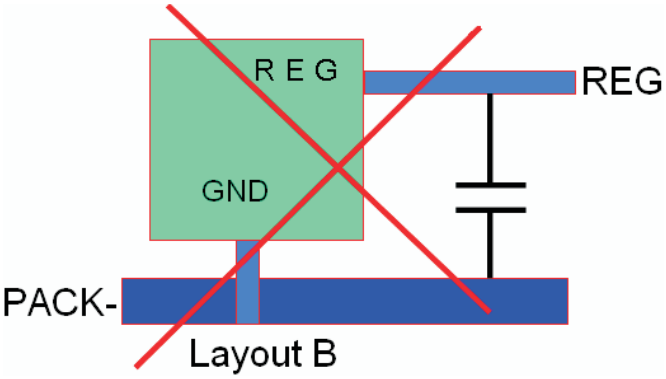


Figure 4. ESD From PACK– Can More Easily Affect Internal Registers

19.5 MRST Connection

XRST (AFE) and MRST (GG) are connected to allow the AFE to control the gas gauge reset state. The connection between these pins must be as short as possible in order to avoid any incoming noise. With the recommended orientation of the two ICs, direct interconnection will not cause a problem. If unwanted resets are found, one or more of the following solutions may be effective:

- Add a 0.1-µF capacitor between MRST and ground.
- Provide a 1-kΩ pullup resistor to 2.5 V at MRST.
- Surround the entire circuit with a ground pattern.

Again, these steps are not normally required if the ICs are located close together. If a test pin is added at MRST, it should be provided with a 10-kΩ series resistor.

19.6 Communication Line Protection Components

The 5.6-V Zener diodes, used to protect the communication pins of the bq20z70/90 from ESD, should be located as close as possible to the pack connector. The grounded end of these Zener diodes should be returned to the Pack(–) node, rather than to the low-current digital ground system. This way, ESD is diverted away from the sensitive electronics as much as possible.

19.7 Protector FET Bypass and Pack Terminal Bypass Capacitors

The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuit. In Figure 5, an example layout demonstrates this technique.

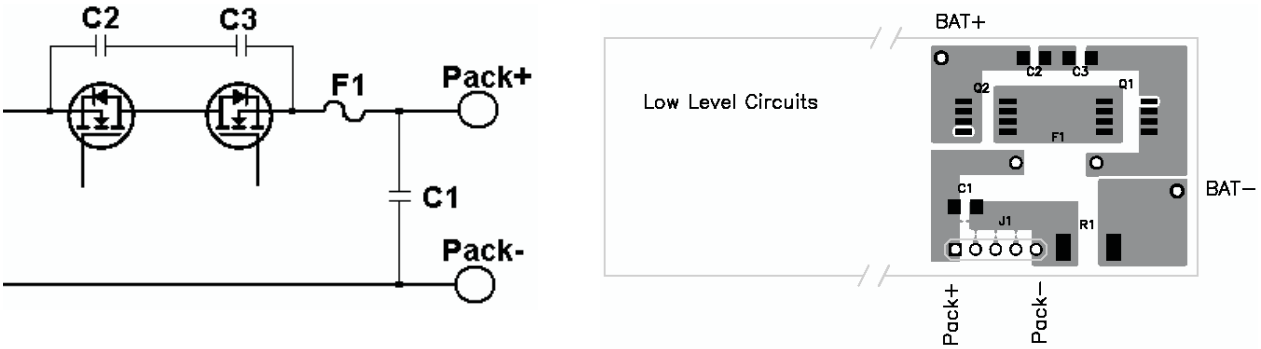


Figure 5. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, and C3

19.8 Ground System

The bq20z70/90 and bq29330 require a low-current ground system separate from the high-current PACK(-) path. ESD ground is defined along the high-current path from the Pack(–) terminal to the sense resistor. See the ground symbols in the bq20z70/90 reference design, and provide the separate low-current ground system accordingly. It is important that the low-current ground systems only connect to PACK(–) at the sense resistor Kelvin pick-off point as shown in Figure 6. The use of an optional inner layer ground plane is recommended for the low-current ground system.

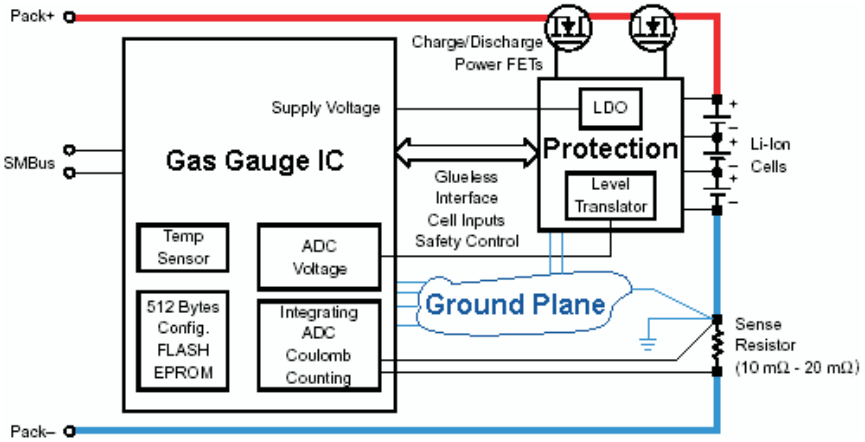


Figure 6. ICs Use a Low-Current Ground System. Ground Plane is Optional.

19.9 Kelvin Connections

Kelvin voltage sensing is extremely important in order to accurately measure current and top and bottom cell voltages. Figure 7 and Figure 8 below demonstrate *correct* and *incorrect* techniques.

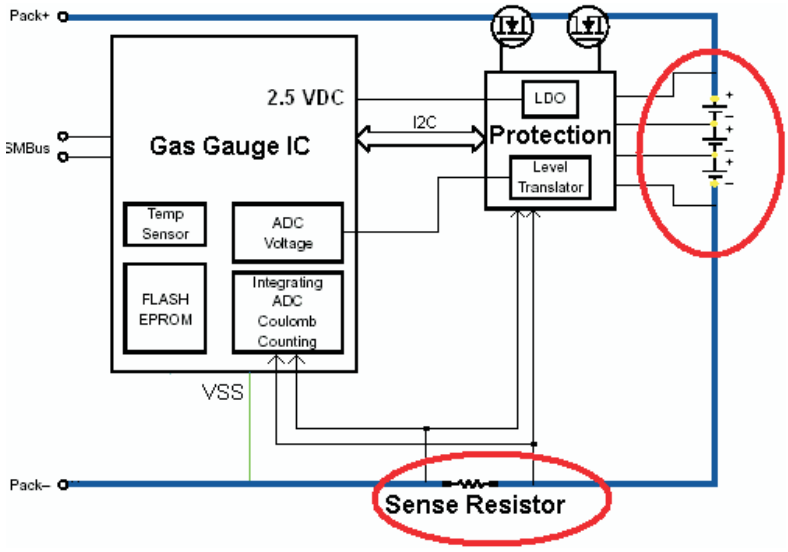


Figure 7. Incorrect: Sensing Through High-Current Copper Traces Produces Measurement Errors

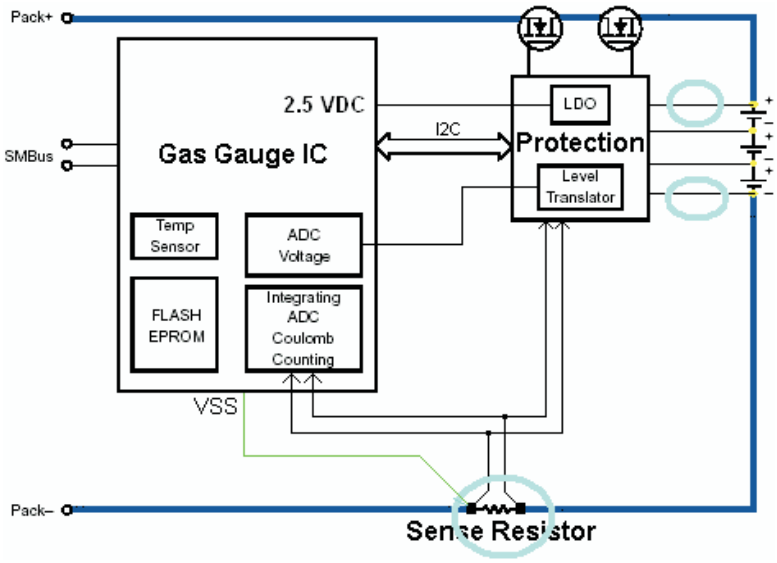


Figure 8. Correct: In Some Cases, Top and Bottom Cell Voltage Sensing May Be Extended Out to Cells

19.10 Board Offset Considerations

Although the most important component for board offset reduction is the decoupling capacitor for Vcc, additional benefit is possible by using this recommended pattern for the Coulomb Counter differential low-pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100-Ω resistors as shown in Figure 9.

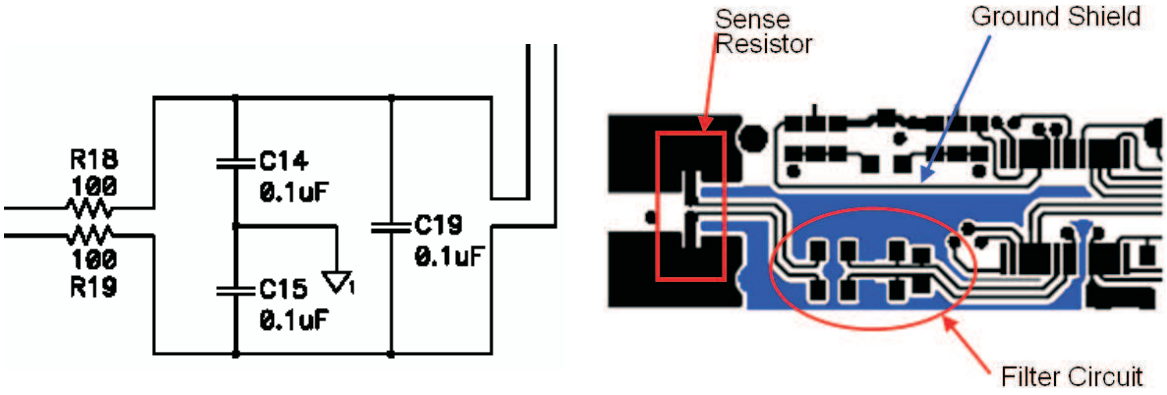


Figure 9. Differential Filter Components With Symmetrical Layout

19.11 ESD Spark Gap

Protect SMBus Clock, Data, and other communication lines from ESD with a spark gap at the connector. The pattern below is recommended, with 0.2-mm spacing between the points.

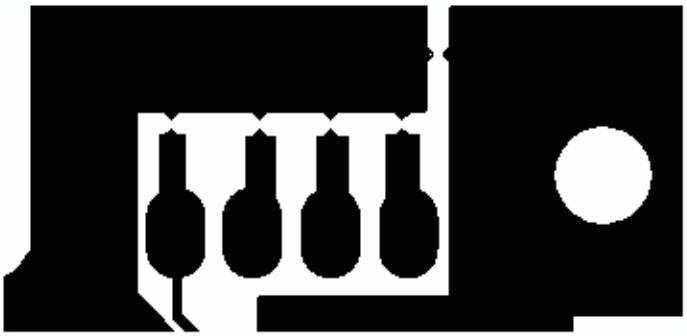


Figure 10. Recommended Spark-Gap Pattern Helps Protect Communication Lines From ESD.

19.12 Radio Frequency Interference

Normally, strong RF signals have no effect on gas gauge performance. However, it should be understood that any silicon structure can rectify RF signals, producing unwanted voltages and currents at critical nodes. The most vulnerable node on the bq20z70/90 reference design is the SAFE output, which feeds into a signal diode, followed by an FET gate and shunt capacitor. This type of network demodulates an RF signal and can produce enough DC on the gate of the fuse ignition FET to actually blow the fuse. The solution is to keep the trace from the SAFE output to the diode as short as possible to reduce its effectiveness as an antenna. Alternately, both sides of the trace can be guarded with grounded copper.

19.13 Unwanted Magnetic Coupling

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high-current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement such as that shown in Figure 11, where the high-current section is on the opposite side of the board from the electronic devices. Clearly this is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high-current traces away from signal traces, which enter the bq20z70/90 directly.

IC references and registers can be disturbed and in rare cases damaged due to magnetic and capacitive coupling from the high-current path. Note that during surge current and ESD events, the high-current traces appear inductive and can couple unwanted noise into sensitive nodes of the gas gauge electronics, as illustrated in Figure 12.

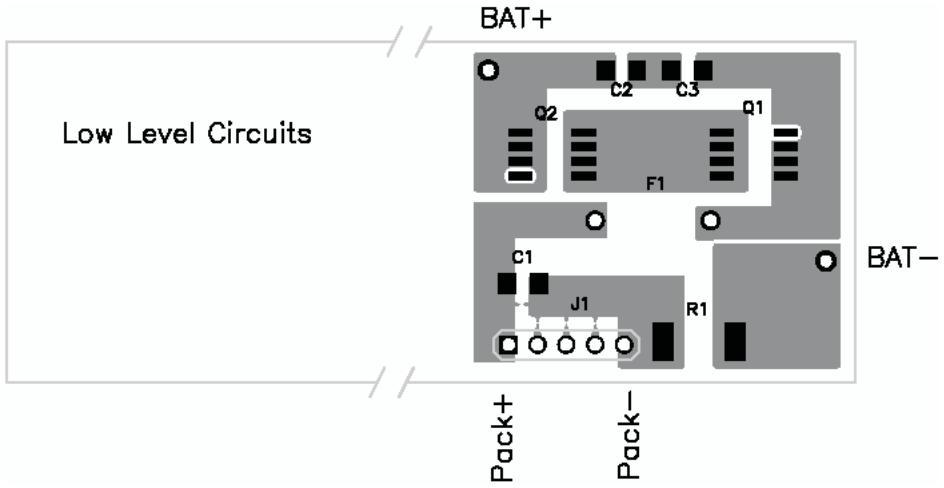


Figure 11. Separating High- and Low-Current Sections Provides an Advantage in Noise Immunity

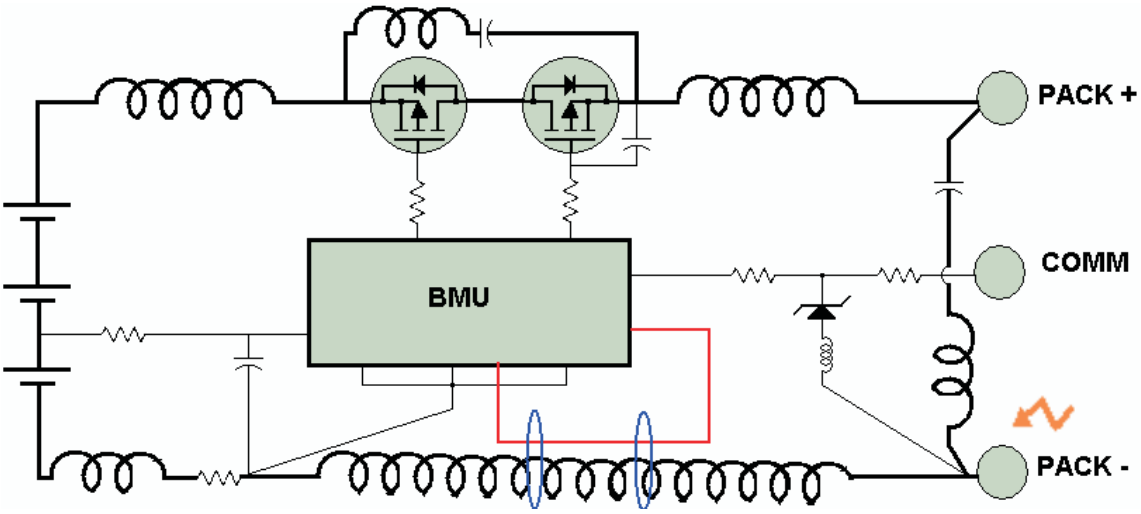


Figure 12. Avoid Close Spacing Between High-Current and Low-Level Signal Lines

Cell Balancing Using the bq20zxx

Yevgen Barsukov *PMP Portable Power*

ABSTRACT

This application report discusses three types of cell imbalances that are observed in a battery pack with serially connected cells.

20.1 Types of Cell Imbalances

1. **State of Charge Imbalance**

   Charging cells to different states of charge (SOC) causes this type of imbalance. For example, given a configuration of 3 x 2200-mAh cells (QMax), if one cell is discharged by 100 mAh (Q1), the second by 100 mAh, and the third by 200 mAh from a fully charged state, the first and second cells' chemical state of charge is (Qmax-Q1)/Qmax = 95.4%, but the third cell is 91%. Therefore, cell 3 is imbalanced by 4.4%.

   This results in a different open-circuit voltage (OCV) for cell 3 compared to cells 1 and 2, because the OCV directly correlates with the chemical state of charge.

2. **Total Cell Capacity Imbalance**

   A specific cell's total chemical capacity, Qmax, initially may be different from the others in the cell package. So, even if all cells were discharged by an equal amount from a fully charged state, their chemical states of charge may be different. Indeed, if all 3 cells are discharged by 100 mAh, but cell 3 has different total capacity (e.g., 2000 mAh), the resulting chemical states of charge is 95.4% and 95%.

   This results in different OCVs. A 200-mAh difference in Qmax causes only a 0.4% difference in SOC because the SOC correlates with voltage. This indicates that the capacity imbalance causes less voltage difference than charge imbalance (cause 1).

3. **Impedance Imbalance**

   Internal impedance differences between the cells (that can be an approximate 15% range in the same production batch) do not cause differences in the OCV. However, they can cause differences in cell voltage during discharge. Indeed, cell voltage can be approximated as $V = OCV + I \times R$. If current is negative (discharge), voltage is lower for a cell with higher R. If current is positive (charge), voltage is higher for a cell with higher R.

   No balancing algorithm can help against resistance imbalance. However, it can significantly distort attempts to balance the SOC. If significant (< 200 mA) current is flowing, attempting to use voltage as a determining factor for passing more charge through a cell with higher voltage, fails to determine if the voltage differences is caused by differences in the SOC or by impedance. If it is caused by impedance imbalance, bypassing more current through this cell results in the opposite effect – increasing the SOC difference from other cells to a larger value than it would be without balancing. As a result, the OCV of this cell at the end of charge is different from the other cells, and can reach high levels, potentially causing the safety circuit to trip.

20.2 Cell Balancing Methods

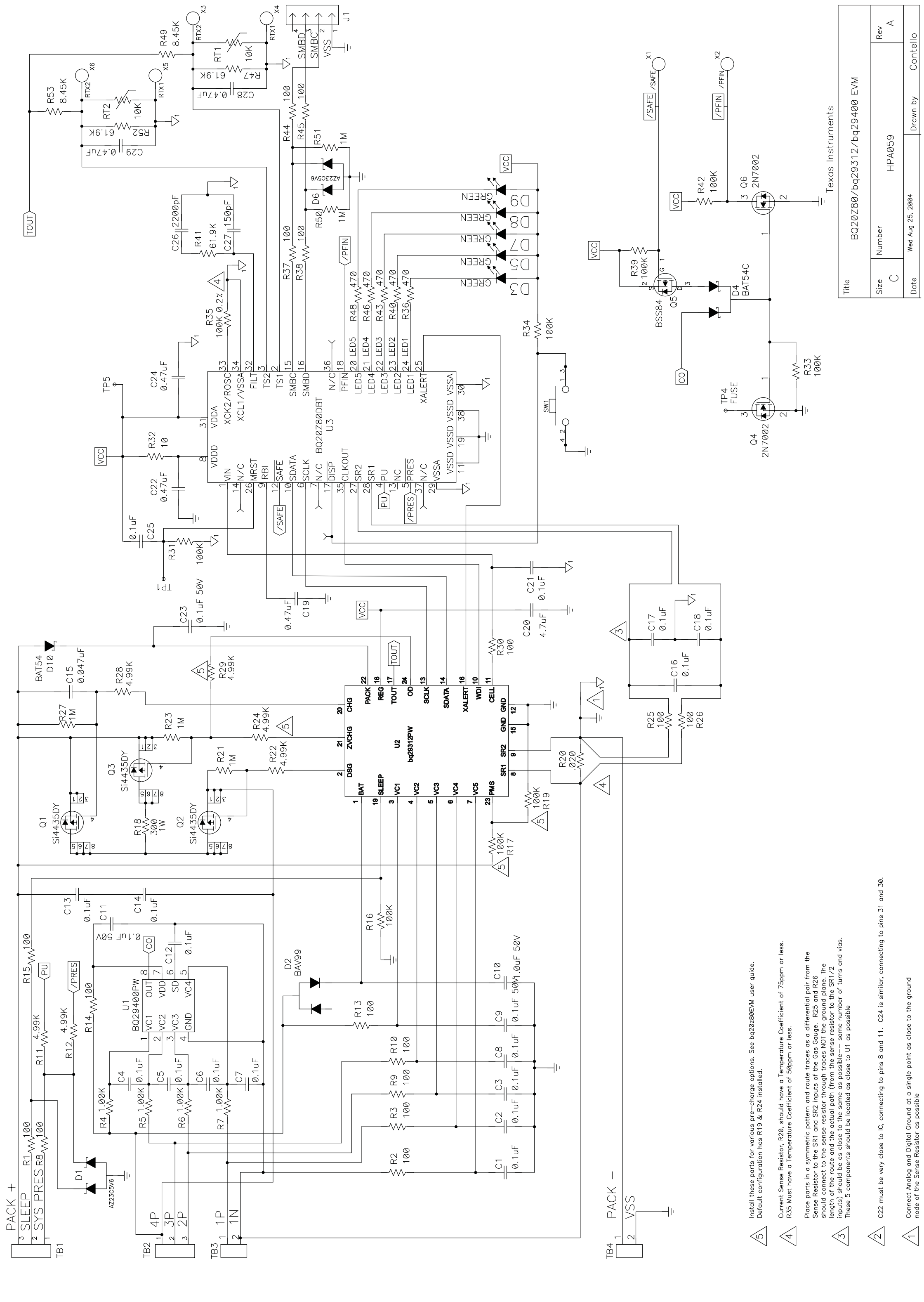
The bq20zxx uses the unique capabilities of Impedance Track™ technology to identify the chemical SOC of each cell, which does not rely on measuring voltage during charge or discharge. This removes the distortion caused by impedance imbalance, and permits precise SOC balancing. The cell-balancing algorithm operates as follows:

1. Determine the initial SOC for each series cell bank separately.
2. Determine the charge needed for each cell to reach a fully charged state.
3. Find the cell requiring the most charge to be fully charged, and then find the differences, dQ, between all the other cells requiring charge and that of the one requiring the most charge.
4. These differences must be bypassed for each “excessive” cell during one or multiple cycles. To achieve this, the bypass FET is turned ON during charging for the calculated duration for each cell bypass time.
5. The bypass time is calculated based on the value of bypass current, which in turn depends on bypass resistance values, R, as time = $dQ \times R / (V \times duty\_cycle)$.
6. R is calculated as the sum of the internal bypass resistor (500 Ω, typical) and the series filter resistors (Rx) leading to the cells. $R = Rx \times 2 + 500$. The resistors in question are R2, R3, R9, and R10. Their default value is 100 Ω, which results in R = 700.

7. The bq20zxx stores the value of R(Ω) × 3.6 / (V × duty_cycle (ratio)) as a flash constant DF.MinCellDeviation (s/mAh). Here, 3.6 is the mAh correction factor. For default values of voltage, V = 3.6 V, R = 700 Ω and duty cycle = 40% (ratio 0.4), the value is calculated as DF.MinCellDeviation = 700 × 3.6 / (3.6 × 0.4) = 1750

This value must be changed if values of resistors R2, R3, R9, and R10 are changed from the default value.

The schematic appears on the following page.


Texas Instruments
BQ20Z80/bq29312/bq29400 EVM
HPA059
Contello

Support of Multiple Li-Ion Chemistries With Impedance Track™ Gas Gauges

Yevgen Barsukov *PMP Portable Power*

ABSTRACT

This application report describes the process of selecting the correct chemistry open-circuit voltage table for a particular cell and the method of correctly programming this information during production.

21.1 Introduction

Impedance Track™ devices rely on a fixed open-circuit voltage (OCV) table to determine the state of charge (SOC), where OCV(SOC) dependence is defined by cell chemistry. Impedance Track™ devices come preprogrammed to support the most common Li-ion cells with $LiCoO_2$ cathode and graphitized carbon anode. However, multiple other chemistries are grouped under *Li-ion*, two examples of which are Co/Mn oxide cathode cells and Ni/Co/Mn cathode cells. Therefore, Impedance Track™ devices have been designed with the ability to be programmed with any Li-ion chemistry OCV table. This application report describes the process of selecting the correct chemistry OCV table for a particular cell and the specifics of correctly programming this information during production.

21.2 Selection of Correct Chemistry

Chemistry Selection Table

Chemistries that are currently supported are listed in the table *Chemistry Selection* which can be found on the TI Web site, in the Tools and Software folder of the corresponding Impedance Track™-based device. The following is an example of the table format, which contains a sample of the data currently available. In the future, more entries will be added to this Web-based table as additional chemistries are identified.

Description	Chemical ID	Known Compatible Cells (Not Exclusive)
$LiCoO_2$/graphitized carbon (default)	**0100**	**Sony US18650S, Sony 18650GR, Moly ICR-18650G, Panasonic CGR-18650C, LG Chem ICR18650A2, LG Chem ICR18650S2, A&TB LGR18650OU, Samsung SDI ICR18650-20**
Co/Ni/Mn cathode	**0101**	**Sony SF US18650GR**
Hybrid Co/Mn oxide cathode	**0102**	**Sanyo-laminate**
$LiCoO_2$ ATL	**0103**	**ATL-laminate 554490**

Firmware Support for Different Chemistries

The firmware required to support the various chemistries is identical, and therefore, no firmware upgrades are required when programming new chemistries into the data-flash (DF) memory of the corresponding Impedance Track™-based device. As an added feature, the Chemical ID of currently programmed OCV data can be checked using TI's EV Software. This is accomplished by entering 0008 into the Manufacturer Access field in the SBS screen and pressing <enter>. The Chemical ID then is reported in the Manufacturer Access field. Note that scanning should be enabled.

21.2.128.5 Methods to Identify Chemistry of a Particular Cell

1. Ask the manufacturer. If the use of standard LiCoO2 can be ensured, then the default database with ID 0100 can be used without change.
2. Search for the cell part number, in the *Known Compatible Cells* column of the Chemistry Selection table provided by TI. If found, then the corresponding chemistry ID can be used.
3. In manufacturer information, search for a *Description* entry similar to that found in the Chemistry Selection table provided by TI. If a similar description is found, then the corresponding chemistry ID can be used.
4. If none of these methods are successful, then a chemistry selection test can be run to help select the best possible fit. Note that this is the most time-consuming option, which requires common

charge/discharge test equipment such as a Maccor or Arbin tester. However, it provides the highest confidence in a chemical database selection process. The chemistry selection test procedure is described in the Addendum *Chemistry Compatibility Check*.

Preproduction Testing With Nondefault Chemistry

Preproduction testing, using a nondefault chemistry, is the same as when using the default chemistry, with one exception – a new firmware file (*.senc) containing the OCV table specific for a particular chemistry has to be programmed into the pack first. Firmware files for selected chemistry IDs can be download from the *Tools and Software* folder of a corresponding Impedance Track™-based device. Programming of the firmware file using TI's EV Software is described in the application note *Updating Firmware With The bq20z80 and EVM* (SLUA336).

After the correct firmware file is programmed, the normal production process can proceed using the steps described in the application report *Pack Assembly and the bq20z80* (SLUA335). Note that prior to production, a relaxation/discharge/relaxation test should be done to acquire optimized parameters for use. This process is described in the application report *Preparing Optimized Default Flash Constants For Specific Battery Types* (SLUA334).

Production Process With Nondefault Chemistry

With the exception of preparing the data-flash image file, the general production process with nondefault chemistries is the same as with default chemistries, as described in the applications report *Data Flash Programming and Calibrating the bq20z80 Family of Gas Gauges* (SLUA355).

The additional steps required to prepare the data-flash image file follow.

1. Using an Impedance Track™-based device programmed with the corresponding chemistry specific firmware file (*.senc), complete the Battery Pack assembly steps, as outlined in the application report *Pack Assembly and the bq20z80* (SLUA335). Key steps include: setting basic flash constants for a given pack configuration; calibrating the pack; connecting System Present to ground; and enabling IT. It is also important to correctly set the parameters specific to the number of serial cells used. This is described in the application report *bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity* (SLVA208).
2. Input an initial estimate for QmaxCell 0, Qmax Cell 1, Qmax Cell 2, Qmax Cell 3, and Qmax Pack using the value specified in the battery manufacturer data sheet. For example, if single-cell data-sheet capacity is 2400 mAh and three parallel cells are used, set each value to 2400 $\times$ 3 = 7200 mAh.
3. Charge the pack to full.
4. Let the pack relax for 2 hours.
5. Discharge the pack to the minimum system-acceptable voltage (this should be the same as DF:Term Voltage) at the typical application rate. Note that the exact rate is not critical.
6. Let the pack relax for 5 hours.
7. Repeat steps 3 through 6 two times to achieve the maximum accuracy. Using the Data Flash screen in the EVSW, verify that *Update Status*, under the Gas Gauging tab, reads 06. If not, then repeat the cycle.
8. Use the EVSW to export the .gg file.
9. Open the .gg file with an application like Notepad and manually change the [IT Cfg(Gas Gauging)] *Update Status* to 02 and the [Data(SBS Configuration)] *Cycle Count* to 0. Save and close the .gg file
10. Reprogram the pack with a fresh firmware (*.senc) file with selected chemistry ID, to clear all hidden constants and set the correct chemistry specific table.
11. Use the Data Flash screen in the EVSW to import the modified .gg file, saved in step 9.
12. In the Data Flash screen of the EVSW click *Write All*
13. In the Pro screen of the EVSW, send the reset command (0x0041).

The golden pack is now ready to have its data flash read into a binary file, as described in Section 3 of the application report titled *Data Flash Programming and Calibrating the bq20z80 Family of Gas Gauges* (SLUA355).

Note that as an alternative option, small volume production facilities can use TI's single-channel prototype data-flash writing and calibration software called *bqTester*. The single site bqTester software can be downloaded directly form the TI Web site (see SLUA352). Ensure that the correct firmware version is input into the bqTester.ini file. For example for bq20z80-v102 set: DEV_VER_REV=800.1.02.

21.3 Addendum: Chemistry Compatibility Check

Setup

- Use a single cell, or an assembled battery pack without any electronics connected. This avoids any current draw and is important because this test takes an extended time and has long inactivity periods.
- Measure the voltage at a single cell (even if a battery pack is used)
- Current measurement accuracy is important. Especially, the current offset should be calibrated to better than a 1-mA accuracy.
- Voltage measurement accuracy is equally important and should be accurate to 1 mV (should be checked with a 0.1-mV accurate digital voltmeter).
- Configure a thermal chamber to 25°C. Note that testing at 0°C and 50°C is also required in order to create a database, but not for a compatibility check.
- Voltage, current, and temperature data should be collected with 10-s to 100-s intervals continuously during the test. The resulting file is used in the chemistry selection tool. Plain text files or Microsoft™ Excel spreadsheets are acceptable formats.

Automated Test (Can be Set Up Using Maccor or Arbin Battery Testers)

1. Charge the cell to full using the CC/CV method, and terminate the charge when taper current reaches C/100. This state of charge corresponds to full chemical capacity. Note that using the C/100 taper current is critical to ensuring an absolutely fully charged cell.
2. Turn off the current (ensure the actual current is below 1 mA) and wait 5 hours for full cell relaxation. If dV/dt smoothed over 100 s is available, wait can be terminated before 5 hours if dV/dt < 1 µV/s. This method helps speed up testing.
3. Discharge at C/20 rate for 1 hour, then go to step 2. If the voltage goes below 3 V, go to step 4.
4. Turn off the current (ensure actual current is below 1 mA) and wait 5 hours for full relaxation. If dV/dt smoothed over 100 s is available, wait can be terminated before 5 hours if dV/dt < 1 µV/s. This method helps speed up testing. Check the voltage after relaxation is terminated. If V < 3V, exit test; otherwise, proceed to step 5).
5. Discharge at C/60 rate for 30 min, or until V < 2.7 V; go to step 4.

Data obtained in this test is used in a Mathcad™ tool provided by TI. For database purposes, additional data at 0°C and 50°C is needed.

Using Mathcad™ Tool to Select Battery Chemistry

To use the chemistry selection tool, Mathcad™ 2001i or higher is needed.

Download the chemistry selection worksheet *chemselect.mcd* from *Tools and Software* folder of the corresponding Impedance Track™-based device, and then follow these steps to verify battery chemistry:

1. Remove the charge portion of the data-file acquired in the preceding testing.
2. Place the file in the same directory containing the *chemselect.mcd* file.
3. Open the chemistry selection file *chemselect.mcd.*
4. Assign columns to reflect your file format:

Columns assignment in data-file: time $tn := 0$ voltage $vn := 2$ temper $ttn := 100$ curr $in := 1$

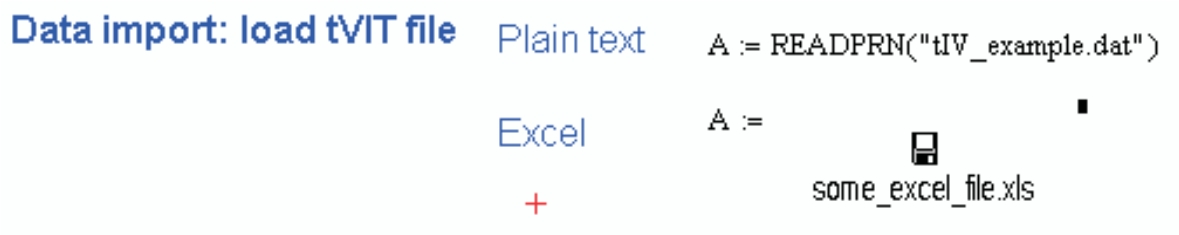
Change column numbers for time (tn), voltage (vn), temperature (ttn) and current (in). If temperature column is not available, set ttn:=100, and set correct chamber temperature in C in the following section:

temperature used in simulation of voltage
if no temperature is present in file. set
ttn=100 if not temperature info present

$T := 25$

$Tpres := T \cdot 10$

5. Enter your file name into data-loading section. You can try running the program with included example data-file *tIV_example.dat*.



   If the file is in Excel format, then right-click on the section to the right labeled *Excel* line, and click *enable evaluation*. If the file is in plain-text format, leave this section disabled. Note that, regardless, the file should not include any text headers, only data.
6. Scroll to the bottom of document, and click anywhere to place the cursor below all lines. Press F9 to execute all calculations
7. Read out the chemical ID best-suited for your battery:

Best chemistry ID

$bestchem = 103$

8. Analyze the reported error for best chemistry. If it is below 3%, this chemical ID firmware can be used with your chemistry:

$$maxerr = \begin{array}{cc} \text{error \%} & \text{ID} \\ \begin{pmatrix} 1.96682 & 103 \\ 3.937942 & 100 \\ 9.521751 & 101 \\ 17.384558 & 102 \end{pmatrix} \end{array}$$

In this example, the maximum error is 1.96% for chemical ID 103 where anything below 3% is acceptable. Therefore, the firmware file (*.senc) for chemical ID 103, should be downloaded and used.

If *maxerr* for all chemical IDs exceeds 3%, a new chemical table needs to be created. To facilitate this, repeat the *Automated test* for the additional required temperatures of 0°C and 50°C. Then contact Texas Instrument support at http://www-k.ext.ti.com/sc/technical-support/product-information-centers.htm or the local sales representative. Using this data, TI will create a new chemical database. Alternatively, the cells can be sent directly to TI for evaluation/characterization but this process takes longer.

Battery Pack Production Flow With bq20zXX

Yevgen Barsukov *Battery Management*

22.1 Introduction

A battery pack production flow diagram for bq20zXX devices is shown in Figure 1. Each production step shown in the diagram is discussed in detail in this application report.

Production Flow Diagram

This diagram presents the steps needed for the gas-gauge operation along with optional steps, which are commonly used by battery pack makers, but are not required for gas-gauge operation. The following sections provide detailed description of each step.

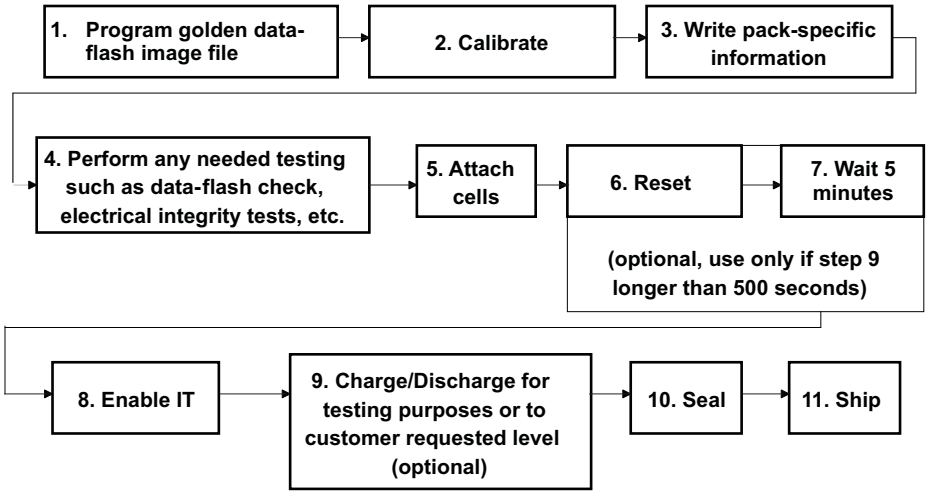


Figure 1. Flow Diagram

22.2 Detailed Description of Production Steps

Step 1: Program Golden Data-Flash Image File

A golden data-flash image is prepared during the characterization step as described in application report SLUA380 for the bq20z80 or in application report SLUA379 for the bq20z70/z90. The golden data-flash image contains data-flash settings customized for each particular device, resistance profiles optimized for a given battery, and multichemistry specific data.

Both programming of the data-flash image and calibration can be performed using example software created by Texas Instruments called bqMTester that can be downloaded from the power.ti.com bq20z80 tools and software folder. This software supports up to 12 simultaneous calibrations. It requires the EV2300 SMB interface and a calibration board (stable voltage and current source) per simultaneous calibration which can be purchased from TI or built using the provided schematics.

For a small-size production or test purposes, a single-channel bqTester can be used. It is downloadable from the bq20z80 folder as source file to application report *Using the BQTester Software* (SLUA352). It requires only the EV2300, but the user's own current and voltage source needs to be used. Source code for both these programs can be obtained by request to a local TI sales representative for the user's own modification.

Users can also write their own programs for programming data flash and calibration, as calibration routines are embedded in bq20zXX firmware which makes it easy (for details, see SLUA380 for the bq20z80 or SLUA379 for the bq20z70/z90).

The data-flash image should not be confused with the GG file – the later does not contain multichemistry support data and should not be used in this step. Programming the GG file using EV Software also is much slower than programming the data-flash image using the bqTester method.

If the data-flash image writing is not used, and chemistry is not the default, then chemistry-specific firmware *.senc file should be written prior to writing the GG file. See details on multichemistry support in the application report SLUA372.

Step 2: Calibration

Perform calibration at the board level before cells are connected. Current flowing through cells can disturb voltage calibration.

The firmware contains calibration routines, which makes this process easy to set up. The test software places the device in calibration mode and sends the true measured values to the device. The procedure is described in detail in SLUA380 for the bq20z80 or SLUA379 for the bq20z70/z90. TI provides bqTester and bqMTester software to automate this procedure (see previous section).

It is important that the voltage is measured with a 1-mV accuracy and that true measured voltage value is sent in a calibration command. Note that the voltage accuracy requirement is higher than in previous devices

Previously used voltage sources can still be used as long as the voltage is measured regularly with a 1-mV accurate voltmeter and the measured value is entered into the calibration program (for example, daily but actual interval depends on observed voltage drift). Only the voltage stability of the source is important, whereas actual voltage value is unimportant as long as it is accurately measured. An example of a voltage and current source that can be used is the calibration board for bqMTester that can be purchased from TI.

The current gain calibration is less critical. It affects only absolute values of gas-gauging (FCC, RemCap) but does not affect relative values (RSOC, Remaining Run Time).

All calibrations take place at the same time, so adding/excluding some calibration does not affect calibration time.

Step 3: Write Pack-Specific Information

Some examples of pack-specific information are Manufacturing Date, Serial Number, Lot Code, etc.

Writing pack-specific information is accomplished using data-flash access commands as described in detail in SLUA380 for the bq20z80 or SLUA379 for bq20z70/z90.

The bqMTester and bqTester programs write all the foregoing pack-specific information. Free source code can be obtained from TI on request, and more pack-specific data-flash constants can be added to it.

Step 4: Perform Any Needed Testing Such as Data-Flash Check, Electrical Integrity Tests, etc.

Any test that is performed on other bq20xx family devices can also be performed in this step. There is nothing bq20zXX specific.

Possible tests include:

1. Registers check
2. Data-flash check
3. Electrical checks (turning FETs ON and OFF)
4. Safety check

If turning the FETs ON is needed for some checks, it can be accomplished by using the SMB word write command 46. Word 0006 turns on charge and discharge FETs.

It is not recommended to send the 0021 (IT enable) command to turn ON the FETs at this point of production flow, because it also starts many gas-gauging functions that can read wrong values if cells are not attached. Functions activated include:

- Life Time Data
- Resistance values update
- Qmax values update

Step 5: Attach Cells

The recommended order of cells attachment is Ground (1N), 1P, 2P, 3P, 4P.

It is recommended that Ground be connected before other cell connections.

After the 1P–4P connection is made, if ground is again disconnected, the voltage measurement digital filter is distorted and wrong voltage readings are reported until the filter settles (up to 5 minutes).

To avoid the possibility of such distortion in case of operator error, a Reset command (0041) can be sent after cells are connected.

The reset (step 6) can be excluded, if after cell connections a handling step that exceeds 5 minutes exists, or if connection of ground first can be guaranteed.

Reset (Optional)

The purpose of this step is to eliminate possible voltage distortion due to a wrong order of cell connections. This step is optional and can be removed if at least one of the following conditions applies:

- After cell connections, a handling step that exceeds 5 min exists.
- Connection of ground (1N) first can be guaranteed.
- Discharge test in optional step 9 does not exceed 500 seconds (or step 9 is absent), and therefore no resistance is updated prior to shipment.

Step 7: Wait 5 Minutes (Optional)

Immediately after cell connection, the digital filter needs maximally 5-minutes of settling time to achieve highest voltage measurement accuracy.

If this step is not done (or not provided by handling time until IT is enabled), the first OCV reading after IT enable has a somewhat lower accuracy. The next reading takes place after 35 minutes and high accuracy is recovered. However, if a discharge activity longer than 500 seconds occurs before that time, the resistance update will be less accurate.

This step can be avoided if one of the following conditions apply:

- After cell connections, a handling step that exceeds 5 minutes exists.
- Discharge test in optional step 9 does not exceed 500 seconds (or step 9 is absent), and therefore no resistance is updated prior to shipment.

Step 8: IT Enable (Command 0021)

The Impedance Track algorithm (IT) is enabled by sending manufacturer access command 0021. This causes the setting of QEN bit in Operation Status. The following processes also are activated:

- Life Time Data update
- Resistance values update
- Qmax values update

The VOK bit in Operation Status also is set if present voltage is in the range of qualified voltages for Qmax update. It is unnecessary that VOK gets set, unless implementing Qmax update during production.

After sending IT enable command, Life Time Data update starts. It is not recommended to do any safety-related tests applying harsh conditions after IT is enabled.

Charge/Discharge for Testing Purposes or to Customer Requested Level (optional)

This step is optional and is not required for the device. Some manufacturers perform this step for their own purposes such as quality control or to bring device to required state of charge.

If this step follows the *IT enable* step, having passed less than 35 minutes and discharge continues for more than 500 seconds, a minimum 5-minute wait is recommended between cell connections and IT enable (step 8).

Step 10: Seal

It is recommended that the user change the default unseal codes in the data flash, so that the seal command prevents unauthorized access (including TI) to data flash and ROM.

Changing the default unseal codes is accomplished in the golden pack by using SMB commands 0x60 and 0x61 prior to creating the data-flash image. Changed values are contained in the data-flash image and copied to all packs in production during step 1.

Note that command 0x60 (like all block read/write commands) has the high byte of each word first. For example, if you want to write codes 0xFDMA 0xMKLR, the block needs to be written as MA FD LR MKX.

Test successful unsealing and accessing ROM during the characterization step before making a data-flash image for production.

22.3 Possible Alternative Production Order

Some manufacturers perform additional tests that require an alternative order that includes charge/discharge testing prior to enabling IT. In this case, production duration is longer. Such changes are possible as long as the principles outlined in the recommended procedure are followed. One example is given in Figure 2.

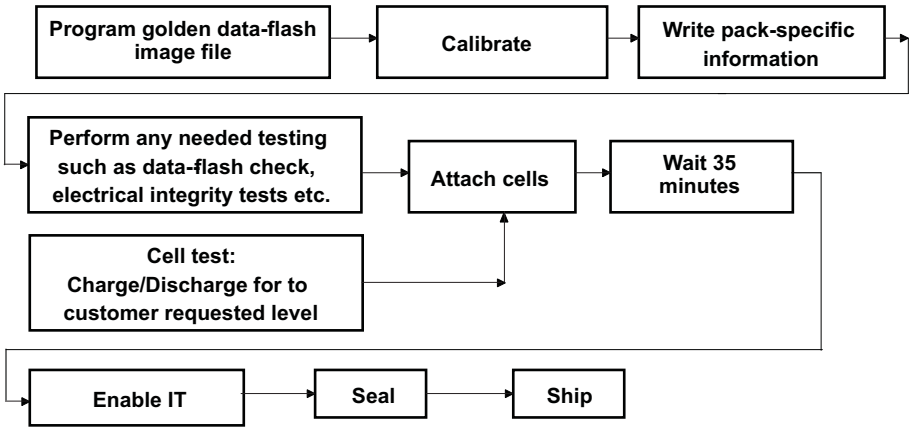


Figure 2. Additional Manufacturers' Charge/Discharge Testing

In this case, the manufacturer undertakes charge/discharge testing at the cell level prior to connecting cells to the PCB. This is acceptable as long as a 35-minute or longer wait period is provided between the charge/discharge and enabling the IT by command 0021.

Chapter 23

Data Flash Programming and Calibrating the bq20z70 and bq20z90 Family of Gas Gauges

Doug Williams *Battery Management*

ABSTRACT

This application report presents a strategy for high-speed, economical calibration and data flash programming of the bq20z70/bq20z90 advanced gas gauge chipset family. VB6 code examples are provided, along with step-by-step instructions for preparing a golden battery pack.

23.1 Introduction

The bq20z70/bq20z90 family of advanced gas gauges is built with new technology and a new architecture for both data flash access and calibration. With this new architecture, unit production cost and capital equipment investment can be minimized, as there is no longer a need to perform a learning cycle on each pack. A single “golden pack” can become the source of data for all other packs. A method is shown to quickly read and write the golden image. Also, the calibration method is quick and simple because most of the calibration routines are built into the firmware of the target device.

The methods in this document are presented as VB6 (Visual Basic 6) functions. These functions were copied directly from working code. In order to read from and write to the data flash, they use five types of SMBus read and write functions. These can be duplicated in any software environment that has SMBus communication capabilities. As used herein, each Read/Write function is designed for communication with a gas gauge, so the device address (0x16) is omitted for clarity.

1. WriteSMBusInteger() has two arguments – the SMBus command and a signed integer. Internally, this function separates the integer into two bytes for transmission by the SMBus write-word protocol.
2. WriteSMBusByteArray() has three arguments – the SMBus command, the array of bytes and an integer specifying the length of the byte array. Internally, this function separates the byte array into separate bytes for transmission by the SMBus write-block protocol.
3. WriteSMBusCommand() has only one argument – the SMBus command.
4. ReadSMBusUnsignedInteger has two arguments – the SMBus command and the returned integer.
5. ReadSMBusByteArray() has three arguments – the SMBus command, the returned array of bytes, and the returned length of the byte array. It is internally implemented with the SMBus read-block protocol.

Also used in these functions is a simple delay routine called DoDelay. VB6 code for this procedure is provided at the end of the document.

Error handling is not implemented in this sample code, because requirements are unique and varied. Also, constants are hard-coded into the functions to improve clarity rather than documenting them in code elsewhere as would normally be good coding practice.

A good strategy for production is a seven-step process flow:

1. Write the data flash image to each device. This image was read from a *golden* pack.
2. Calibrate the device.
3. Update any individual flash locations, such as serial number, lot code, and date.
4. Perform any desired protection tests.
5. Connect the cells.
6. Initiate the Impedance Track™ algorithm
7. Seal the pack.

In this document, the first three steps are examined in detail.

23.2 Preparing the Golden Pack

Impedance Track™ technology allows the bq20z70/bq20z90 gas gauge to automatically acquire and maintain parameters for battery modeling needed for continuous accuracy, regardless of battery model or manufacturer. The ICs are shipped preprogrammed with default values for these parameters. In the course of daily use (charge, discharge, unused), the algorithm collects new parameters. Parameter acquisition is complete after one full discharge cycle and subsequent relaxation takes place.

The default parameters that are used for fuel gauging prior to discharge activity are less accurate than

parameters acquired during such activity. Therefore, the error of the gas gauge is more than the 1% that is achieved after parameter acquisition. It is desirable to have optimal accuracy in the battery packs coming from the production line even before any discharge activity occurs. This can be accomplished by performing a discharge cycle on one battery pack (let it acquire optimized parameters), save its data flash in a file, and then program the golden data into all battery packs coming from the production line.

Creating Pre-Learned Defaults

1. Assemble a battery pack with the bq20z80 solution, which includes setting basic flash constants for a given pack configuration, calibrating the pack, connecting *System Present* to ground, and enabling IT. This is described in detail in the application report *Pack Assembly and the bq20z80* (SLUA335), which also applies to the bq20z70 and the bq20z90.
2. In particular, it is important to set parameters specific to the number of serial cells used. This is described in application report *bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity* (SLVA208),which also applies to the bq20z70 and the bq20z90 .
3. To achieve maximum accuracy of first cycle parameter acquisition, set an initial guess for Qmax Cell 0, Qmax Cell 1, Qmax Cell 2, Qmax Cell 3 and Qmax Pack. These values are in mAh as specified in the battery manufacturer data sheet. For example, if single-cell data-sheet capacity is 2400 mAh and 3 parallel cells are used, set each value to 2400 × 3 = 7200 mAh.
4. Charge the pack to full.
5. Let it relax for 2 hours.
6. Discharge the pack to the minimum system-acceptable voltage (should be the same as DF.Gas Gauging.IT Cfg.Term Voltage) at the typical application rate. The exact rate is not critical.
7. Let it relax for 5 hours.
8. Repeat steps 4 through 7 to achieve maximum impedance table accuracy. Verify that DF.Gas Gauging.State.Update Status reads 06. If not, repeat the cycle. Its normal value should be 06.
9. Use the EVSW to export the .gg File. Open the .gg file with Notepad to change DF.Gas Gauging.State.UpdateStatus to 02. Change DF.SBS Configuration.Data.Cycle Count to 0.
10. Reprogram the pack with a fresh .senc to clear all hidden constants.
11. Use the EVSW to import the modified .gg file as saved in step 9. Write All.
12. Send reset command (0x0041).

The *golden pack* is now ready to have its data flash read into a binary file as described in the function listed in Section 3.

23.3 Reading and Saving the Data Flash Image From the Golden Pack

Note that this step only needs to be done once for a given project.

```
Function SaveDataFlashImageToFile(sFileName As String) As Long

    Dim iNumberOfRows As Integer
    Dim lError As Long
    Dim yRowData(32) As Byte
    Dim yDataFlashImage(&H700) As Byte
    Dim iRow As Integer
    Dim iIndex As Integer
    Dim iLen As Integer
    Dim iFileNumber As Integer

    '// FOR CLARITY, WITHOUT USING CONSTANTS
    '// 0x700 is the data flash size.
        0x700 \ 32 = 56 rows
    iNumberOfRows = &H700 \ 32

    '// PUT DEVICE INTO ROM MODE
    lError = WriteSMBusInteger(&H0, &HF00)
    DoDelay 0.01

    '// READ THE DATA FLASH, ROW BY ROW
    For iRow = 0 To iNumberOfRows - 1

        '// Set the address for the row. &H9 (0x09) is the ROM mode command.
        '// 0x200 is the row number where data flash starts.
        '// Multiplication by 32 gives us the actual physical address where each row starts
```

```
            lError = WriteSMBusInteger(&H9, (&H200 + iRow) * 32)

            '// Read the row. &HC (0x0c) is the ROM mode command.
            lError = ReadSMBusByteArray(&HC, yRowData, iLen)

            '//Copy this row into its place in a big byte array
            For iIndex = 0 To 32 - 1
                yDataFlashImage((iRow * 32) + iIndex) = yRowData(iIndex)
            Next iIndex

        Next iRow

        '// WRITE DATA FLASH IMAGE TO FILE
        iFileNumber = FreeFile
        Open sFileName For Binary Access Write As #iFileNumber
        Put #iFileNumber, , yDataFlashImage
        Close #iFileNumber

        '// EXECUTE GAS GAUGE PROGRAM
        lError = WriteSMBusCommand(&H8)

    End Function
```

23.4 Writing the Data Flash Image to Each Target Device

The following method is fast. It only takes about 2 seconds to write the entire data flash in this manner.

CAUTION
If power is interrupted during this process, the device may become unusable.

```
Function WriteDataFlashImageFromFile(sFileName As String) As Long
    Dim lError As Long
    Dim iFileNumber As Integer
    Dim iNumberOfRows As Integer
    Dim iRow As Integer
    Dim iIndex As Integer
    Dim yRowData(32) As Byte
    Dim yDataFlashImage(&H700) As Byte
    '// READ THE FLASH IMAGE FROM THE FILE INTO A GLOBAL BYTE ARRAY
    iFileNumber = FreeFile
    Open sFileName For Binary Access Read As #iFileNumber
    Get #iFileNumber, , yDataFlashImage
    Close #iFileNumber
    '// FOR CLARITY, WITHOUT USING CONSTANTS
    iNumberOfRows = &H6C0 \ 32  '54 Rows
    '// PUT DEVICE INTO ROM MODE
    lError = WriteSMBusInteger(&H0, &HF00)
    DoDelay 0.01
    '// ERASE DATA FLASH, ROWS ARE ERASED IN PAIRS
    For iRow = 0 To iNumberOfRows - 1 Step 2
        lError = WriteSMBusInteger(&H11, iRow)
        DoDelay 0.04
    Next iRow
    '// WRITE EACH ROW
    For iRow = 0 To iNumberOfRows - 1
        '// Set the row to program into the first element of the 33 byte array
        yRowData(0) = iRow
        '// Copy data from the full array to the row array
        For iIndex = 0 To 31
            yRowData(iIndex + 1) = yDataFlashImage((iRow * 32) = iIndex)
        Next iIndex
        '// Write the row. Length is 33 because first byte is row number
        1Error = WriteSMBusByteArray(&H10, yRowData, 32 + 1)
        DoDelay 0.02
    Next iRow
    '// EXECUTE GAS GAUGE PROGRAM
    lError = WriteSMBusCommand(&H8)
End Function
```

23.5 Calibration

Devices in the bq20z70/bq20z90 family of advanced gas gauges are quick and easy to calibrate. It only takes about 5 seconds to accurately calibrate current offset, voltage, temperature, and board offset. With the Impedance Track™ devices, most calibration routines have been incorporated into firmware algorithms, which can be initiated with SMBus commands. The hardware for calibration is also simple. One current source, one voltage source, and one temperature sensor are all that is required. The accuracy of the sources is not important, only their stability. However, accurately calibrated reference measurement equipment should be used for determining the actual arguments to the function. For periodic voltage measurement, a DVM with better than 1-mV accuracy is required.

The elapsed time for calibration can be changed by modifying values in the data flash, but this is not recommended. Use the default values for the times in DF.Calibration.Config

In the CalibrateAll( ) function, command 0x51 is used to setup a current offset, voltage, current , and temperature calibration of the device.. Pack voltage calibration is generally not performed because its accuracy is not required for standard applications. In this case, Pack Voltage refers to a separate measurement of the voltage at the pack terminal and is unrelated to the SBS.Voltage( ) measurement.

The definition of the bits in command 0x51 are:

Bit 0	**Coulomb Counter Offset**	**Bit 8**	**Pack Gain**
Bit 1	**Reserved**	**Bit 9**	**Pack Voltage**
Bit 2	**ADC Offset**	**Bit 10**	**AFE Error**
Bit 3	**Temperature, Internal**	**Bit 11**	**Reserved**
Bit 4	**Temperature, External 1**	**Bit 12**	**Reserved**
Bit 5	**Temperature, External 2**	**Bit 13**	**Reserved**
Bit 6	**Current**	**Bit 14**	**Run ADC Task Continuously**
Bit 7	**Voltage**	**Bit 15**	**Run CC Task Continuously**

Bits 14 and 15 should always be set. These cause the Coulomb Counter and ADC tasks to run continuously, just as they do in normal operation. This has been found to increase the accuracy of the calibration.

After command 0x51 is issued, the calibration sequence is started in the firmware of the gas gauge. The calibrations are run in sequence starting from the least significant bit. Then, command 0x52 is used to poll these bits, which change from high to low as the tasks are completed. However, bits 14 and 15 do not change; hence, the masking of them in the polling loop.

It can be seen from this code that a simple modification to command 0x51 would allow it to work as a single function calibration. For example, to only calibrate voltage, only bit 7 could be set.

```
Function CalibrateAll(iVoltage As Integer, iCurrent As Integer, iTemperature As Integer, iCells
As Integer) As Long

'// iVoltage is in millivolts
'// iCurrent is in milliamps (normally negative, such as -2000)
'// iTemperature is in Kelvin/10 units, so the argument is: 10 * (Celsius + 273.15)

    Dim lError As Long
    Dim bDoingCal As Boolean
    Dim iValue As Long

    '// GO TO CALIB MODE
    IError = WriteSMBusInteger(&H0, &H40)

    '// WRITE THE NUMBER OF CELLS
    IError = WriteSMBusInteger(&H63, iCells)

    '// WRITE THE ACTUAL VOLTAGE, CURRENT & TEMPERATURE
    IError = WriteSMBusInteger(&H60, iCurrent)
    IError = WriteSMBusInteger(&H61, iVoltage)
    IError = WriteSMBusInteger(&H62, iTemperature)

    '// START CALIBRATION
    '// Useful cal lo byte  &HD5 - External temperature sensor 1
    '//                     &HF5 - External temperature sensor 1 and 2
    '//                     &HCD - Internal temperature sensor
    IError = WriteSMBusInteger(&H51, &HC0D5)

    '// POLL CALIBRATION STATUS - WAIT FOR LOWER 14 BITS TO ALL CLEAR
    bDoingCal = True
    While bDoingCal
        IError = ReadSMBusUnsignedInteger(&H52, IValue)
        bDoingCal = IValue And &H3FFF
        DoDelay 0.2 '// check every 200 millisecond
```

```
    Wend

    '// TRANSFER RESULTS TO DATAFLASH
    IError = WriteSMBusCommand(&H72)
    DoDelay 0.1 '// Insure write process is finished

    '// EXIT CALIB MODE
    IError = WriteSMBusCommand(&H73)

    End Function
```

Because of the simplified single ground system in the bq20z70/bq20z90 family, each unit should be calibrated for board offset. Use the following function in normal mode to calibrate the board offset. During this procedure, the device under test must be powered from the cells only and no external load or charge current may be applied. Note that the function requires the sense resistor value in milliohms as an argument.

```
Function CalibrateBoardOffset(fSenseMilliohms As Single) As Long
'// Device under test must be powered from the Cell side, which
'// allows the device current to flow through the sense resistor.
'// Insure no other current is flowing through the sense resistor.

   Dim 1Error As Long
   Dim lValue As Long
   Dim i As Integer
   Dim iExternalOffset As Integer
   Dim iInternalOffset As Integer
   Dim iBoardOffset As Long
   Dim yData(32) As Byte
   Dim iLen As Integer

   '// READ EXTERNAL OFFSET CURRENT
   1Error = WriteSMBusInteger(&H40, &H8042) '//Set address of coulomb counter
   DoDelay 0.2 '// Extra settling time to clear the decimation filter

   For i = 1 To 4
      DoDelay 0.3 '// take 4 samples at 300 ms intervals
      1Error = ReadSMBusUnsignedInteger(&H42, 1Value) '// Peek Coulomb Counter
      iExternalOffset = iExternalOffset + 1Value
   Next i

   '// READ INTERNAL OFFSET CURRENT
   1Error = WriteSMBusInteger(&H40, &H8040) '//Set address of coulomb counter config register
   1Error = WriteSMBusInteger(&H41, &H43) '//Change configuration to internal mode
   1Error = WriteSMBusInteger(&H40, &H8042) '//Set address of Coulomb Counter
   DoDelay 0.2 '// Extra settling time to clear the decimation filter

   For i = 1 To 4
       DoDelay 0.3
       1Error = ReadSMBusUnsignedInteger(&H42, IValue) '// Read Coulomb Count
       iInternalOffset = iInternalOffset + 1Value
   Nexti

   1Error = WriteSMBusInteger(&H40, &H8040) '//Set address of coulomb counter config register

   1Error = WriteSMBusInteger(&41, &H2) '//Return configuration to external mode

   '// CALCULATE BOARD OFFSET

   iBoardOffset = Int(16 * (iExernalOffset - iInternalOffset) + (3745 * fSenseMilliohms/1000))

   If iBoardOffset < 0 Then iBoardOffset = 65536 + iBoardOffset '// fix negative case

   '// WRITE BOARD OFFSET TO DATA FLASH. FROM DATA MANUAL, SUBCLASS=104, OFSET=16
   1Error = WriteSMBusInteger(&H77, 104) '//Set subclass to 104
   1Error = ReadSMBusByteArray(&H78, yData(), iLen) '// Read the page

   yData(16) = (iBoardOffset And &HFF00) \ 256 '// Modify MS byte
   yData(17) = iBoardOffset And &HFF '// Modify LS byte

   1Error = WriteSMBusByteArray(&H78, yData(), iLen) '//Write page back to flash
   DoDelay 0.1 '// Insure flash write is finished

End Function
```

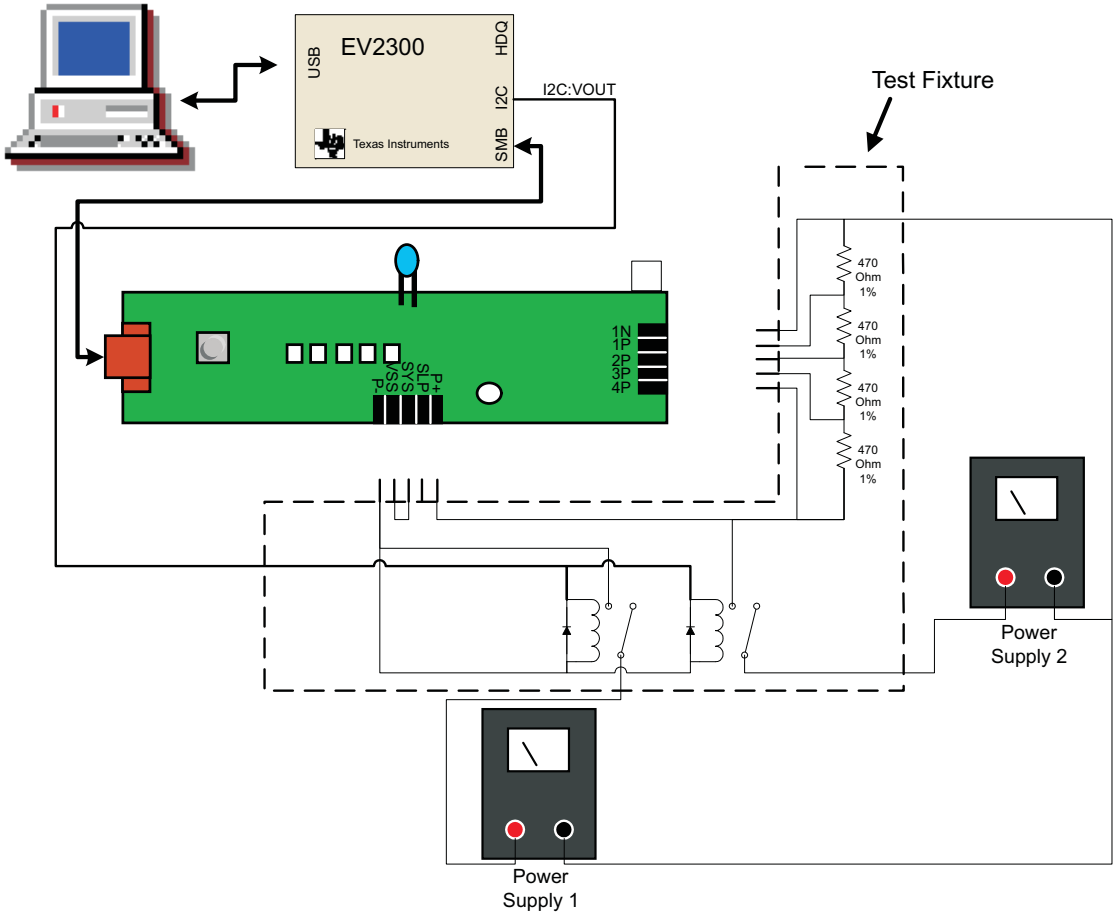
23.6 Writing Pack-Specific Data Flash Locations

The third step is to fine tune the data flash a little for each pack, to give it a unique identity. In the following example, the pack Serial Number is written using subclass and offset information found in the gas gauge product data sheet. Modifications to single data flash locations normally require a block read of the 32-byte data flash page, then updating the desired element of the block, and writing it back to the device. This procedure is documented in the product data sheet.

```
Function WritePackSerialNumber(iSerialNumber As Integer) As Long

    Dim lError As Long
    Dim yData(32) As Byte
    Dim iLen As Integer

    '// SET THE SUBCLASS TO 48 (FOUND IN PRODUCT DATASHEET)
    lError = WriteSMBusInteger(&H77, 48)

    '// READ THE PAGE
    lError = ReadSMBusByteArray(&H78, yData(), iLen)

    '// REPLACE THE TWO BYTES AT OFFSET 12 (FOUND IN DATASHEET) WITH NEW S/N
    yData(12) = (iSerialNumber And &HFF00) \ 256 '// modify MS byte
    yData(13) = iSerialNumber And &HFF '// modify LS byte

    '// WRITE THE PAGE BACK TO FLASH
    lError = WriteSMBusByteArray(&H78, yData(), iLen)

    '// FLASH WRITES ARE SLOW
    DoDelay 0.1

End Function

Sub DoDelay(fWaitTime As Single)

    Dim vTime As Variant

    vTime = Timer
    While Timer < (vTime + fWaitTime)

        '// fix midnight problem
        If Timer < vTime Then Exit Sub

        '// Yield to various Windows events while the delay is in progress
        DoEvents

    Wend

End Sub
```

Using bqTester Single Site Software

- **FEATURES**
  - Programs and calibrates smart battery modules based on the bq20zxx
  - Calibrates coulomb counter offset, voltage, temperature, and current
  - Programs
    - Serial number
    - Date
    - Pack Lot Number
  - Test software is Windows™ 2000 and Windows™ XP compatible.
  - Data-logging feature preserves calibration records.



bqTester single site software from Texas Instruments (TI) is designed to calibrate and program electronic smart battery modules based on the bq20z70, bq20z80, bq20z90, and future advanced battery gas gauges. The bqTester works with the TI EV2300 USB-based PC interface board for battery fuel gauge evaluation. The bqTester is open-source software and can be modified to suit the user's requirements.

24.1 Minimum System Requirements

- Computer: PC or compatible
- Operating system: Windows™ 2000, or Windows™ XP. Operation with Windows™ 98SE may be possible but is untested and unsupported.
- Minimum video resolution is 640x480; recommended: 800x600 or above
- 1 available USB port
- 1 EV2300 USB-based PC interface board for battery fuel gauge evaluation from Texas Instruments
- 5-MB available hard drive space
- Visual Basic version 6.0 with Service Pack 5 is required if user wishes to alter program operation.

24.2 Software Installation

The **TI bq SingleStationTester Software.exe** executable file installs all required software, drivers, and DLL files for proper software operation. To install the software:

- **Do not** connect any EV2300s to the PC before installing the software. If any are connected, disconnect them now.
- It is recommended to check for software in the *bqTester Tool Folder* on the www.ti.com Web site. The Tool Folder is located at: http://focus.ti.com/docs/toolsw/folders/print/bqtester.html
- If installing software downloaded from the above Web site, then unzip the downloaded file into a temporary directory and go to **Start, Run**, and type: **C:\Yourdirectory\TI bqSingleStationTester Software.exe** and click **OK** (replace *C:\Yourdirectory* with the location where the file was unzipped).
- . The welcome screen shown in Figure 1 is displayed.

Figure 1. Welcome Screen

After a few seconds, the Single Site Setup Wizard will appear as shown in Figure 2.

Figure 2. Single Site Setup Wizard

Click *Next* to continue installing the Single Site software. The License Agreement box appears. After carefully reading the License Agreement, click *I Agree* to continue installation. Note: clicking *cancel* aborts the installation. After *I Agree* has been clicked, the Choose Components box appears as shown in Figure 3.

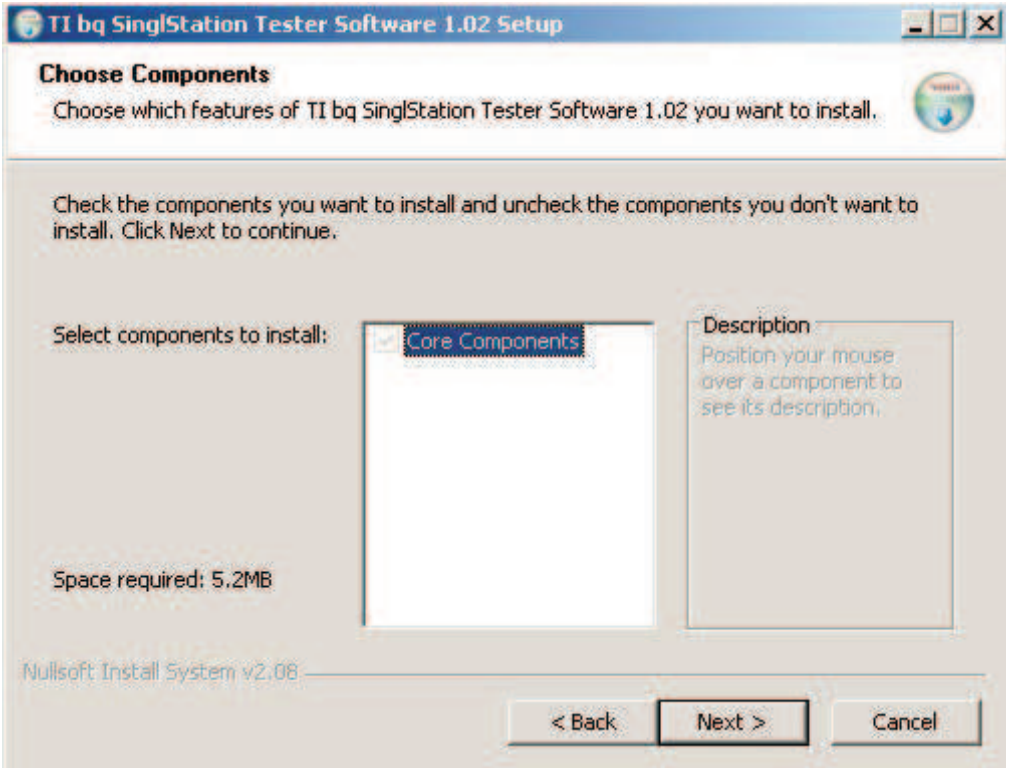


Figure 3. Choose Components Box

Notice that *Core Components*= is selected and grayed out. No other selections can be made. Click *Next* to proceed. The *Choose Start Menu Folder* box appears as shown in Figure 4.

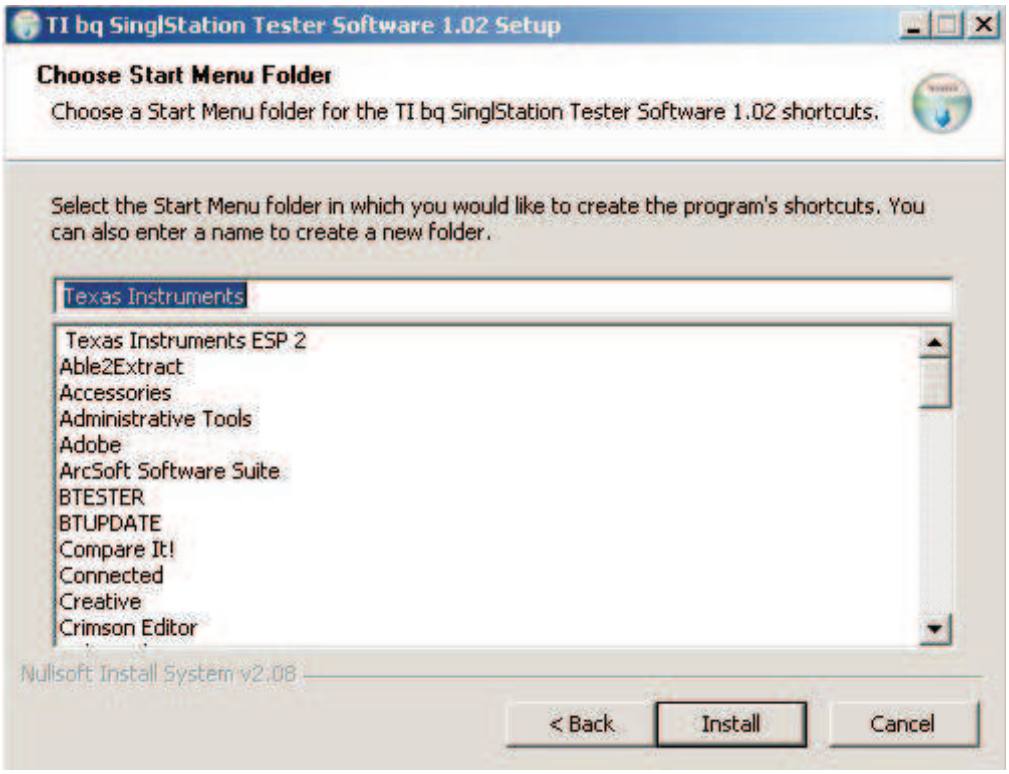


Figure 4. Choose Start Menu Folder Box

Choose the Start Menu folder where you want the program's shortcuts to be created. The default is Texas Instruments. After choosing the installation folder, click *Install*. A box is displayed showing the files being installed, followed by the Completing Setup Wizard as shown in Figure 5.

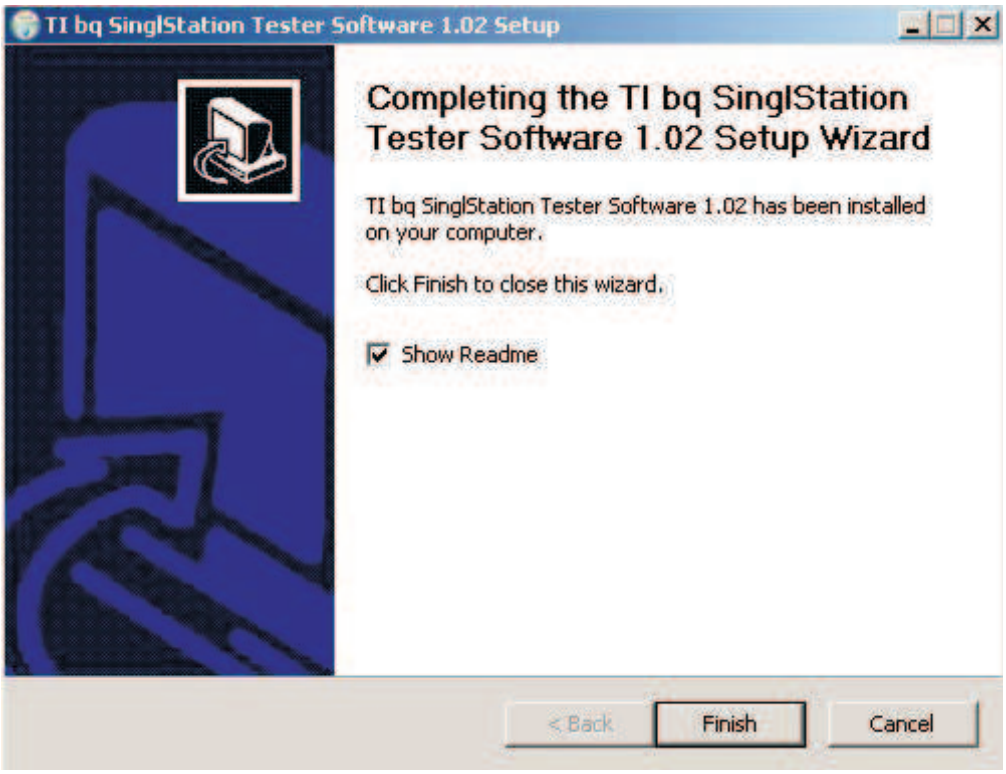


Figure 5. Completing Setup Wizard Box

Click *Finish* to complete installation. Be sure to check the *Show Readme* box if additional information is desired

EV2300 Driver to USB Port Association

Two drivers are associated with the EV2300. An instance of the two drivers must be associated with the EV2300 connected to the bqTester PC through any USB port. If an EV2300 is connected to the bqTester PC and the PC detects that it has not had an EV2300 connected to that particular USB port before, then the computer requires the following procedure to associate a copy of the drivers for that USB port. To associate an instance of the EV2300 drivers to any given USB port, connect an EV2300 to the bqTester PC. After a few seconds the Found New Hardware screen appears as seen in Figure 6. Note: if an EV2300 has been installed on the PC previously, the Found New Hardware screen does not appear and installation is complete.

Figure 6. Found New Hardware Wizard

Select *No, not at this time* and click *Next*. If the first screen that appears does not look like this screen, then it looks like the one shown in Figure 7.

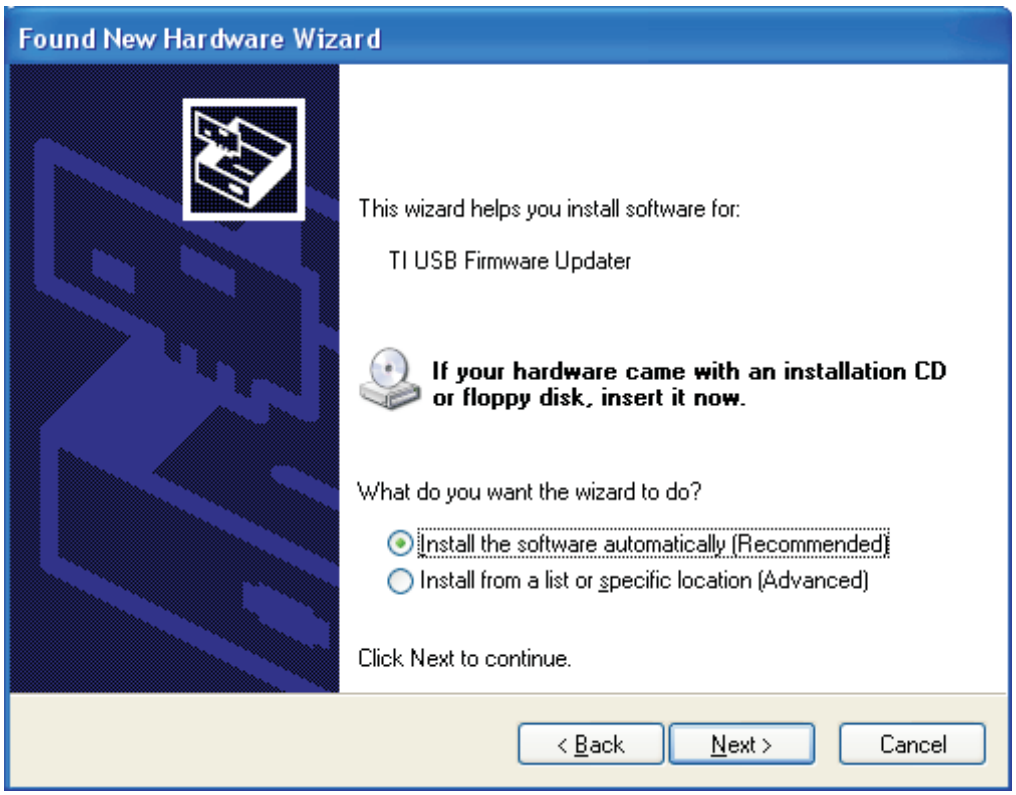


Figure 7. Alternate Found New Hardware Screen

Select *Install the software automatically (Recommended)* and click *Next*. This wizard is for the first of the two drivers (TI USB Firmware Updater) required for the EV2300. The Windows Logo Testing screen appears as shown in Figure 8.

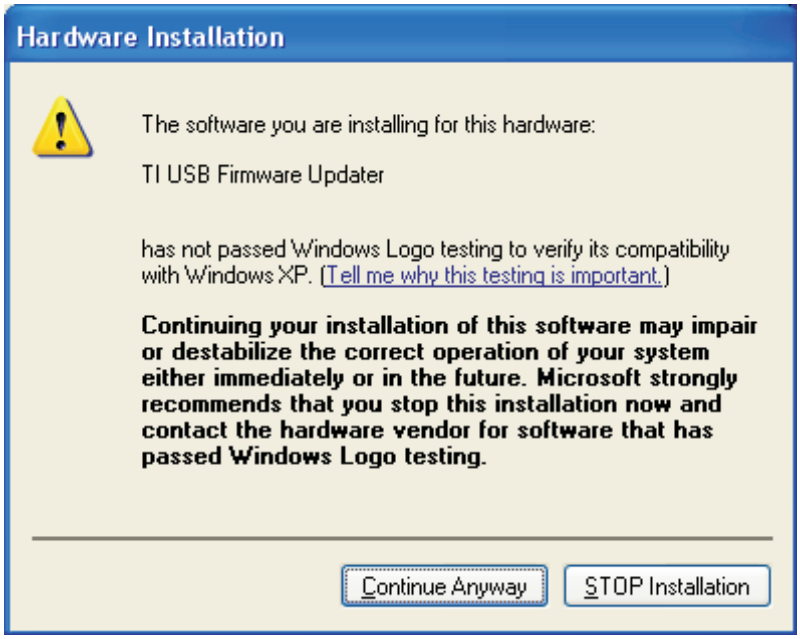


Figure 8. Windows Logo Testing Screen

Click *Continue Anyway* to proceed with the installation. It is common for the next screen to be the Confirm File Replace screen as shown in Figure 9.

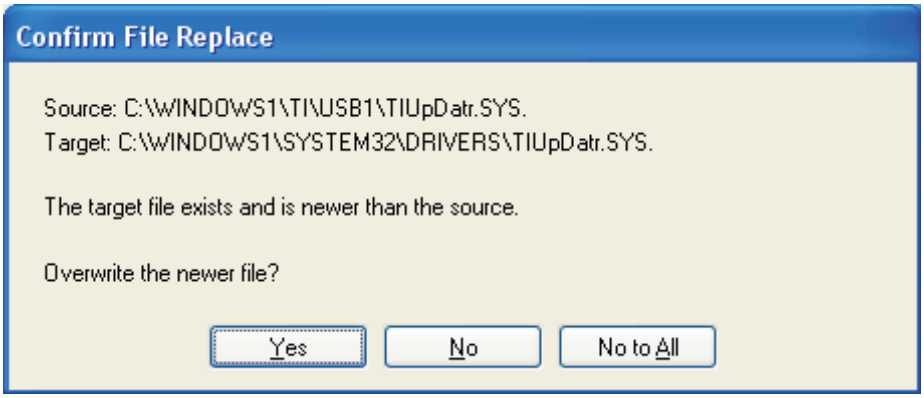


Figure 9. Confirm File Replace Screen

Click *No* to continue. If this screen does not appear, then the next screen is the *Completing the Found New Hardware Wizard* screen as seen in Figure 10.

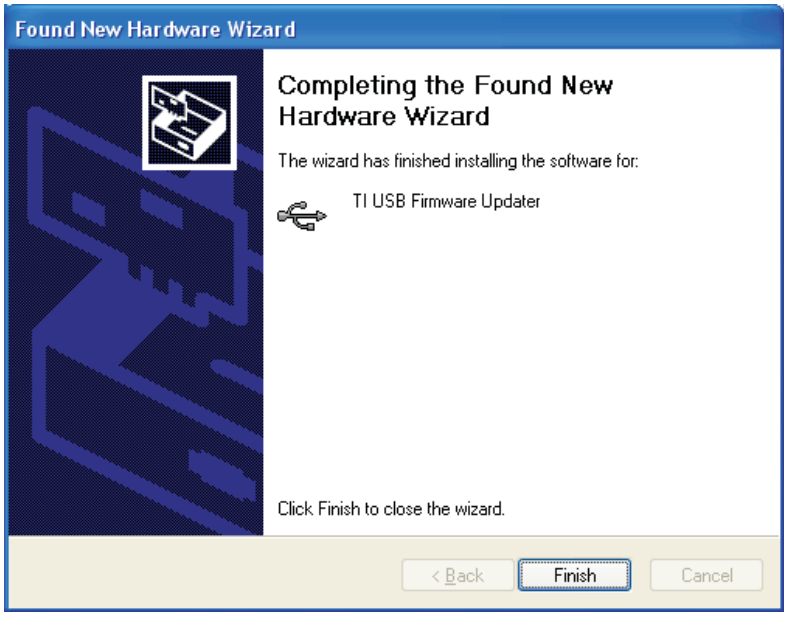


Figure 10. Completing the Found New Hardware Wizard Screen

The TI USB Firmware Update driver is now installed for the EV2300. Click *Finish* to exit the driver install wizard. After a few seconds, another Found New Hardware screen appears to start the installation of the final driver for the EV2300 as shown in Figure 11.

Figure 11. Found New Hardware Wizard

Select *No, not at this time* and click *Next*. If the screen that appears does not look like this, then it looks like the one shown in Figure 12.

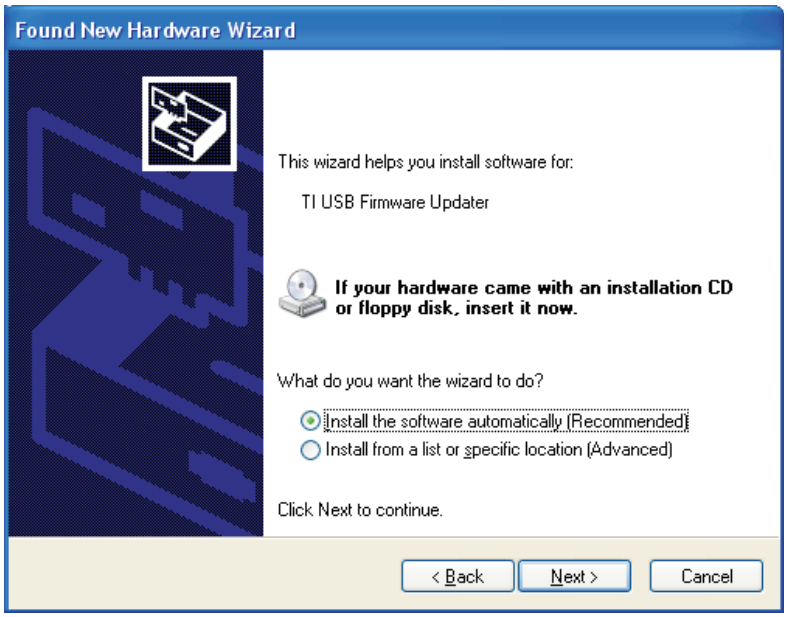


Figure 12. Alternate Found New Hardware Screen

Select *Install the software automatically (Recommended)* and click *Next*. This wizard is for the second of the two drivers (TI USB bq80XX Driver) required for the EV2300. The Windows Logo Testing screen appears as shown in Figure 13.

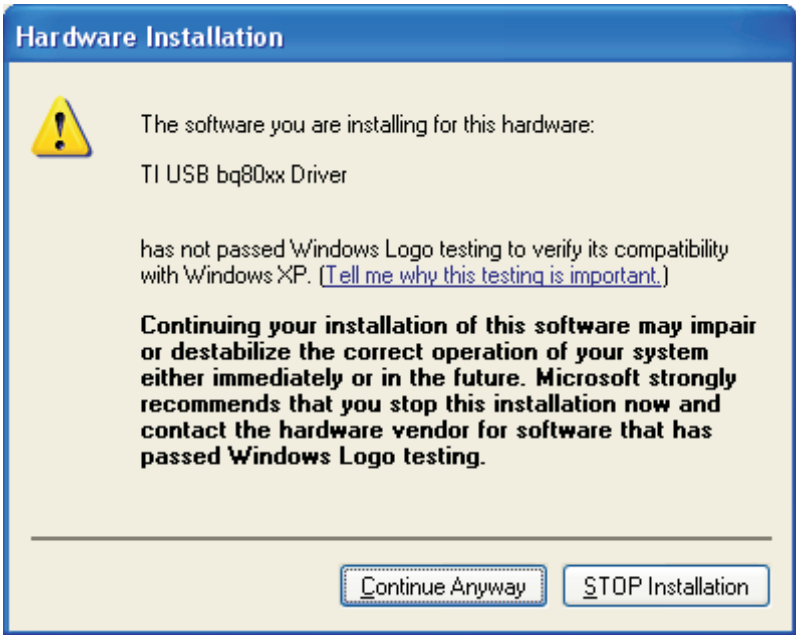


Figure 13. Windows Logo Testing Screen

Click *Continue Anyway* to proceed with installation. It is common for the next screen to be the *Confirm File Replace* screen as shown in Figure 14.

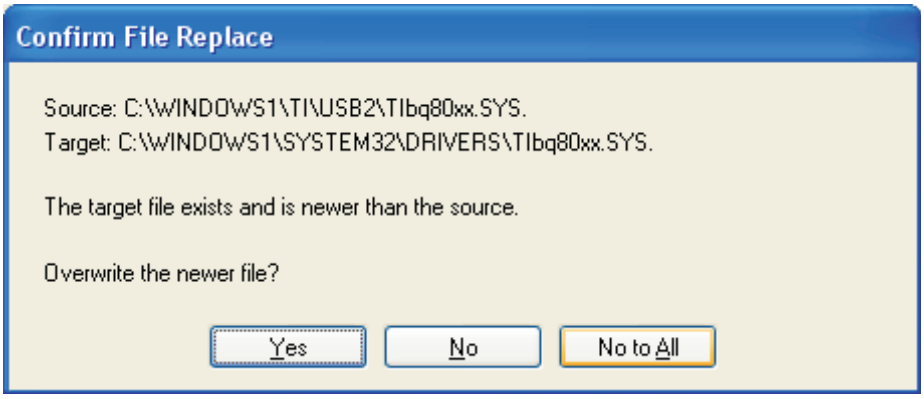


Figure 14. Confirm File Replace Screen

Click *No* to continue. If this screen does not appear, then the next screen is the *Completing the Found New Hardware Wizard* screen as seen in Figure 15.

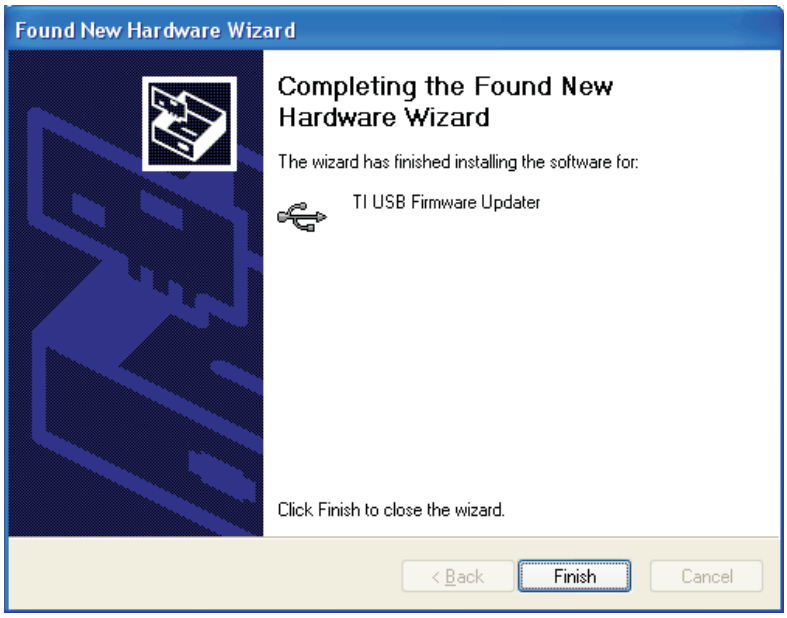


Figure 15. Completing the Found New Hardware Wizard Screen

The TI bq80xx Driver is now installed for the EV2300. Click *Finish* to exit the driver install wizard. At this point, the installation of the EV2300 is complete.

Source code in Visual Basic 6.0 format is available if the user wishes to modify the behavior of the bqTester. Contact TI for access to the source code.

24.3 Interface Connections

The bqTester software requires that the TI EV2300 USB-based PC interface board for battery fuel gauge evaluation interface be installed and running properly. The smart battery module should be connected to the EV2300 board and external power supplies as shown in Figure 16.

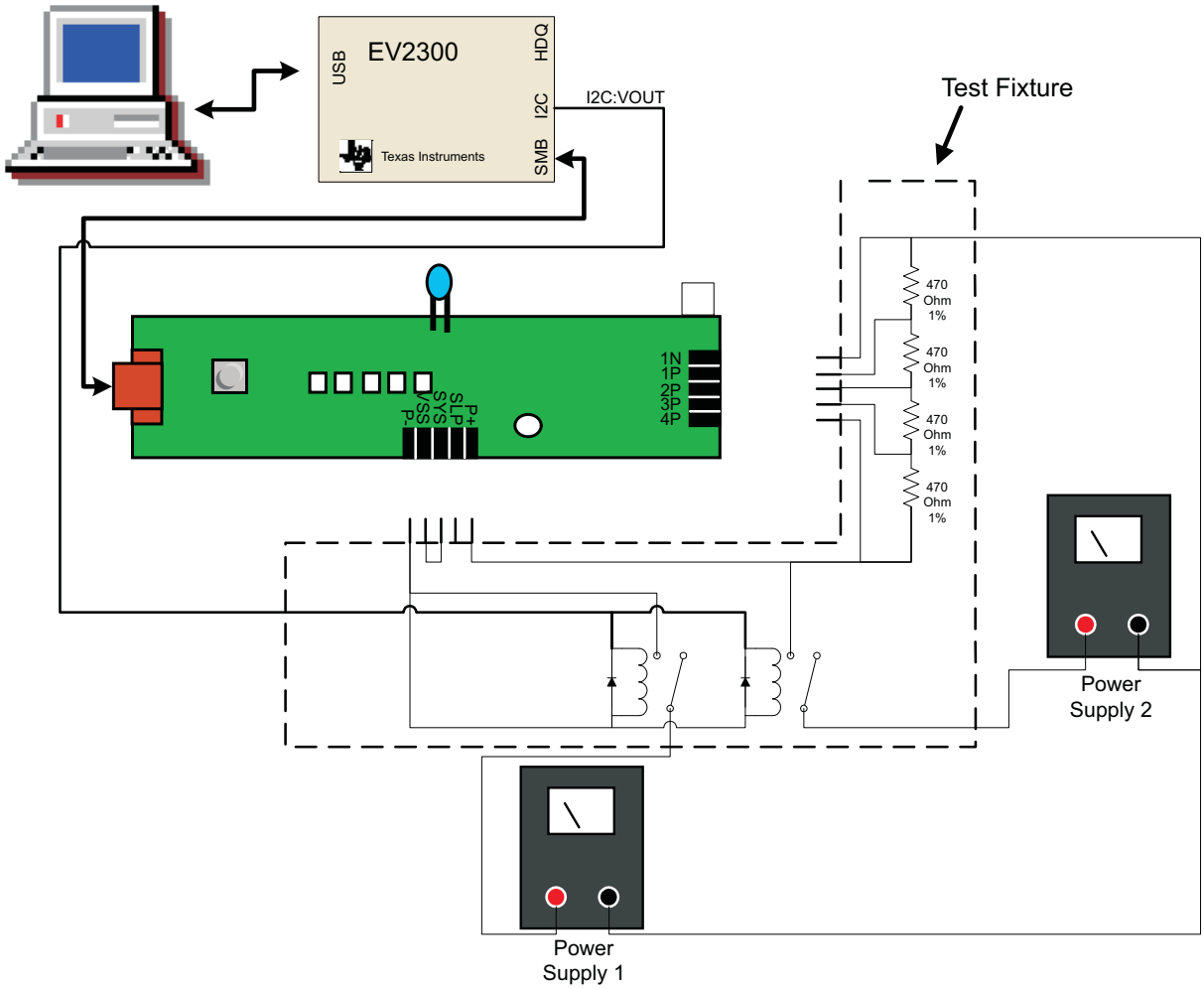


Figure 16. Single Site Tester Interface Connections

Do not use actual battery cells with this software. Cells should be simulated with resistors as shown in Figure 16.

The relays used to validate this procedure are 10-A, 250-Vac relays with a 5-Vdc coil. Any brand can be used but the ones used during this test were Omron model G6RN-1. The diodes used were 1N4148. Set the power supply 1 Vdc to 3 Vdc and limit current to 2 A dc. Set power supply 2 to the voltage corresponding to the number of cells being simulated (e.g., 10.8 Vdc for 3 cells or 14.4 Vdc for 4 cells). A calibrated temperature probe also is needed to measure the actual temperature.

24.4 Testing

Creating the Golden Image File (mandatory procedure)

After engineering development has been completed, a *golden* data flash image file must be made from an *Engineering Perfect* module. This *Golden* Image file is used as a default to program the Static Data Flash constants in all the bq20zxx-based smart battery modules using bqTester during production. It is important

that this process is completed. If it is not, then the Impedance Track™ algorithm may not function correctly. This section assumes the user's familiarity with Texas Instruments evaluation software for the bq20zxx modules because the user was most likely used it during the engineering development phase of this project. If unfamiliar with the software, then see the *bq20z80-001 EVM tool folder* that includes a user's guide for the EVM, application reports, and the latest EV software:

http://focus.ti.com/docs/toolsw/folders/print/bq20z80evm-001.html

24.4.147.6 Creating the "Engineering Perfect" Battery Pack It is assumed at this point that an engineering prototype battery pack is complete and that all static data flash constants have been reviewed and verified for a particular battery pack model. Static data flash is all data flash constants that are not battery pack specific.

Static Data examples: Static data examples are Charging Voltage, Impedance Track resistance tables, and QMAX settings. Examples of nonstatic data include serial number, date, and calibration. It is also assumed that this Engineering Perfect battery pack was created using the correct chemistry support SENC file. For more information on this, see the multichemistry support application report *Support of Multiple Li-Ion Chemistries With Impedance Track™ Gas Gauges* (SLUA372).

At this point, the Impedance Track data must be verified. This data must be updated and accurate so that all battery packs produced have accurate Impedance Track tables in data flash *right out of the box*. To ensure that the Impedance Track tables are optimized, complete the following steps:

1. Using an EV2300 and the EV software appropriate for the device being used in this application (e.g., bq20z70, bq20z80, or bq20z90), ensure that the data flash locations **Qmax Cell 0–Qmax Cell 3**, and **Qmax Pack** have good estimates in them for the battery pack capacity. This information can be derived from the battery cell manufacturer data sheet. Also note that if more than one cell is connected in parallel, then the capacity increments by one cell capacity for every cell in parallel. For example, if a single-cell data-sheet capacity is 2400 mAh, and three parallel cells are used, set each value to 2400 x 3 = 7200 mAh.
2. Charge the pack to full. If it does not charge then ensure that Impedance Track is enabled by sending data 0x0021 to SMBus command 0x00 (*Manufacturer Access*).
3. When the pack is full, remove the charger, and let the pack relax for 2 hours.
4. Discharge the pack to minimal device acceptable voltage (also set as *Term Voltage* flash constant), at a typical rate for the target application. The exact rate is not critical.
5. Let the pack relax for at least 5 hours.
6. Repeat steps 2 through 5 for maximum accuracy.
7. Connect the pack to the EV software, go to the data flash screen, and ensure that **Update Status** is 0x06.
8. The battery pack is now *Engineering Perfect*.

24.4.147.7 Creating Golden GG file from Engineering Perfect Battery Pack A GG file needs to be created with all the data from the *Engineering Perfect* battery pack that is used in creating the *Golden Image* File. The purpose of this GG file is to ensure that all the nonreserved data is saved so that it can be installed back into the module after the battery pack is put back into the original state with a new SENC file (discussed in the next section). You also want to change *usage* data to original values so th at all production battery packs do not report that they have been used. To make this Golden GG file, do the following:

1. Ensure that the *Engineering Perfect* battery pack is still connected to the EV2300 and that the EV software for the applicable device is open.
2. Go to the Data Flash screen in the EV software, and click the Read All button.
3. Select the File pulldown menu, click Export, and chose a (*.gg) file name for saving the prelearned defaults (example: optimized.gg).
4. Open the saved GG file from step 3 in a text editor such as Notepad, and change the value of Update Status from 06 to 02, which indicates that the parameters are learned but the Impedance Track feature is disabled (as should be the case for a new pack prior to calibration). Also, reset the *Cycle Count* field to 0 as shown in Figure 17.

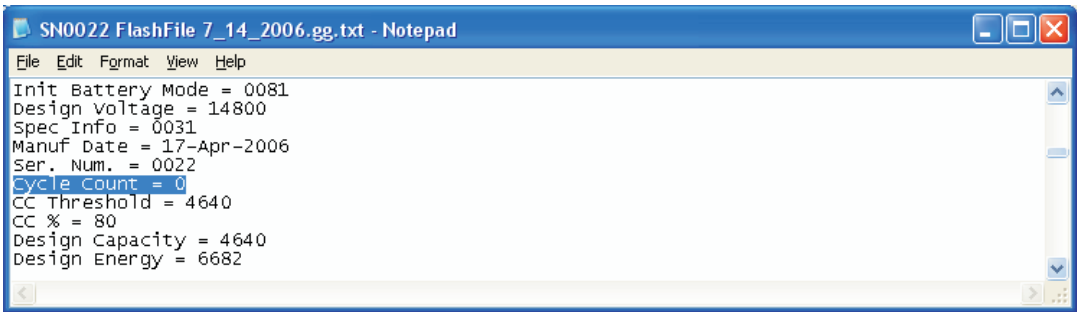


Figure 17. Cycle Count Modification in GG File Using Notepad

5. Save the file. This file is used in the following discussion.

It is assumed that the proper Chemistry Support SENC file has been determined for this application during the Engineering and Development Phase of this project. For most applications (LiCoO2/graphitized carbon chemistry), the default SENC file for the applicable device (e.g., bq20z80, bq20z90, or bq20z70) is used. For more information on multichemistry support. see the TI application report *Support of Multiple Li-Ion Chemistries With Impedance Track™ Gas Gauges* (SLUA372).

The following instructions explain how to install the original chemistry supported SENC file into the *Engineering Perfect* battery pack. Do not worry about losing all the static data from this pack because it was stored as discussed previously.

1. Go to the product folder for the device being used in this application.
   Some Examples:
   a. For the bq20z70 go to: *bq20z70 Tools and Software Section*
   b. For the bq20z80 go to: *bq20z80 Tools and Software Section*
   c. For the bq20z90 go to: *bq20z90 Tools and Software Section*
2. Click on the Multi-Chemistry Support Software zip file pertaining to the device being used:
   Some Examples:
   a. For the bq20z70 go to: *bq20z70-V101 Multiple Li-Ion Chemistries Software*
   b. For the bq20z80 go to: *bq20z80-V102 Multiple Li-Ion Chemistries Software*
   c. For the bq20z90 go to: *bq20z90-V102 Multiple Li-Ion Chemistries Software*
3. Download the applicable zip file and extract to a temporary directory. An example would be C:\Temp\sluc058.zip
4. Ensure that the *Engineering Perfect* battery pack is still connected to the EV2300 and that the EV software for the applicable device is open. Then go to the Pro screen in the EV software as shown in Figure 18.

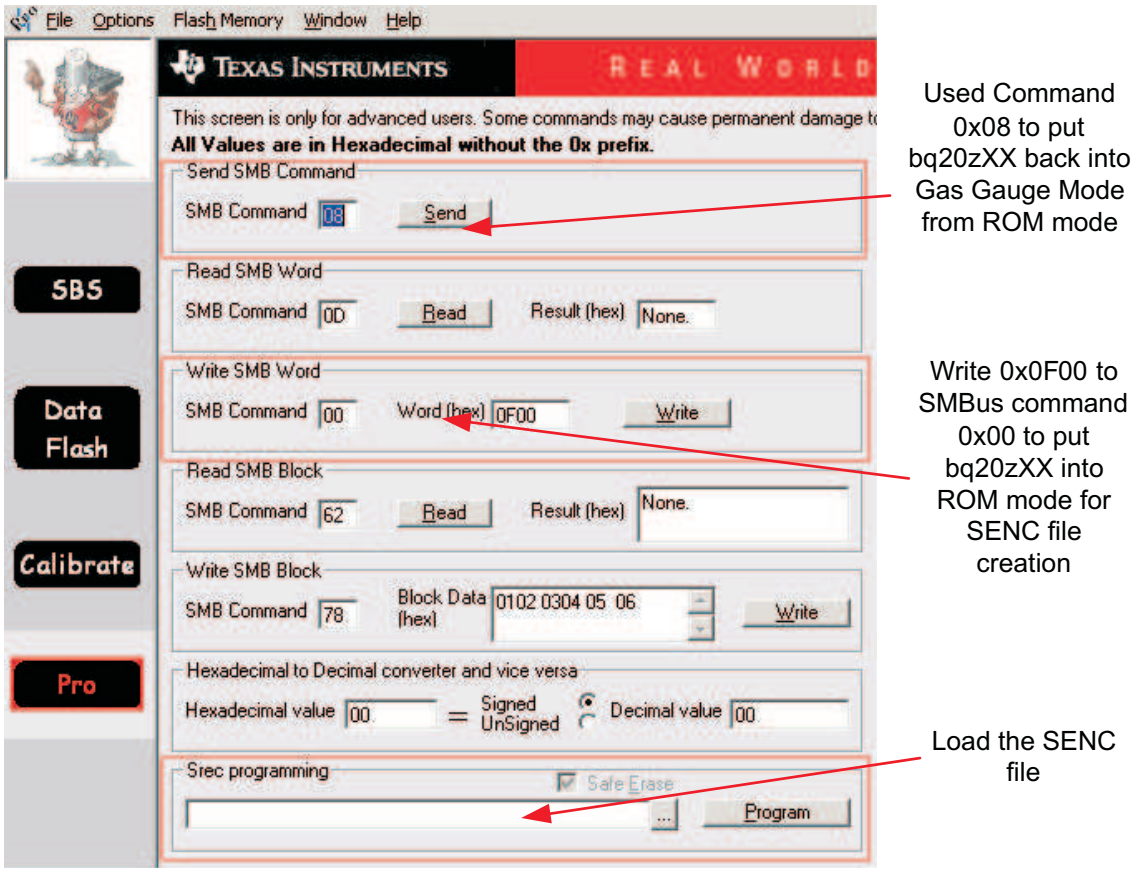


Figure 18. EV Software Pro Screen

5. Ensure that *Write SMB Word* frame has the SMBus Command set to 0x00 and the SMBus Word set to 0x0F00. If they are not, then change them.
6. Then click *Write*. This puts the bq20zxx module into ROM mode to prepare for writing the SENC file created in the previously discussed section.
7. Write the SENC file to the *Engineering Perfect* pack by clicking the browse () button in the *Srec programming* frame.
8. In the file manager that pops up, locate and select the previously saved SENC file created in the previously discussed section.
9. Then click the *Program* button. The software will indicate when finished.
10. After writing is finished, ensure that the **SMB Command** is 0x08 in the *Send SMB Command* frame. If it is not, then change it to 0x08.
11. Click the *Send* button. This puts the bq20zxx back into Gas Gauge mode. Your factory default SENC file is now loaded.

24.4.147.9 Creating the Golden Image File The final step in this process is creating the *Golden* Image file. This file includes all the static data in the data flash that is constant from one smart battery module to the next. It also has all the reserved data and *usage* data set to default states to ensure that all production packs start out in a new state. This process is mandatory for new designs. Without this process the Impedance Track Algorithm may not function properly. Follow these steps to create this file:

1. Ensure that the *Engineering Perfect* battery pack is still connected to the EV2300 and that the EV software for the applicable device is open. Then go to the Data Flash screen, open the *File* pulldown menu, and select *Import*.
2. In the file manager that pops up, locate and select the Golden GG file created in the preceding section and click the *Write All* button.

3. The *Engineering Perfect* battery pack now has all *Golden* data in it. The next step is to retrieve that data into a *Golden* image file.
4. Run the Data Flash reading software in the bqTester suite by double-clicking the TesterDFReader icon. The Data Flash reader screen appears as shown in Figure 19.

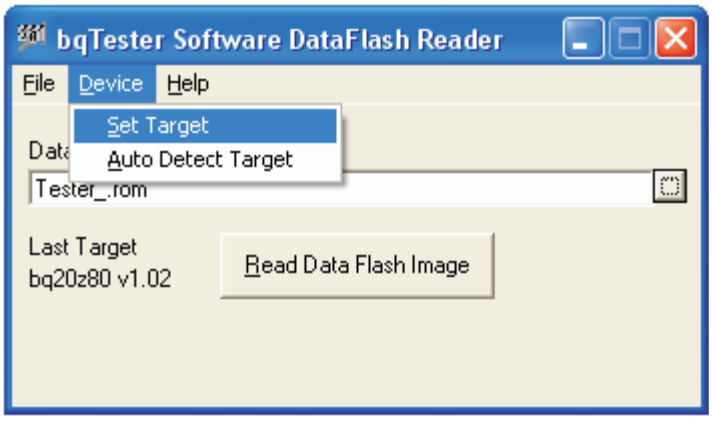


Figure 19. Data Flash Reader Screen

5. Select the device type being read from the Device pulldown menu.
6. Type in a complete path and file name with a .rom extension in the dialog box or click the browse button (). This is the file that contains the *Golden Image*.
7. Click the *Read Data Flash Image* button. This causes the software to read the data flash information from the bq20zxx-based smart battery module and store it in this file. This .rom file is now the *golden* data flash image file which is used to program all other similar bq20zxx-based smart battery modules in the production process.

24.4.147.10 Running the bqTester Software Follow all instructions in Section 1 to install the software. After installation, double-click the bqTester icon on the PC desktop or launch the bqTester program from the Start menu. The single site tester main window appears as shown in Figure 20. Press the *Unlock Configuration button*. The default password is *bq20z80*. After entering the default password, two new buttons appear on the single site tester screen as shown in Figure 21. They are Global Configuration and VTI configuration.

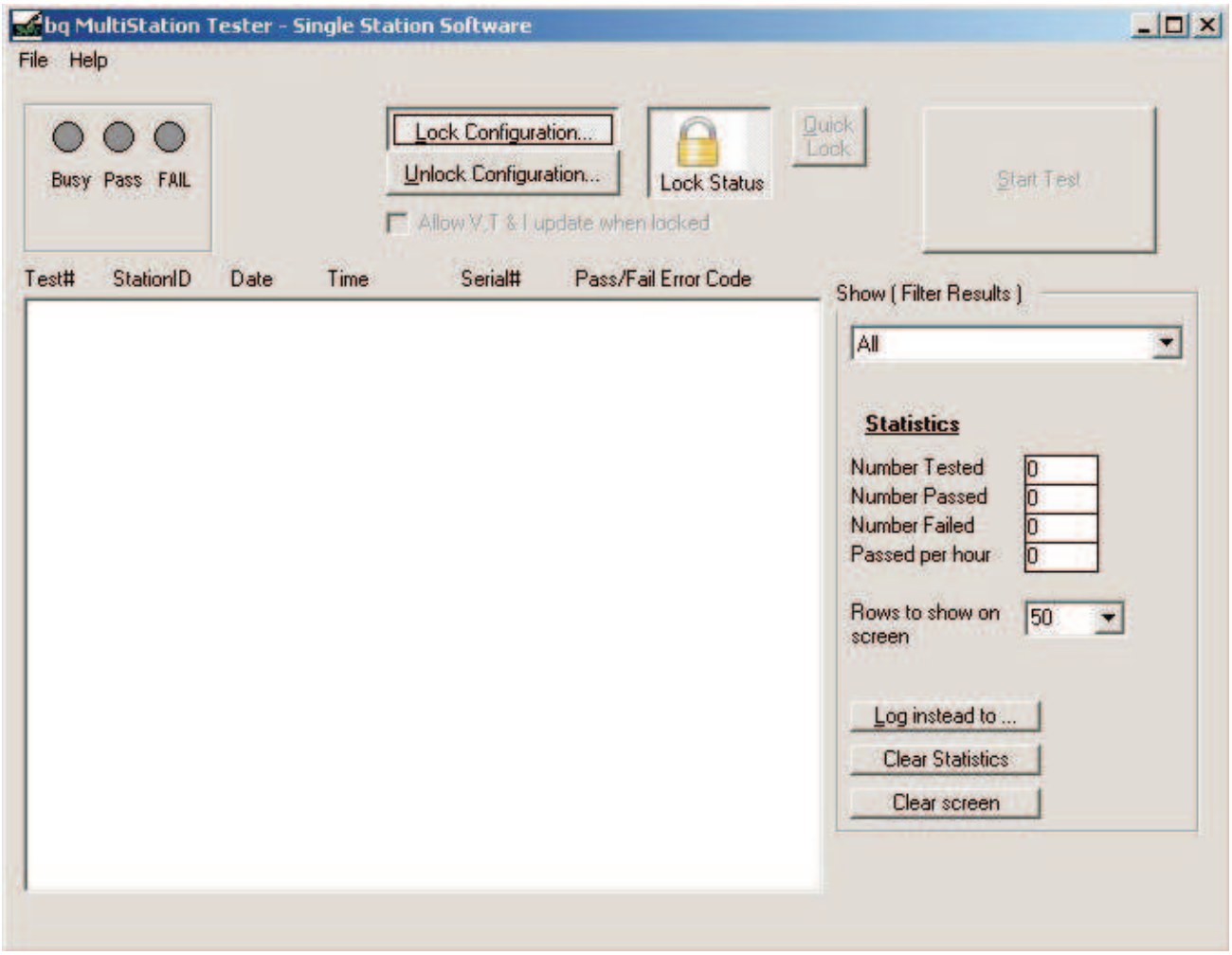


Figure 20. bqTester Main Window

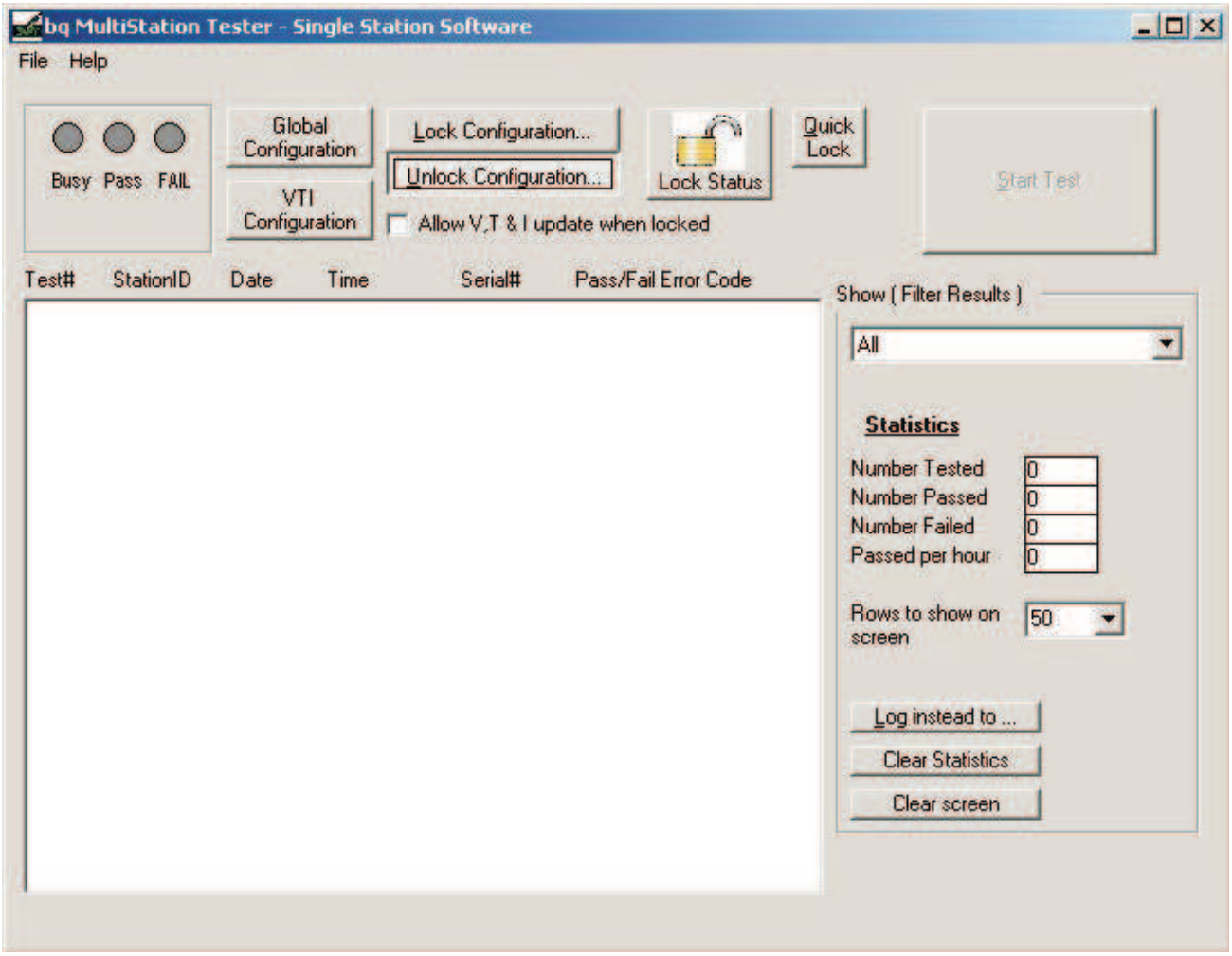


Figure 21. bqTester Main Window Unlocked

Setting Global Configuration Values

Pressing the Global Configuration button causes the bqTester Configuration window to be displayed as shown in Figure 22. In the global configuration screen, all numeric values are specified in signed decimal except for the serial number field which is unsigned with a maximum value of 65535.

24.4.148.11 Current Sense Resistor This box contains two values. Enter the value of the sense resistor used in the Impedance Track-based smart battery pack in the Sense Resistor field. This value is entered in units of milliohms. Enter the desired acceptable percent error that the sense resistor can differ from the value listed in the Sense Resistor field in the % Error field. Note that the default value for this field is 25%. This test is intended only as a rough test to ensure that the sense resistor is mounted and not shorted; it is not intended to be a highly accurate test of the sense resistor value. This value must be specified as a positive integer value.

24.4.148.12 Voltage Reference/FSV This box contains two values. The tester calibrates the voltage gain by manipulating the Full Scale Voltage Reference. Do not change the values in these fields.

24.4.148.13 Temperature Maximum Offset This box contains one value and is in units of 0.1°C. Enter the maximum amount of offset that can be put into the module being tested, either positive or negative from 0. The default value of this field is 20, meaning that the calibrated offset entered in the data flash cannot exceed positive or negative 2°C.

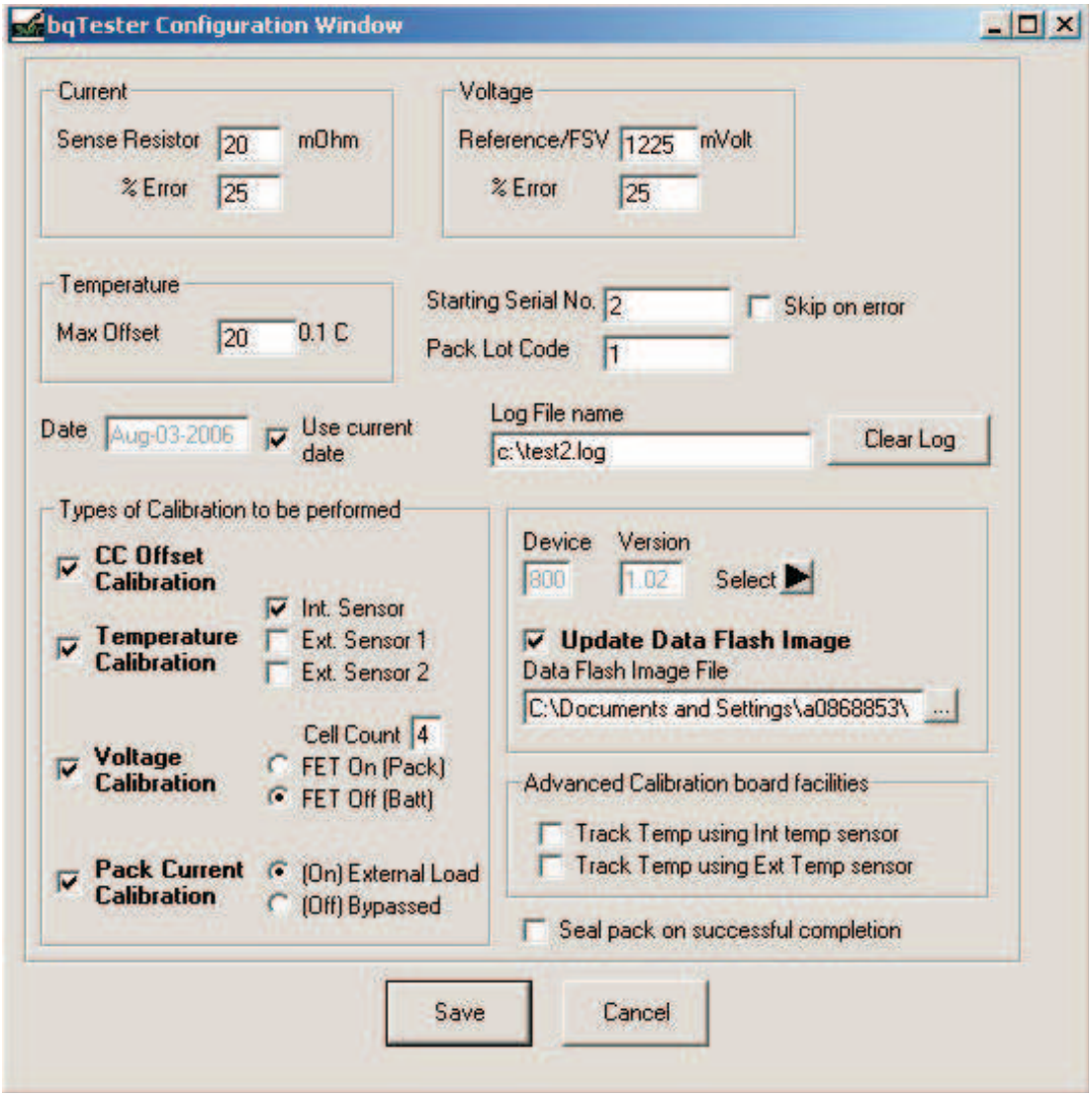


Figure 22. Global Configuration Window

24.4.148.14 Starting Serial Number Enter the value for the serial number of the first Impedance Track-based smart battery module to be tested. This number is incremented by one as each new module is tested. If the Skip On Error check box is checked, the number is not incremented in the case of a module that fails the test. The default for this box is 1. This value must be specified as a positive integer value

24.4.148.15 Pack Lot Code Enter the value for the Pack Lot Code of the group of Impedance Track-based smart battery modules currently being tested. This number does not change until it is changed manually and is programmed into each module tested. This value must be specified as a positive integer value.

24.4.148.16 Date Enter the value for the desired date to be programmed into each Impedance Track-based smart battery module. If the Use Current Date check box is checked, the system date from the computer running the bqTester software is used.

24.4.148.17 Log File Name Enter the complete path and file name to be used for the log file. This file contains all relevant test data for each Impedance Track-based smart battery module tested. If the Clear Log button is pressed, the log file contents are deleted.

24.4.148.18 CC Offset Calibration This is the coulomb counter offset. No user-definable values are in this box. Select this calibration by placing a check in its selection box, or deselect it by removing the check. The default is checked. Note that if this test is disabled, the values from the gold data flash file are used and not the values currently in the part.

24.4.148.19 Temperature Calibration This box shows the currently measured temperature and provides a box for the user to enter the actual temperature as measured by a calibrated meter. If the ambient air temperature changes, this value needs to be updated. This box also offers three different temperature probe selections. The proper selections should be made depending on the application. Temperature calibration can be selected by placing a check in its selection box or deselected by removing the check. The default is checked. Note that if this test is disabled, the values from the gold data flash file are used and not the values currently in the part.

24.4.148.20 Voltage Calibration This box shows the currently measured voltage and provides a box for the user to enter the actual voltage being supplied to the part as measured by a calibrated meter. It also has a box for the user to enter the number of series cells being simulated. The default number of cells is 4. It also has a FET Control selection box. Select Off (Batt), and supply voltage to the simulation resistors as shown in Figure 16 (this configuration is the default). Never select On (Pack); it is only included for possible future use. To select voltage calibration, place a check in its selection box, or deselect it by removing the check. The default is checked. Note that if this test is disabled, the values from the gold data flash file are used and not the values currently in the part.

24.4.148.21 Pack Current Calibration This box shows the currently measured current and provides a box for the user to enter the actual current being supplied to the part as measured by a calibrated meter. It also has a FET Control selection box. Always select On (External Load) and supply current to the Pack– and 1N (Batt–) inputs of the bq20zxx-based smart battery pack as shown in Figure 16 (this configuration is the default). Never select Off (Bypassed); it is only included for possible future use. To select Pack Current calibration, place a check in its selection box, or deselect it by removing the check. The default is checked. Note that if this test is disabled, the values from the gold data flash file are used and not the values currently in the part.

24.4.148.22 Device and Version The correct Device and Version must be selected using the select () button. Once the select button is pressed, select the proper device and firmware version of the modules to be tested form the dialog box that appears. If the device or version desired is not available, check the Texas Instruments Web site for an updated version of the bqTester software in the bqTester tool folder:

http://focus.ti.com/docs/toolsw/folders/print/bqtester.html

Advanced Information: For special/custom parts, it is possible that the part can be added to the file that holds all allowed parts compatible with bqTester. Using this option is sometimes tricky. It is recommended that TI be contacted before using this option to ensure that the bqTester has been tested with the requested device. The file to be edited is called *Targets* and is located in the directory that bqTester was installed. This file is shown in Figure 23.

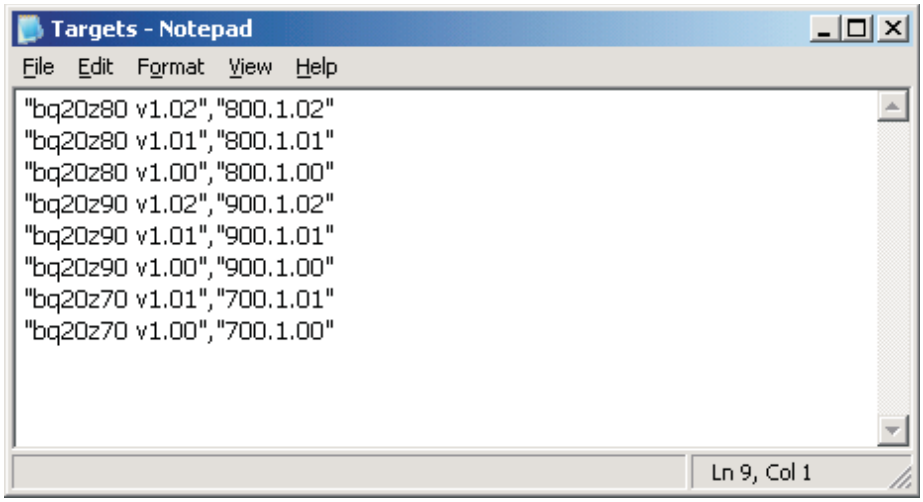


Figure 23. Targets File

24.4.148.23 Data Flash Image File Input the location of the data flash Golden file that will be stored in all parts that will be tested when running the bqTester.exe program. Clicking the browse (…) button gives the option to browse for the Golden image file. If the *Update Data Flash Image* check box is not checked, then no data flash image will be installed in any parts. It is always recommended that an Image file be used.

24.4.148.24 Advanced Calibration Board Facilities This frame contains two check boxes. These check boxes are not currently supported for single site testing. They are for use with the HPA169 calibration board when that functionality is added. Both should remain unchecked when using the single site tester software.

24.4.148.25 Seal Pack on Successful Completion If checked, then the module is sealed on completion of the test.

24.4.148.26 Save Clicking the Save button causes the current configuration settings to be saved.

VTI Configuration

Clicking the VTI Configuration button causes the VTI configuration box to be displayed as shown in Figure 24.

Figure 24. VTI Configuration Box

24.4.149.27 Voltage Enter the voltage supplied by Power Supply 2 as seen in Figure 16. This voltage must be extremely stable. Set the voltage at 3.6 volts times the number of cells being simulated (e.g., 4 x 3.6 = 14.4 v for 4 cells). Measure this voltage with a calibrated meter.

24.4.149.28 Temperature Enter the temperature near the module under test which has been measured with a calibrated meter.

24.4.149.29 Current Enter the current supplied by Power Supply 1 as seen in Figure 16. A reasonable current setting is 2 amperes. This current value must be extremely stable. This voltage should be measured with a calibrated meter.

24.4.149.30 Save Pressing the Save button causes the currently recorded values for V, T, and I to be saved.

Running the Test

24.4.150.31 Locking the Configuration The test cannot be started until the Lock Configuration button has been clicked. First, check or uncheck the box called *Allow V, T, and I update while locked*. If selected, the user is able to change actual values for voltage, temperature, and current even though the configuration has been locked. If not selected, the user is unable to alter these values without unlocking the configuration. Note that the configuration must be currently unlocked to select this option. Once *Allow V, T, I*= while locked has been selected or deselected, click on *Lock Configuration*. This causes a password dialog to appear. Enter a password, and record it in a safe location for future reference. If you do not wish to enter the password every time the *Lock Configuration* button is pressed, check the box called *Quick Lock*. This causes555 the configuration to be locked with the current password. Notice that the Lock Status icon changes from an open lock to a closed lock. Also notice that the *Start* button is now active and testing can now begin.

24.4.150.32 Starting the Test Click on the *Start* button to run the test. The software displays a busy indication and then indicates Pass or Fail. The software also displays information about each bq20zxx-based smart battery module tested and its Pass or Fail status. This same information is also recorded in a log file. The log file can be specified by pressing the *Log Instead To*… button. If a module fails, an error code is displayed and logged. Appendix A defines the error codes for the bqTester software. The information on the screen can be cleared by pressing the *Clear Screen* button. The statistical information can be cleared by pressing the *Clear Statistics* button.

24.5 Software Change Recommendations

1. Add new files when new functionality is added. Do not edit existing files.
2. Edit modSerial.bas to change the way serial numbers are generated.
3. Examples of how to use existing functions to read/write gas gauge constants can be found in the modGGDF.bas file. It is recommended that end-users use these functions for data flash access instead of writing their own.

Error Code Definitions

Table 1. Error Code Definitions

Error Code	Error #	Description	Most Probable Cause	Possible Action
NO_ERROR	0	Successful (No errors)		
LOST_SYNC	1	EV2300 lost synchronization	EV2300 has outdated firmware or drivers are outdated.	Contact TI to get EV2300 with latest firmware. Ensure latest drivers for EV2300 installed.
NO_USB	2	USB Connection Missing	No EV2300 is connected.	Close program, reboot, and connect EV2300 first.
BAD_PEC	3	Bad PEC on SMBus	Possible Bad hardware.	Replace EV2300 / target board
WRONG_NUM_BYTES	5	Unexpected number of bytes sent/received	Unexpected hardware behavior.	May need assistance from TI
T2H_UNKNOWN	6	SMBus communication terminated unexpectedly / timed out or the bus was busy.	Wrong kind of target connected or target timing is off Trim oscillator	make sure that the target mode accepts the SMB command being sent
INCORRECT_PARAM	7	Invalid parameter type passed to function – especially Variant argument.	Incorrect parameter in call to function. Software Bug or overflow	Contact TI
TIMEOUT_ERROR	8	USB Timeout	No response on USB	EV2300 or driver problems or software is not supposed to wait for a response.
INVALID_DATA	9	AssemblePacket could not build a valid packet	Bad data / bad packet. Software found problem with data	Possible version incompatibility between BqTester and Module under test.
ERR_UNSOLICITED_PKT	10	Found an unsolicited non-error packet when looking for error packets	Unexpected packet received. The packet may be a response from a previous transaction that failed or that did not check the response.	Make corrections to software
COMPARE_DIFFERENT	11	Comparison failed and data read is different from srec	Flash comparison results in mismatch. Possible Flash failure or SMBus failure.	Module under test Flash failure
BQ80XRW_OCX_INTERNAL_ERROR	12	Problems with pointers being NULL etc.	Possible software bug or overflow.	Contact TI
USER_CANCELLED_OPERATION	34	User clicked on cancel button on progress bar dialog		
DF_CHECKSUM_MISMATCH	51	Data Flash checksum mismatch	Flash comparison results in mismatch. Possible Flash failure or SMBus failure.	Module under test Flash failure
IF_CHECKSUM_MISMATCH	52	Instruction Flash checksum mismatch	Flash comparison results in mismatch. Possible Flash failure or SMBus failure.	Module under test Flash failure
OPERATION_UNSUPPORTED	53	Unsupported type	Software problem	Check that Module under test and bqTester versions are compatible. Then contact TI
ERR_TOO_MANY_QUERIES	81	Not used		
ERR_BAD_QUERY_ID	82	Not used		

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
BAD_CRC	83	Packet was corrupted during USB communication	Too much noise or bad connection	
ERR_TOO_MANY_RESPONSES	84	Not used		
ERR_NO_QUERIES_TO_DELETE	85	Not used		
ERR_QUERY_UNAVAILABLE	86	Not used		
ERR_NO_RESPONSES_TO_DELETE	87	Not used		
ERR_RESPONSE_UNAVAILABLE	88	Not used		
ERR_TMMT_NO_RESPONSE	90	Not used		
T2H_ERR_TIMEOUT	92	SMBus communication terminated unexpectedly / timed out or the bus was busy.	Wrong kind of target connected or target timing is off Trim oscillator	make sure that the target mode accepts the SMB command being sent
BUS_BUSY	94	SMBus communication terminated unexpectedly / timed out or the bus was busy.	Wrong kind of target connected or target timing is off Trim oscillator	make sure that the target mode accepts the SMB command being sent
T2H_ERR_BAD_SIZE	95	SMBus communication terminated unexpectedly / timed out or the bus was busy.	Wrong kind of target connected or target timing is off Trim oscillator	make sure that the target mode accepts the SMB command being sent
ERR_BAD_PAYLOAD_LEN	97	Packet was corrupted during USB communication or software sent in a bad packet	Bad USB connection	Check Version Compatibility and USB cable
ERR_TMMT_LIST_FULL	98	Not used		
ERR_TMMT_BAD_SELECTION	99	Not used		
UNKNOWN	100	Unexpected/unknown error		Outdated software Contact TI
UNEXPECTED_ERROR	110	Should not happen	Unexpected error	Hardware not expected to respond to this error
OUT_OF_MEMORY	111	Not enough memory on PC		Install more memory
SREC_OPEN_FAIL	221	Srec specified does not exist or cannot be opened	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqTester software and Module under Test.
SREC_BAD_START_RECORD	222	Srec not in expected format	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqTester software and Module under Test.
SREC_UNKNOWN_TYPE	223	Srec not in expected format	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqTester software and Module under Test.
SREC_BAD_CHECKSUM	224	Srec not in expected format	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqTester software and Module under Test.
SREC_BAD_RECORD_COUNT	225	Srec not in expected format	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqTester software and Module under Test.
SREC_DEV_MISMATCH	226		SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqTester software and Module under Test.
CONFIG_OPEN_FAIL	227	Config file not found / cannot be opened		Redo StationSetup.exe configuration
CONFIG_UNEXPECTED_EOF	228	Config file not found / cannot be opened		Redo StationSetup.exe configuration
CONFIG_BAD_FORMAT	229	Config file format incorrect		Redo StationSetup.exe configuration

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
PCFG_DEVVER_MISMATCH	231	Config file device version not compatible		Ensure version compatibility between bqTester software and Module under Test.
PCFG_DEV_MISMATCH	232	Config file device not compatible		Ensure version compatibility between bqTester software and Module under Test.
PCFG_SRECDEVVER_MISMATCH	233	Srec not compatible with current hardware device		Ensure version compatibility between bqTester software and Module under Test.
PCFG_SRECDEV_MISMATCH	234	Srec not compatible with current hardware device		Ensure version compatibility between bqTester software and Module under Test.
BCFG_DEVVER_MISMATCH	235	Srec not compatible with current hardware device		Ensure version compatibility between bqTester software and Module under Test.
BCFG_DEV_MISMATCH	236	Srec not compatible with current hardware device		Ensure version compatibility between bqTester software and Module under Test.
SMBC_LOCKED	260	Unused but reserved for backward compatibility		
	516	Unused but reserved for backward compatibility		
T2H_NACK	772	No response from target	Target not connected/not powered	Connect target and check is correct power is applied
SMBD_LOW	1028	Unused but reserved for backward compatibility		
SMB_LOCKED	1284	Unused but reserved for backward compatibility		
ERR_NOTHINGTODO	5001	Calling the function with specified values resulted in nothing being done		
ERR_VOLTAGE_LESSTHANZERO	5002	Specified Voltage must be greater than 0		
ERR_TEMPERATURE_LESSTHANZERO	5003	Specified temperature must be greater than 0		
ERR_CURRENT_EQUALSZERO	5004	Specified current cannot be 0		
ERR_NOT_IN_CAL_MODE	5010	Gas gauge was not in Calibration mode/ could not be put in calibration mode		
ERR_CALIBRATION_IN_FIRMWARE_ FLASHWRITE	5020	Error writing flash in calibration mode		
ERR_CALIBRATION_IN_FIRMWARE_AFE	5021	Error in AFE calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ PACKV	5022	Error in Pack voltage calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ PACKG	5023	Error in Pack gain calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ VGAIN	5024	Error in Voltage gain calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ CCIGAIN	5025	Error in Current gain calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ TMPOFFEXT1	5026	Error in external temperature 1 offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ TMPOFFEXT2	5027	Error in external temperature 2 offset calibration	Value too large (Overflow) in firmware	

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
ERR_CALIBRATION_IN_FIRMWARE_TMPOFFINT	5028	Error in internal temperature offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ADCOFF	5029	Error in ADC offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_BRDOFF	5030	Error in Board offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_CCIOFF	5031	Error in CC offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_RSVD0	5032	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_RSVD1	5033	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_RSVD2	5034	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_RSVD3	5035	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_RSVD4	5036	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_RSVD5	5037	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_RSVD6	5038	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_UNDEFINED	5039	Unknown error code returned by hardware	Software is obsolete	
ERR_DF_RD_REQ_B4_WR	5041	Data flash cannot be written before reading the remaining values in a given class		
ERR_INVALID_DATA_ENTERED	5042	Invalid data entered on screen		
ERR_USB_ACQUIRE	5043	EV2300 is locked by another thread	Attempting to do multiple transactions possibly from different windows in background at the same time. Could also be a software problem. Stop scanning in SBS.	
NVALID_FILENAME	65537			Check File Name for Rom File and Log File
DEVICE_VERSION_MISMATCH	65538	Incompatible device/version		Check Connections. Verify version compatibility between bqTester software and Module under Test.
RETURN_TO_ROM_FAILED	65539	Gas gauge could not be put in Rom mode	Hardware incompatibility	Check Connections. Verify version compatibility between bqTester software and Module under Test.
RUNGG_FAILED	65541	Gas gauge could not exit ROM mode	Hardware incompatibility	Check Connections. Verify version compatibility between bqTester software and Module under Test.
WRITEFLASH_GG_FAILED	65542	Writing to flash failed	Data Flash Failure	Module Repair
CALIBRATE_FAILED	65543	Calibration failed	Module hardware failure or Configuration failure	Module Repair or Check Testing Configuration Settings
POST_CAL_CHECKS_FAILED	65544	Post calibration checks failed	Module hardware failure or Configuration failure	Module Repair or Check Testing Configuration Settings
WRITESERIAL_FAILED	65545	Write serial number failed	Data Flash Failure	Module Repair/Retry Test
ERR_UNEXPECTED	65552	Unexpected value/response	Software does not know how to handle this	

Table 1. Error Code Definitions (continued)

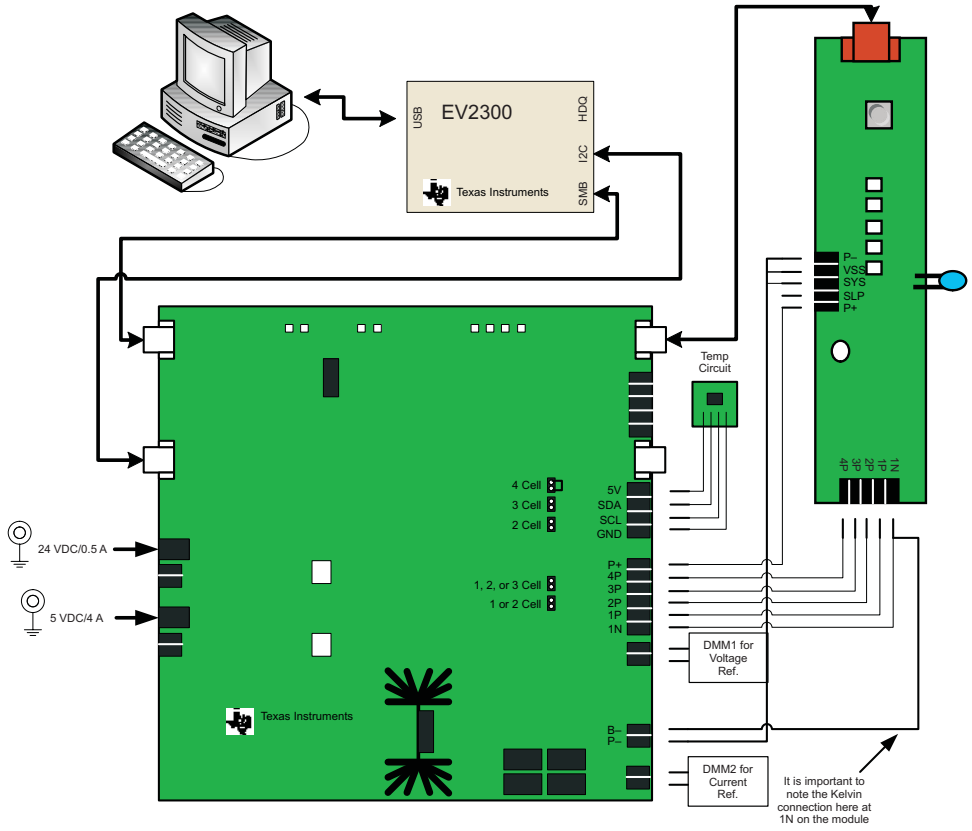
Error Code	Error #	Description	Most Probable Cause	Possible Action
ERR_FILE	65553	Error opening/processing File	Wrong File location settings.	Check all File location settings in bqTester Software
ERR_NOT_IN_ROM	65554	GG not in ROM mode when expected – communication failure?	Gas gauge could not be put in ROM	Check Connections. Verify version compatibility between bqTester software and Module under Test.
ERR_ENTER_CALMODE	65555	Cannot put GG in Cal mode	Gas gauge could not be put in Calibration mode	Check Connections. Verify version compatibility between bqTester software and Module under Test.
ERR_CUSTOM_FUNC	65556	User defined function returned error		
BAD_FILE_FORMAT	65557	Header bad or format bad	Bad image file format	
ERR_WRITE_MFG_DATA	65558	Failed to write manufacturer data	Data Flash Failure	Module Repair/Retry Test
ERR_READ_DEV_VER	65559	Communication error reading device version	Hardware incompatibility	Check Connections. Verify version compatibility between bqTester software and Module under Test.
CAL_VOLT_LESSTHANZERO	65600	Calibration voltage must be greater than 0	On screen values incorrect	Verify VTI and Configuration Settings
CAL_TEMP_LESSTHANZERO	65601	Calibration current must be greater than 0	On screen values incorrect	Verify VTI and Configuration Settings
CAL_CURR_LESSTHANZERO	65602	Calibration current must be greater than 0	On screen values incorrect	Verify VTI and Configuration Settings
WRITEFLASH_ROM_FAILED	65560	Failed to write flash while in ROM mode		
SENSE_RES_CAL_HIGH	65570	Sense resistor value too high in post cal checks	Sense Resistor Hardware Failure, Connection Problem, Setting Problem, or HPA169 Power Supply Problem	Verify Sense Resistor Value, check current supply connections, and verify VTI and Configuration Settings. Try increasing tolerances if possible
SENSE_RES_CAL_LOW	65571	Sense resistor value too low in post cal checks	Sense Resistor Hardware Failure, Connection Problem, Setting Problem, or HPA169 Power Supply Problem	Verify Sense Resistor Value, check current supply connections, and verify VTI and Configuration Settings. Try increasing tolerances if possible
VOLT_CAL_HIGH	65580	voltage value too high in post cal checks	Module hardware failure, HPA169 Voltage power supply problem or Configuration failure	Verify Voltage circuit, voltage power supply, VTI, and Configuration Settings. Try increasing tolerances if possible
VOLT_CAL_LOW	65581	voltage value too low in post cal checks	Module hardware failure, HPA169 Voltage power supply problem or Configuration failure	Verify Voltage circuit, voltage power supply, VTI, and Configuration Settings. Try increasing tolerances if possible
TEMP_CAL_HIGH	65590	temperature value too high in post cal checks	Module hardware failure, HPA169 Temperature sensor Failure	Verify VTI settings, and Temperature sensor location
TEMP_CAL_LOW	65591	temperature value too low in post cal checks	Module hardware failure, HPA169 Temperature sensor Failure	Verify VTI settings, and Temperature sensor location
SEAL_CMD_FAILED	65610	Seal command failed	Communication Failure	Check Connections. Verify version compatibility between bqTester software and Module under Test.

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
ERR_READ_CB_INT_TEMP_SENSOR	65611	Error reading internal temperature sensor on HPA169 calibration board	Temperature sensor failure	Verify HPA169 calibration board temperature sensor connections or replace sensor
ERR_READ_CB_EXT_TEMP_SENSOR	65612	Error reading external temperature sensor on HPA169 calibration board	Temperature sensor failure	Verify HPA169 calibration board temperature sensor connections or replace sensor
ERR_CALIBRATION_OUTOFSPEC	65613	Time to recalibrate HPA169 calibration board	VTI calibration Timer expired	Calibrate VTI settings
ERR_TEST_ROUTINE	65614	Reserved		

bqMTester User's Guide

- **FEATURES**
  - Programs and calibrates smart battery modules based on the bq20z80.
  - Calibrates coulomb counter offset, voltage, temperature, and current.
  - Programs serial number, date, pack lot code, and other defaults obtained from a *golden* data image file.
  - Test software is Windows 2000 and Windows XP compatible
  - Data logging feature preserves calibration records.



The bqMTester from Texas Instruments is designed to calibrate and program electronic smart battery modules based on the bq20zXX and future advanced battery gas gauges. The bqMtester consist of a software suite, a maximum of 12 calibration boards (HPA169) and an equal number of communication boards (EV2300).

One EV2300 and one HPA169 calibration board is included in the bqMtester kit when purchased from Texas Instruments. Please refer to the bqMtester product folder for more information: http://focus.ti.com/docs/toolsw/folders/print/bqmtester.html.

Some code modules of bqMtester are written with open source customizability in mind. Contact Texas Instruments to request this source code.

26.1 Installation and Setup

Minimum System Requirements

26.1.151.33 bqMTester Multi Station Tester

- Computer: PC or compatible.
- Operating System: Windows 2000, or Windows XP. Operation with Windows 98SE may be possible, but is untested and unsupported.
- Minimum video resolution is 640 x 480, recommended: 800 x 600 or above.
- 1 available USB port.
- 1 EV2300 USB-Based PC Interface Board for Battery Fuel Gauge Evaluation from Texas Instruments that includes the *USB Tester Ready* label (firmware version 3.1L or greater) This is supplied in the bqMtester kit.. The bqMtester software will verify the EV2300 compatibility as described in section 7.
- 1 Texas Instruments HPA169 Calibration Circuit Board (Supplied in bqMTester Kit).
- For Multi-Station support: 5V/4A and 24V/0.5A power supplies with isolated grounds (not included).
- 10MB available hard drive space.
- Visual Basic version 6.0 with Service Pack 5 is required if user wishes to alter program operation (open source abilities).
- Traceable Digital Multi-Meter (DMM) capable of measuring 2.5A and 20V accurate to less than 1mv and 1mA.
- Traceable Temperature probe accurate to 0.1°C.

26.2 Functional Overview: Exploring How Multi-Stie Tester Works

bqMTester: Multi-Station Tester

The bqMTester software is a suite of programs used as a whole to calibrate and test bq20zXX modules. It has 4 executables. Two of them, StationSetup.exe and TesterDFReader.exe, are used for module test preparation. The other two, bqTester.exe and MultiStationTester.exe, are used for testing. This section discusses the 4 executables as they relate to Multi-Station Testing Theory of Operation.

- **MultiStationTester.exe:** The main test program for multi-site testing. This program can only be run after StationSetup.exe has been run. It requires the calibration board (HPA169). This programs only purpose is to coordinate background bqTester.exe functions and data. It initiates tests, handles priority conflicts, and handles/stores test statistical data received from bqTester.exe.
- **bqTester.exe:** This program is the backbone of the Multi-Station Tester. It performs all the testing. bqTester.exe is a background object that is not visible to the user. There is an instance of bqTester.exe running for each EV2300 test station connected to the PC. The bqMtester (MultistationTester.exe) software calls on bqTester.exe to perform all the calibration and testing. All data from this testing is reported back to bqMtester where it is displayed and logged.
- **StationSetup.exe:** This is the setup program for MultiStationTester.exe. This program must be run prior to running MultiStationTester.exe. The EV2300/Temperature/Test Limits are configured using this program.
- **TesterDFReader.exe:** This program is used to read the “Golden Image File” from an optimized module. This file is then used for production testing with the MultiStationTester.exe program. If a Golden Image File is not used then only calibration data as enabled will be installed in the bq20zXX.

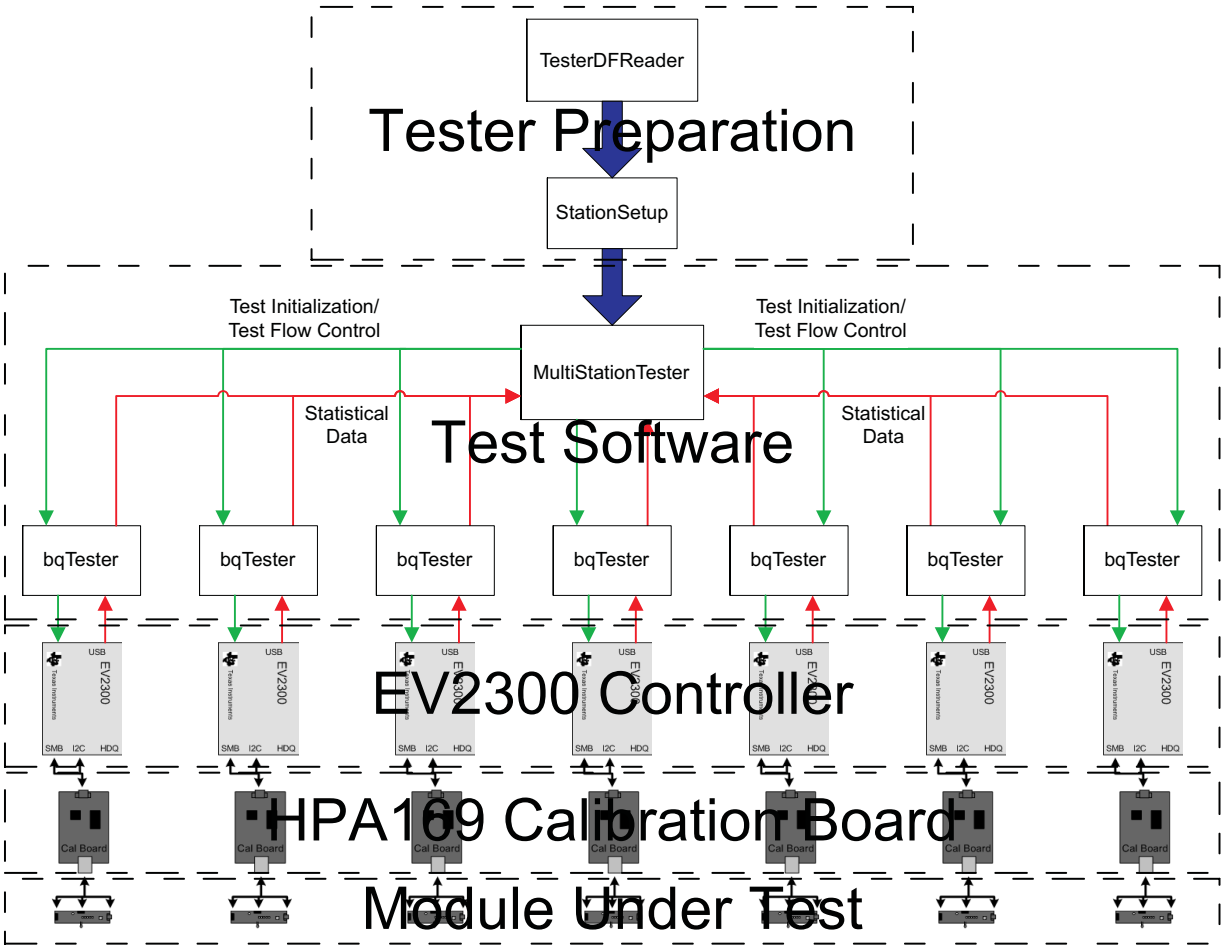


Figure 1. bqMTester Multi-Station Flow

26.2.152.34 bqMtester: Functionality The bqMTester functional procedure is as follows:

1. First you must setup the tester. Install the software and connect all stations to the PC until there are drivers associated with each instance of the tester as explained in chapter 4
2. Then, after a *Golden* pack has been made as described in section 5, the data flash from that *Golden* pack is retrieved and stored to a *Golden Image File* using the TesterDFReader.exe program. This file has optimized data specific to the batteries used for this particular production run that is being tested using bqMtester.
3. The next step is to run the StationSetup.exe file.
   a. This program will first detect all stations and request names for those stations.
   b. Next is a temperature probe setup screen where individual temperature probes are assigned to stations.
   c. Then the program will request calibration specific data and the location of the golden image file so that data can be installed in all gas gauge modules to be tested.
4. Finally the MultistationTester.exe program is run. Here you will:
   a. Update voltage, current, and temperature settings in the Update VTI screen to ensure that the voltage, current, and temperature data from the reference sources used to calibrate are as accurate as possible.
   b. Start testing. Log data will be displayed on the log screens and stored to a file as setup in step 3.

26.2.152.35 bqMtester Multi-Station (bqMultiStationTester.exe): Configuration bqMtester as a multi-station test application requires an HPA169, 2 wall brick power supplies (5V/4A and 24V/0.5A each with isolated grounds), and a user supplied Test Head for every test station. Each station will also require an EV2300 with the firmware compatible with Multi-Station Testing support (denoted by a *USB Tester Ready* label on the top of the EV2300 as seen below):

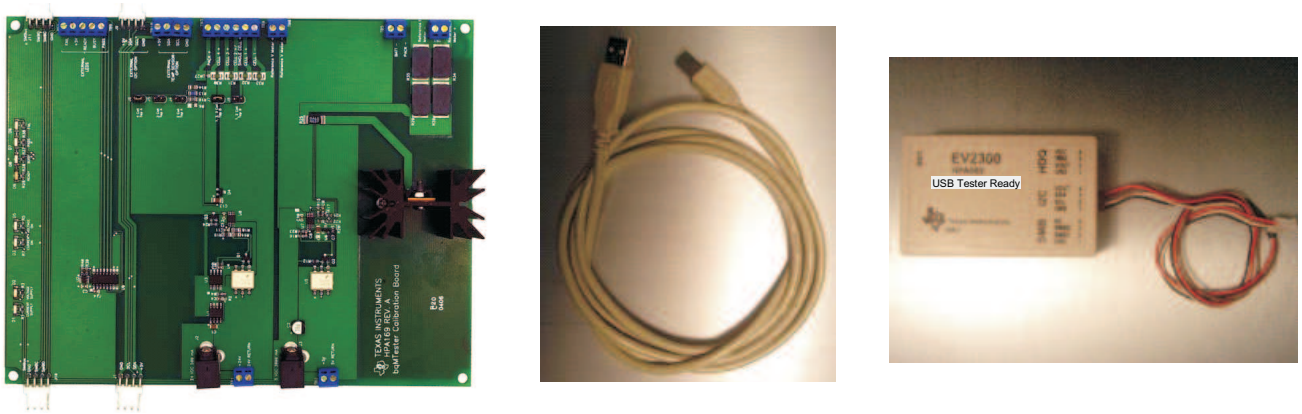
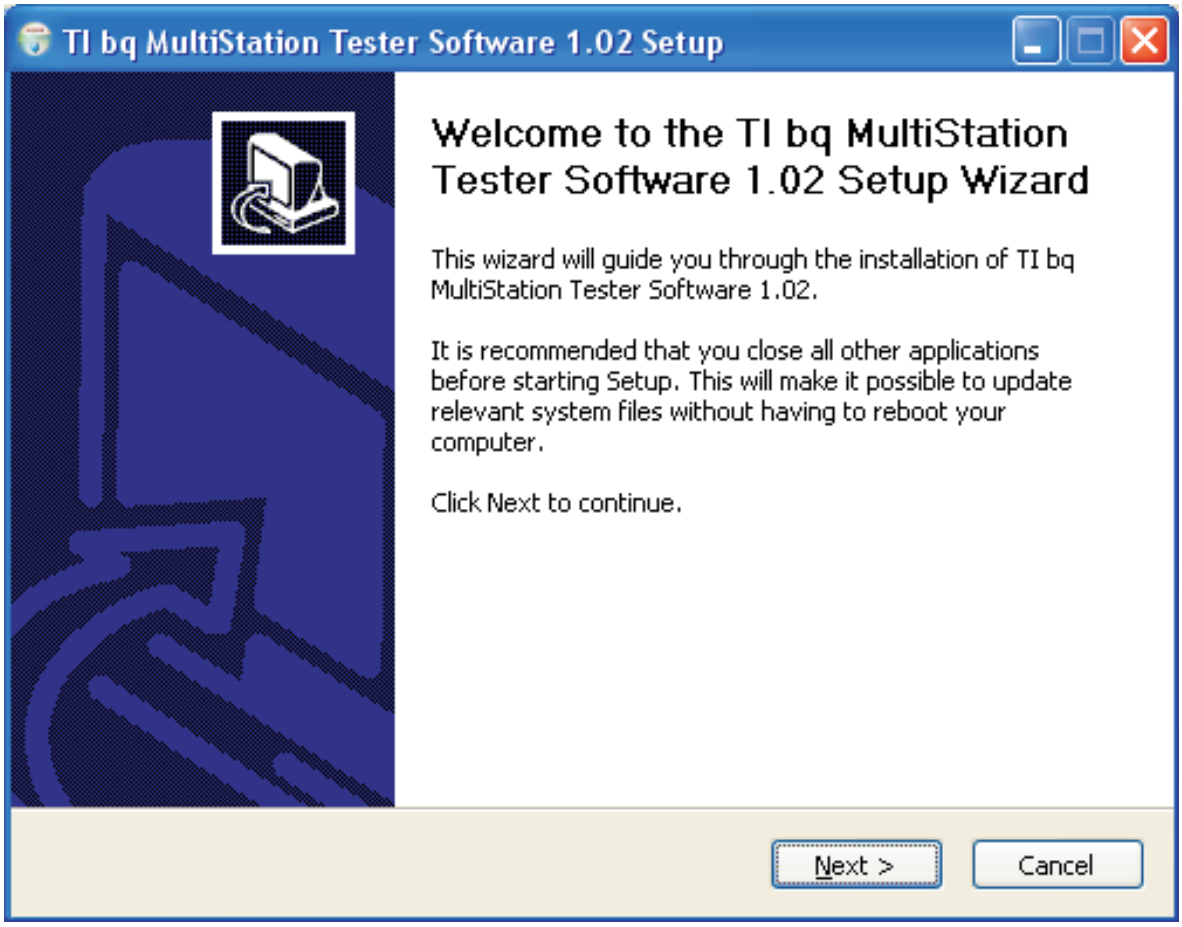


Figure 2. Included Hardware With bqMTester Kit

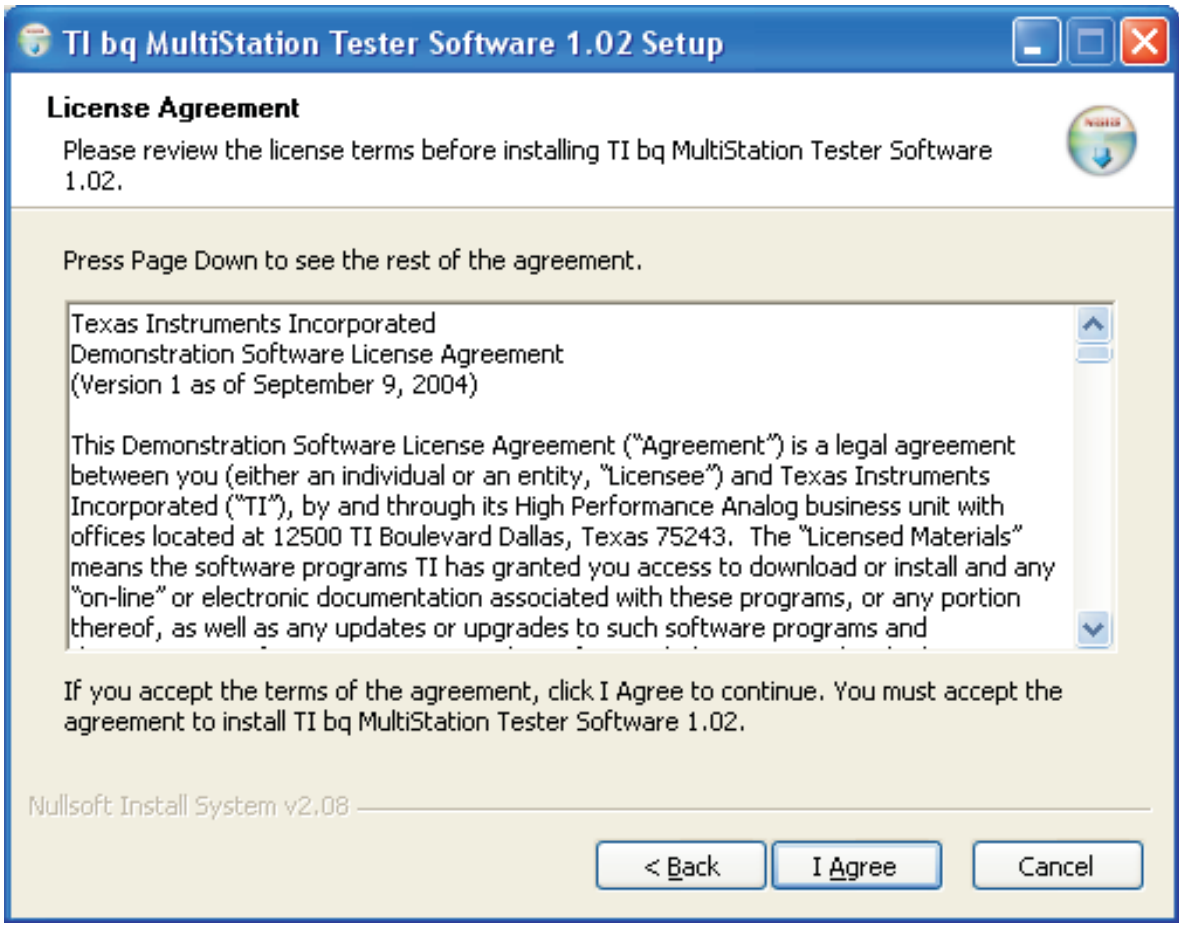
26.3 Software Installation

The **bqMultiStationTester102hSetupWDriver_supports701n702.exe** executable installs all required software, drivers, and DLL files for proper software operation (*102h* indicates the version of the software and may not represent the current version of the Impedance Track device). To install the software:

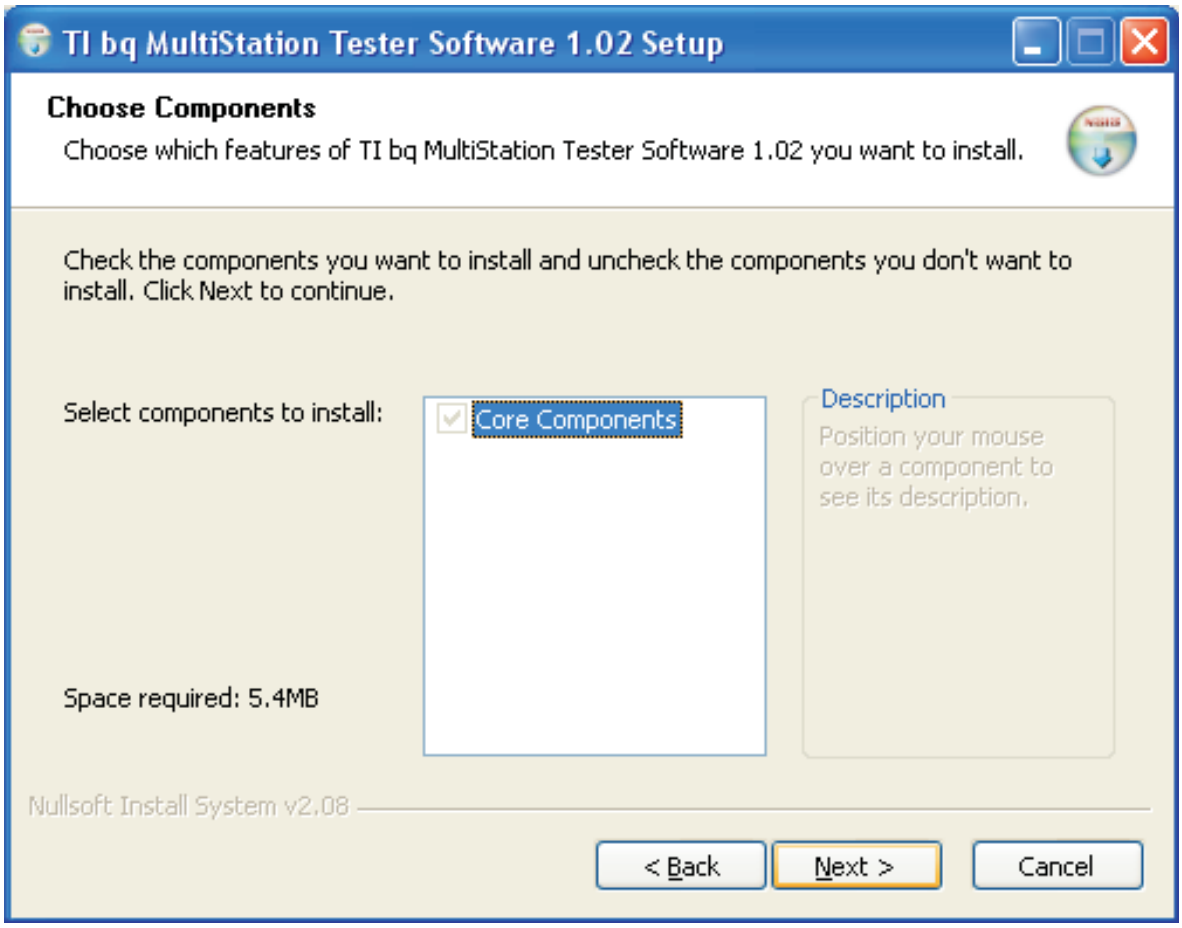
1. **Do Not** connect any EV2300s to the PC before installing software. If any are connected please disconnect them now.
2. It is recommended to check for software in the *bqMtester Tool Folder* on the www.ti.com web site. The Tool Folder is located at:
   http://focus.ti.com/docs/toolsw/folders/print/bqmtester.html
3. If installing software downloaded from the above website then unzip the downloaded file into a temporary directory and go to **Start, Run**, and type:
   C:\Yourdirectory\bqMultiStationTester102SetupWDriver.exe and click **OK** (replace *C:\Yourdirectory* with the location that you unzipped the file). Then go to step 6.
4. If installing software from the CD included in the bqMTester kit then insert the bqMTester CD into your CD drive.
5. Go to **Start, Run**, and type **D:\bqMultiStationTester102SetupWDriver.exe** (assuming D:\ is your CD player) and click **OK**.



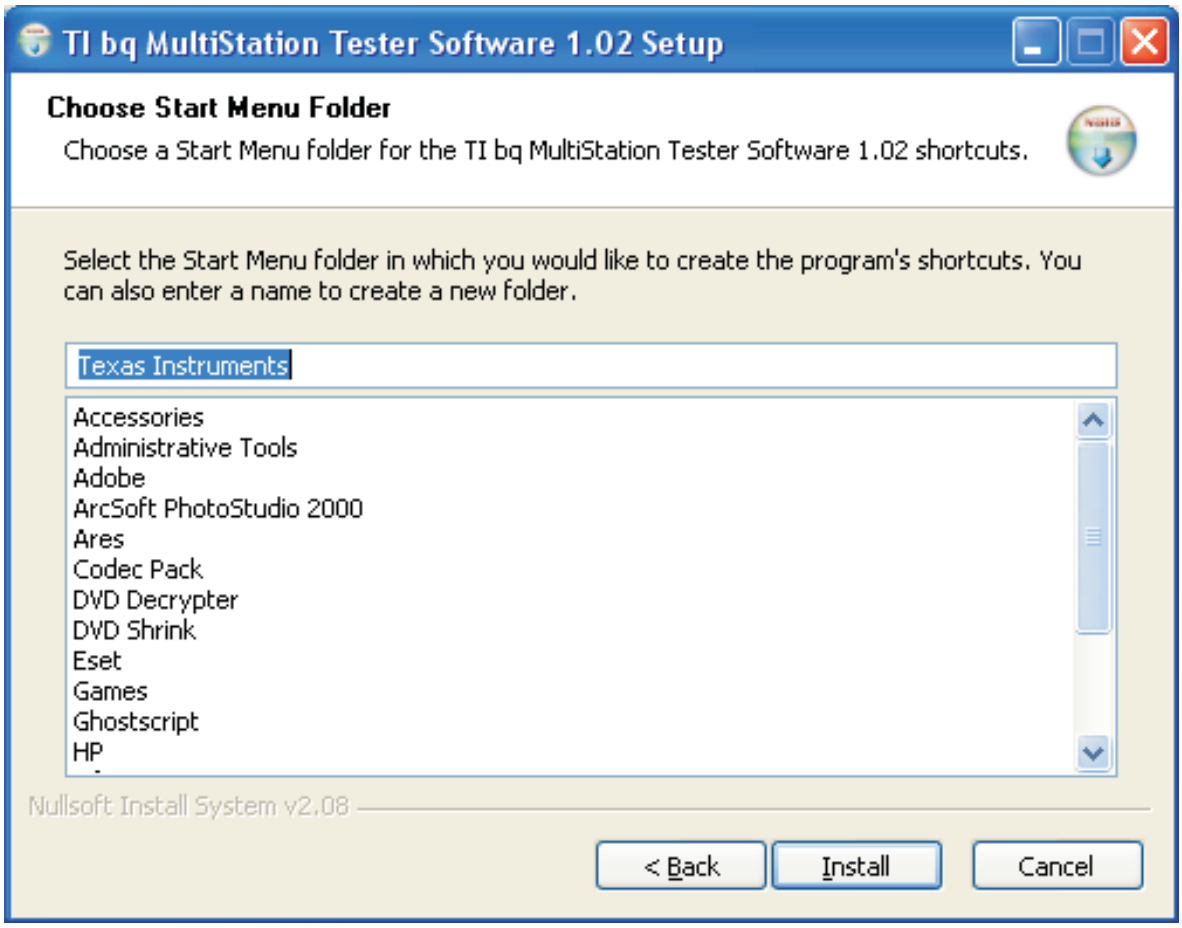
6. Click **Next** at the welcome screen.



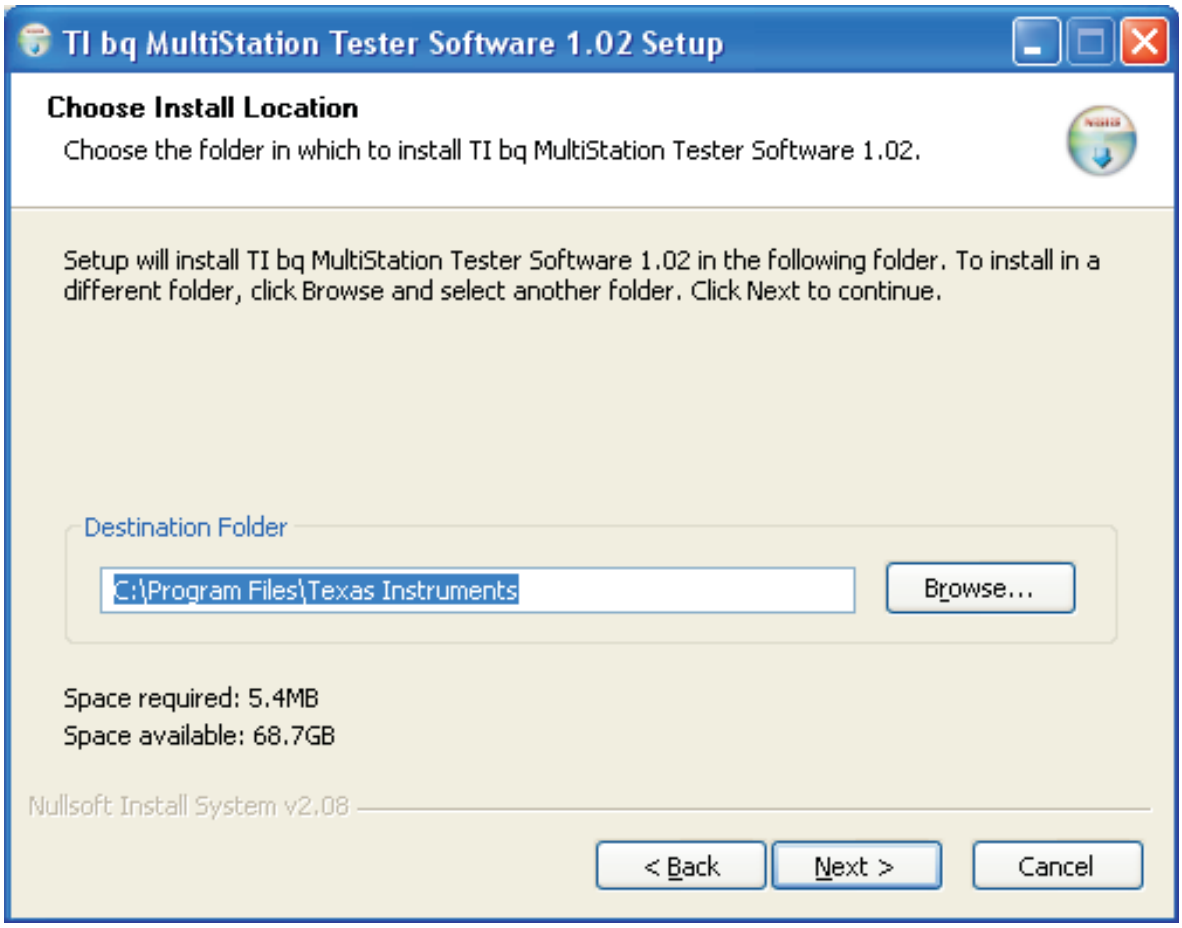
7. Read the License Agreement at the license agreement screen and click **I Agree** when are done if you agree with the terms, otherwise, click **Cancel** and exit the installation software.



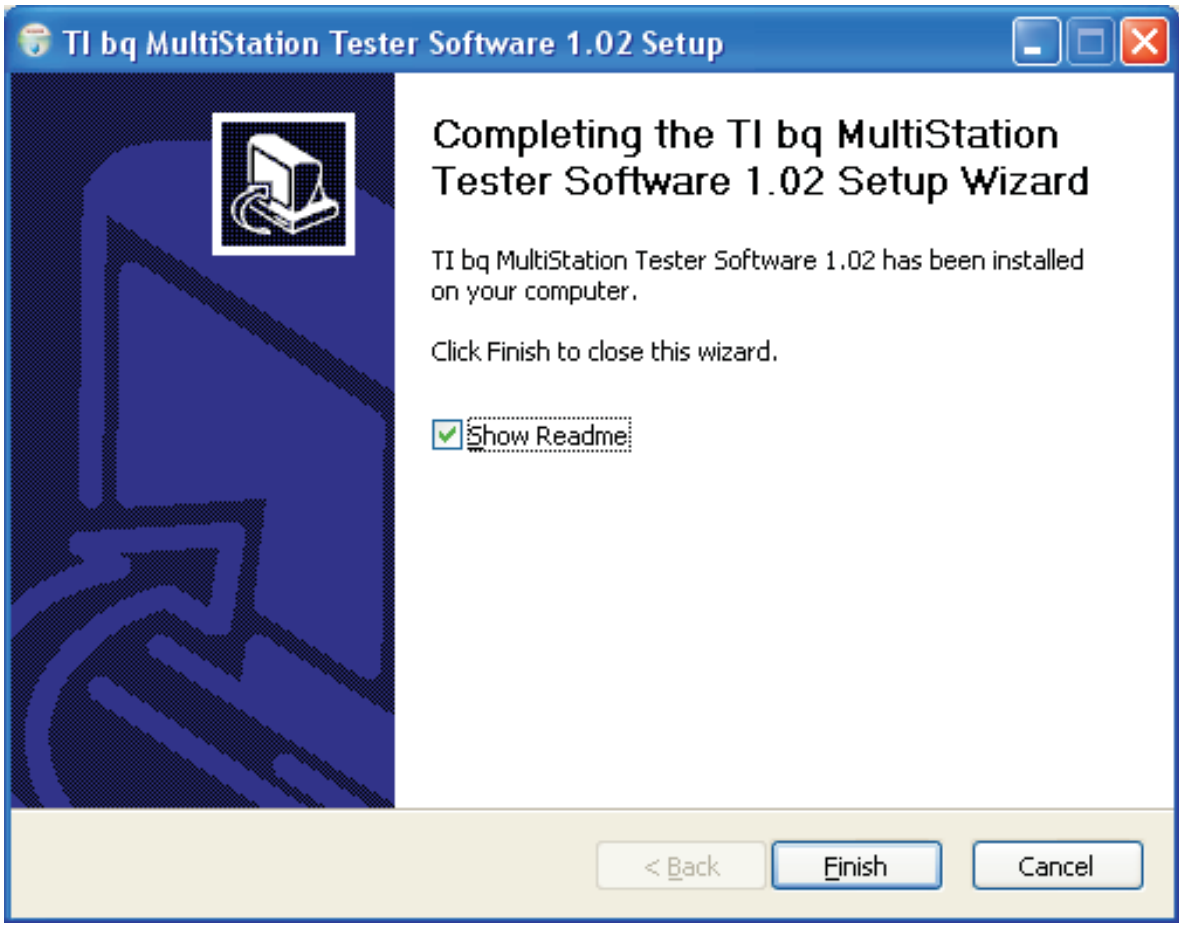
8. Click **Next** at the Choose Components screen since there is only one option for the bqMTester installation



9. Choose the Start Menu Folder where you would like to install the bqMTester associated shortcuts. Texas Instruments is the default destination. Then click **Install**.



10. Select a destination folder where the software will be installed or use the default. Then click **Next** to start the installation.

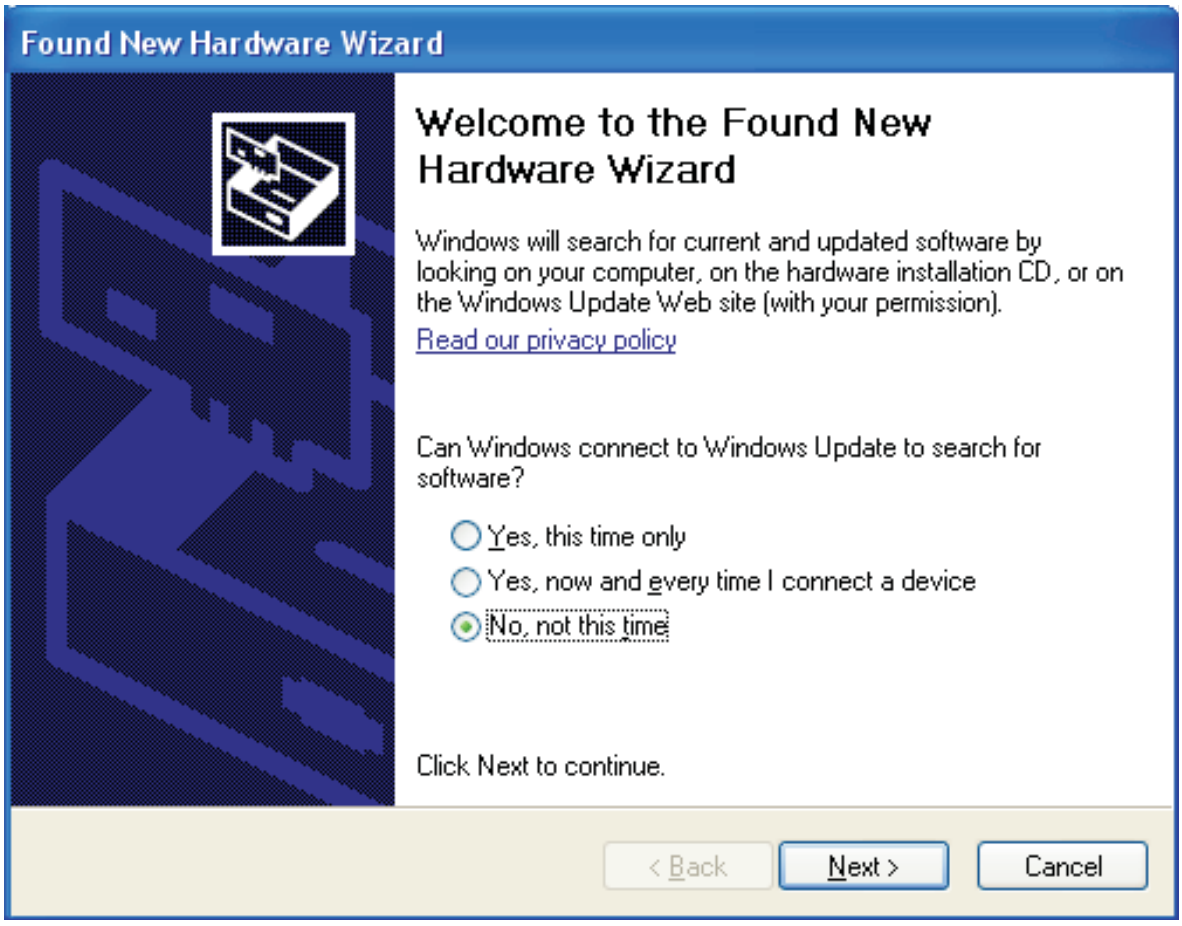


11. If at any time you are asked to reboot, then select **No** and continue.
12. When the software installation is complete click **Finish** to exit the software installation

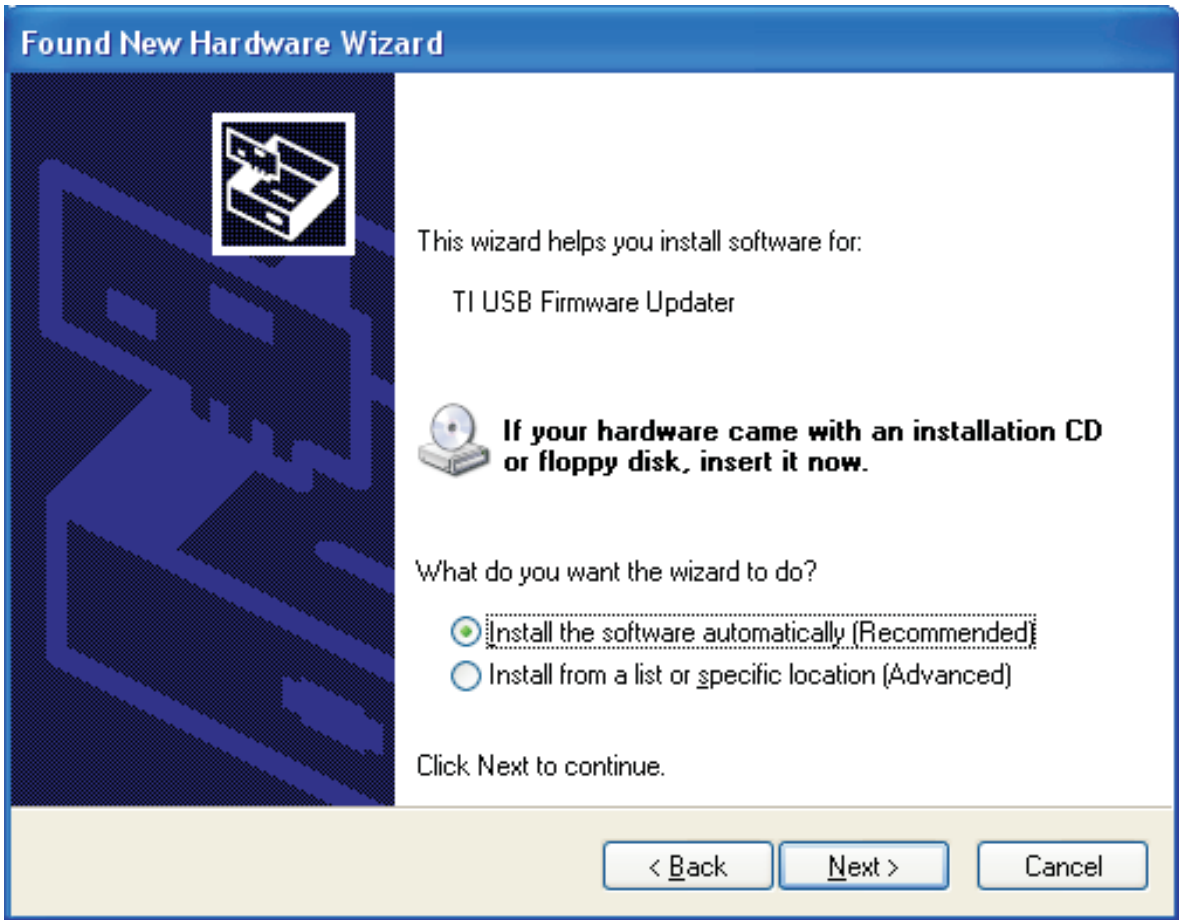
All bqMTester software is now installed on the PC. The EV2300 drivers now have to be associated with the USB ports that will be used with bqMTester software as described in the following section.

EV2300 Driver to USB Port Association

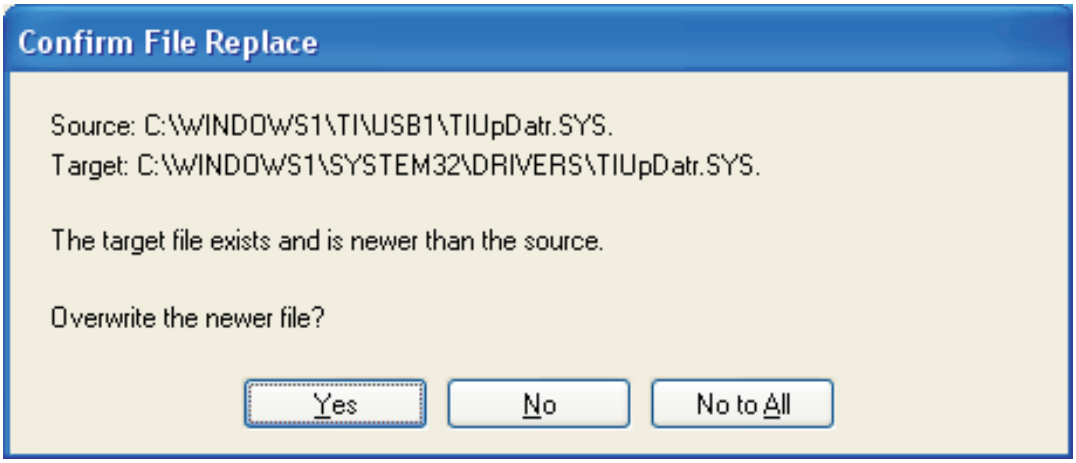
There are 2 drivers associated with the EV2300. An instance of the 2 drivers must be associated with each EV2300 connected to the bqMTester PC through any USB port. In other words, each USB port that has an EV2300 connected to it must have an additional instance of the 2 EV2300 drivers. That means for 12 stations of bqMTester there will be a total of 24 drivers running at the same time. If an EV2300 is connected to the bqMTester PC and the PC detects that it has not had an EV2300 connected to that particular USB port, then the computer will require the following procedure to associate a copy of the drivers for that USB port. To associate an instance of the EV2300 drivers to any given USB port:



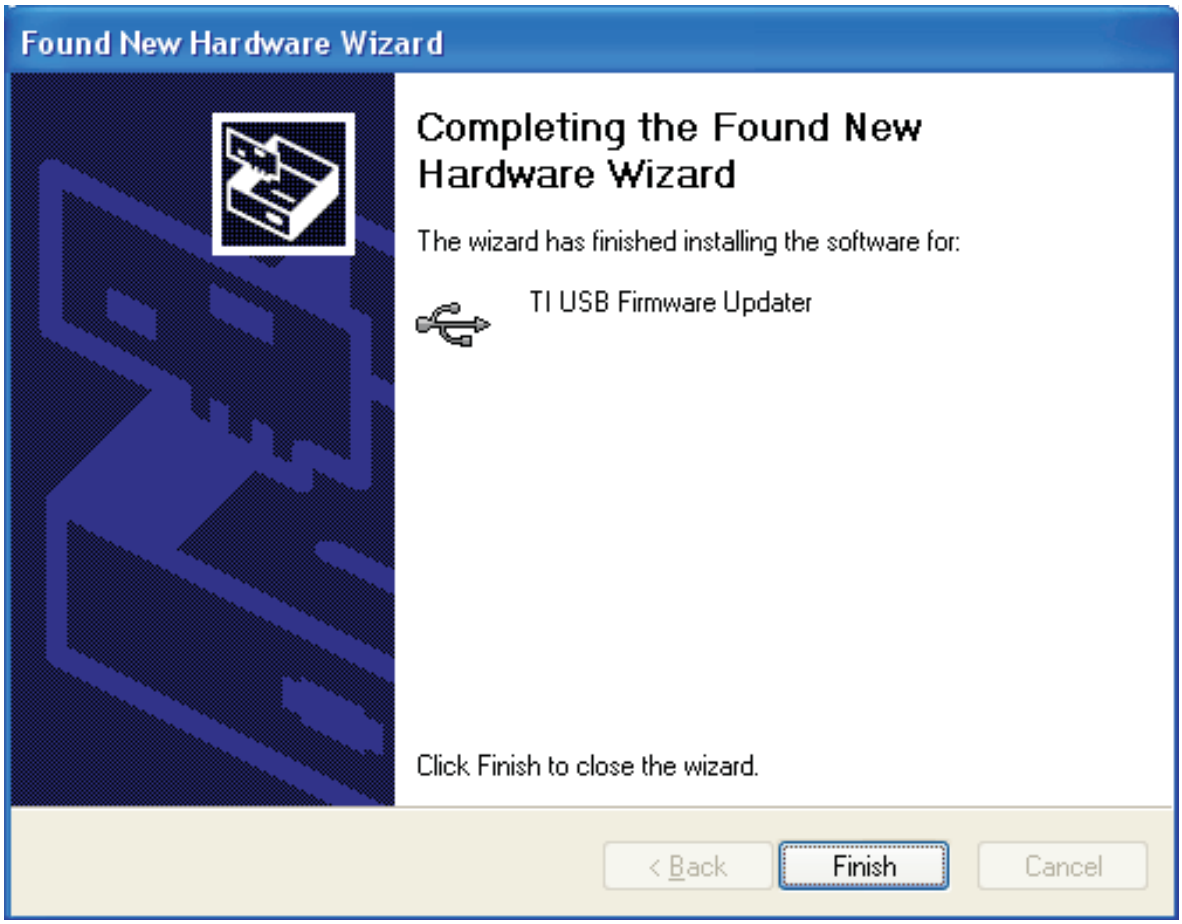
1. Connect an EV2300 to the bqMTester PC. After a few seconds the Found New Hardware screen will appear. Select **No, not at this time** and click **Next**. If the first screen that appears does not look like this screen then proceed to the next step.



2. Select **Install the software automatically (Recommended)** and click **Next** on the next Found New Hardware screen for the first of the 2 drivers (TI USB Firmware Updater) required for this instance of the EV2300.
3. Click **Continue Anyway** on the Windows Logo Testing screen.

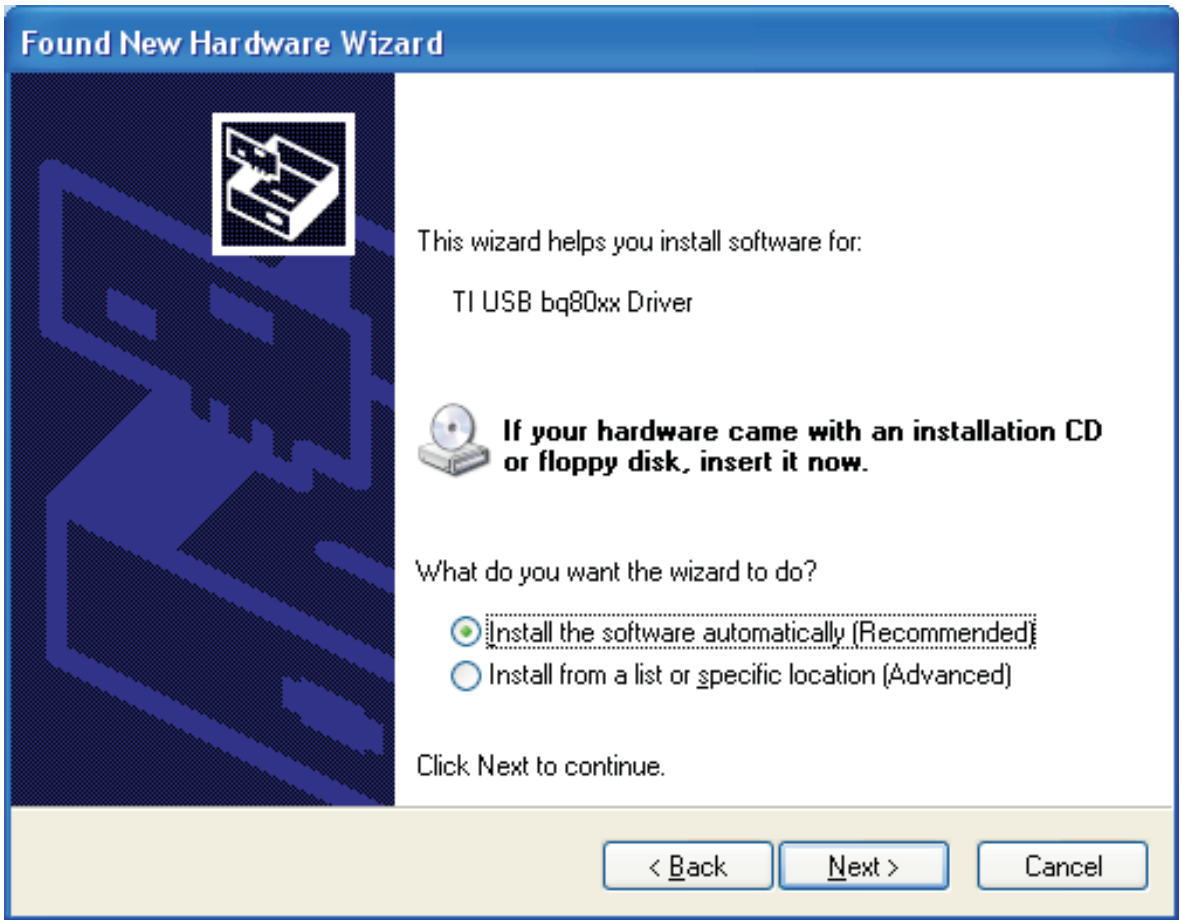


4. It is common for the next screen to be the Confirm File Replace screen. Click **No** to continue. If this screen does not appear then go to the next step.

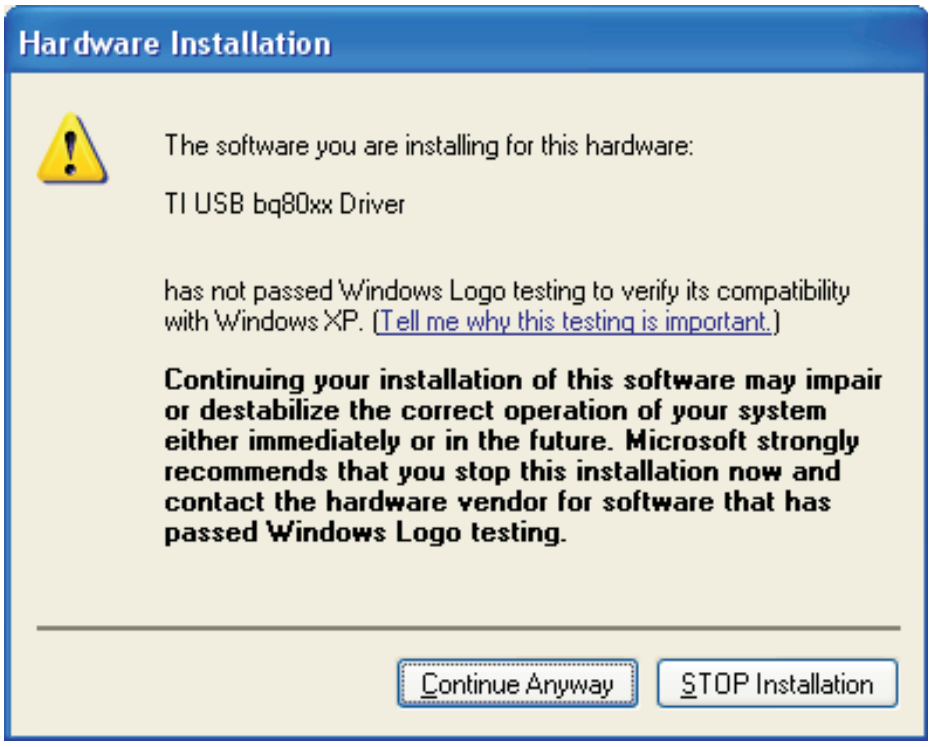


5. The TI USB Firmware Update driver is now installed for this instance of the EV2300. Click **Finish** to exit the driver install wizard.

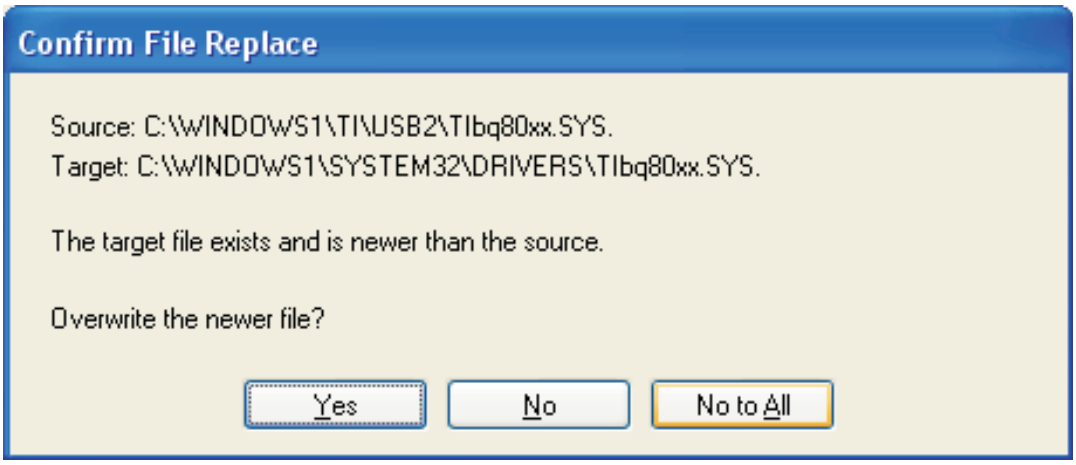
6. After a few seconds another Found New Hardware screen appears to start the installation of the final driver for this instance of the EV2300. Select **No, not at this time** and click **Next**. If the screen that appears does not look like this screen then proceed to the next step.



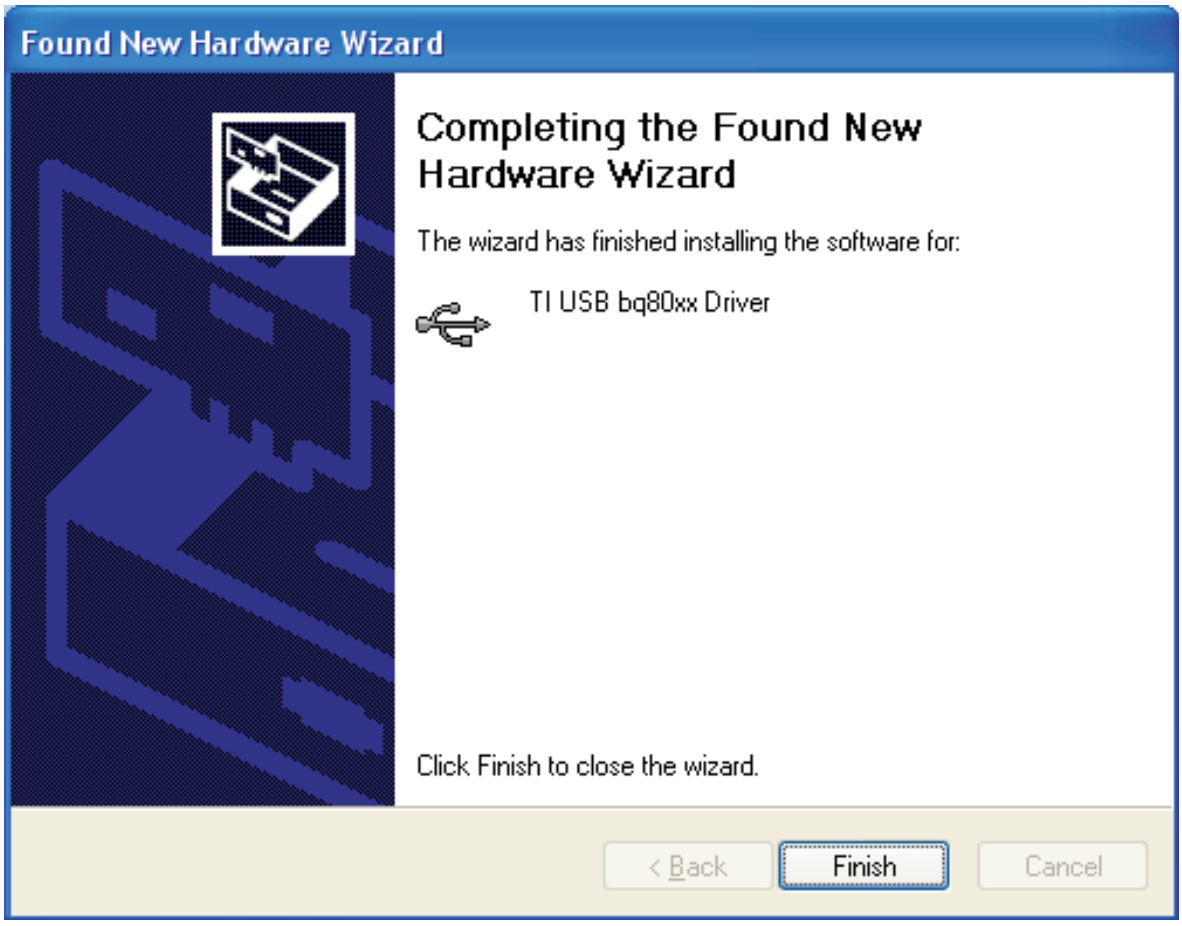
7. Select **Install the software automatically (Recommended)** and click Next on the next Found New Hardware screen for the second of the 2 drivers (TI USB bq80XX Driver) required for this instance of the EV2300.



8. Click **Continue Anyway** on the Windows Logo Testing screen.



9. It is common for the next screen to be the Confirm File Replace screen. Click **No** to continue. If this screen does not appear then go to the next step.



10. The TI bq80XX Driver is now installed for this instance of the EV2300. Click **Finish** to exit the driver install wizard.

At this point the installation of 1 instance of the EV2300 on one USB port is complete. To install more EV2300s to the bqMTester PC then repeat the install process from step 1 above for every instance of EV2300 required to a maximum of 12.

The driver installation process of each instance of EV2300s should only need to be done 1 time. After this the only reason it would be required is if the orientation between USB ports and EV2300s change. This could happen if a USB HUB position is changed, a USB hub is installed, or if an additional EV2300 is installed.

USB hubs can be used to accommodate stations for the bqMTester. It is recommended not to exceed 7 Ev2300/Test Stations per USB hub and that USB hubs not be nested. It is possible stations will not install with nested USB hubs. It is also recommended that the USB hub be USB 2.0 compliant and capable of 1.0A of output current.

26.4 Setup

Creating the "Golden" Image File (mandatory procedure): for bqTester (Single Station Testing) and bqMTester (Multi-Station Testing)

After engineering development has been completed, a *golden* data flash image file must be made from an *Engineering Perfect* module. This *Golden* Image file will be used as a default to program the Static Data Flash constants in all the bq20zXX based smart battery modules using bqMTester during production. It is very important that this process is completed. If it is not then the impedance track algorithm may not function correctly.

This chapter assumes familiarity with Texas Instruments evaluation software for the bq20zXX modules since it was most likely used during the engineering development phase of this project. If it is not familiar then refer to the *bq20z80-001 EVM tool folder* that includes a user guide for the EVM, application notes, and the latest EV software:

http://focus.ti.com/docs/toolsw/folders/print/bq20z80evm-001.html

26.4.154.36 Creating the "Engineering Perfect" Battery Pack: It is assumed at this point that an engineering prototype battery pack is complete and that all static data flash constants have been reviewed and verified for a particular battery pack model. Static data flash is all data flash constants that are not battery pack specific.

Static Data Examples: Static data examples are Charging Voltage, Impedance Track resistance tables, and QMAX settings. Examples of non-static data include serial number, date, and calibration data are all examples of data that is not static.

It is also assumed that this Engineering Perfect battery pack was created using the correct chemistry support SENC file. For more information on this please refer to the Multi-Chemistry Support application note:

Support of Multiple Li-Ion Chemistries w/Impedance Track™ Gas Gauge

This can be found at:
http://focus.ti.com/analog/docs/techdocsabstract.tsp?familyId=412&abstractName=slua372

Now the impedance track data must be verified. This data must be updated and accurate so that all battery packs produced have accurate impedance track tables in data flash *right out of the box*. To ensure that the impedance track tables are optimized, complete the following steps:

1. Using an EV2300 and the EV software appropriate for the device being used in this application (ex: bnq20z70, bq20z80, or bq20z90), ensure that the data flash locations **Qmax Cell 0–Qmax Cell 3**, and **Qmax Pack** have good estimates in them for the battery pack capacity. This information can be derived from the Battery cell manufacturer data sheet. Also note that if more than one cell is connected in parallel then the capacity will increment by one cell capacity for every cell in parallel. For example, if a single-cell data-sheet capacity is 2400mAh, and 3 parallel cells are used, set each value to 2400 × 3 = 7200mAh.
2. Charge the pack to full. If it does not charge then ensure that impedance track is enabled by sending data 0x0021 to SMBus command 0x00 (*Manufacturer Access*).
3. When the pack is full, remove the charger and let the pack relax for 2 hours.
4. Discharge the pack to minimal device acceptable voltage (also set as *Term Voltage* flash constant), at a typical rate for the target application. The exact rate is not critical.
5. Let the pack relax for at least 5 hours
6. Repeat steps 2 through 5 for maximum accuracy.
7. Connect the pack to the EV software, go to the data flash screen, and ensure that **Update Status** is 0x06.
8. The battery pack is now *Engineering Perfect*.

Creating Golden GG File From Engineering Perfect Battery Pack

A GG file needs to be created with all the data from the *Engineering Perfect* battery pack that will be used in creating the *Golden Image* File. The purpose of this GG file is to insure that we get all the non-reserved data saved so that we can install it back into the module after the battery pack is put back into the original state with a new SENC file in the next chapter. We also want to change *usage* data to original values so all production battery packs do not report that they have been used. To make this Golden GG file, do the following:

1. Insure that the *Engineering Perfect* battery pack is still connected to the EV2300 and that the EV software for the applicable device is open.
2. Go to the Data Flash screen in the EV software and click the **Read All** button.
3. Select the *File* pulldown menu, click **Export**, and chose a (*.gg) file name for saving the pre-learned defaults (example: optimized.gg).
4. Open the saved GG file from step 3 in a text editor such as Notepad, and change the value of *Update*

Status from 06 to 02, which indicates that the parameters are learned but the Impedance Track™ feature is disabled (as should be the case for a new pack prior to calibration).

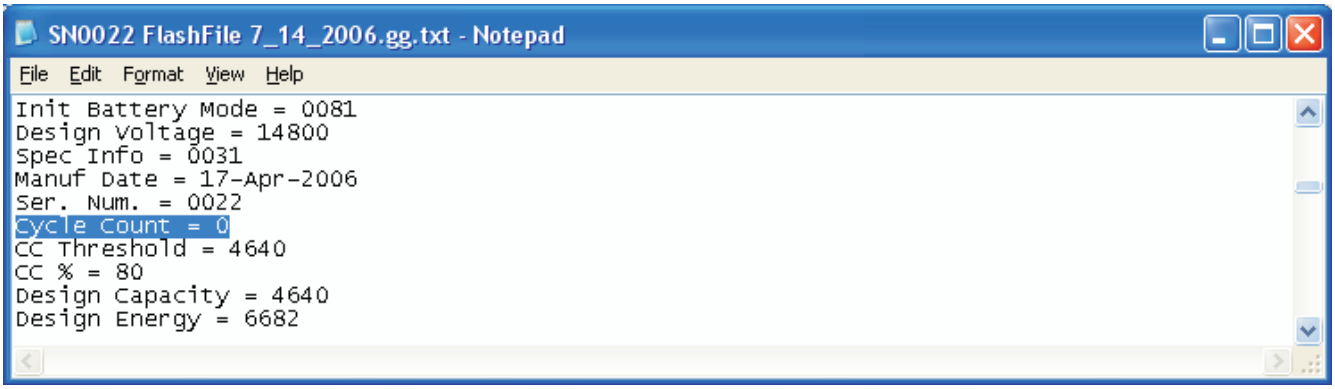


Figure 3. Cycle Count Modification in GG File Using Notepad

5. Also Reset the *Cycle Count* field to *0* as shown in Figure 3.
6. Then save the file. This file will be used below.

Installing the Original SENC File With Correct Chemistry Support

It is assumed that the proper Chemistry Support SENC file has been determined for this application during the Engineering and Development Phase of this project. For most applications (LiCoO2/graphitized carbon chemistry), the default SENC file for the applicable device (ex: bq20z80, bq20z90, or bq20z70) will be used. For more information on multi-chemistry support please refer to the Multi-Chemistry Support application note:

Support of Multiple Li-Ion Chemistries w/Impedance Track(TM) Gas Gauge

The following instructions explain how to install the original chemistry supported SENC file into the *Engineering Perfect* battery pack. Do not worry about losing all the static data from this pack because it was stored in the previous chapter.

1. Go to the product folder for the device being used in this application.
   Some Examples:
   a. For the bq20z70 go to: *bq20z70 Tools and Software Section*
   b. For the bq20z80 go to: *bq20z80 Tools and Software Section*
   c. For the bq20z90 go to: *bq20z90 Tools and Software Section*
2. Click on the Multi-Chemistry Support Software zip file pertaining to the device being used:
   Some Examples:
   a. For the bq20z70 go to:
      bq20z70-V101 Multiple Li-Ion Chemistries Software
   b. For the bq20z80 go to:
      bq20z80-V102 Multiple Li-Ion Chemistries Software
   c. For the bq20z90 go to:
      bq20z90-V102 Multiple Li-Ion Chemistries Software
3. Download the applicable zip file and extract to a temporary directory. An example would be C:\Temp\sluc058.zip
4. Insure that the *Engineering Perfect* battery pack is still connected to the EV2300 and that the EV software for the applicable device is open. Then go to the Pro screen in the EV software.

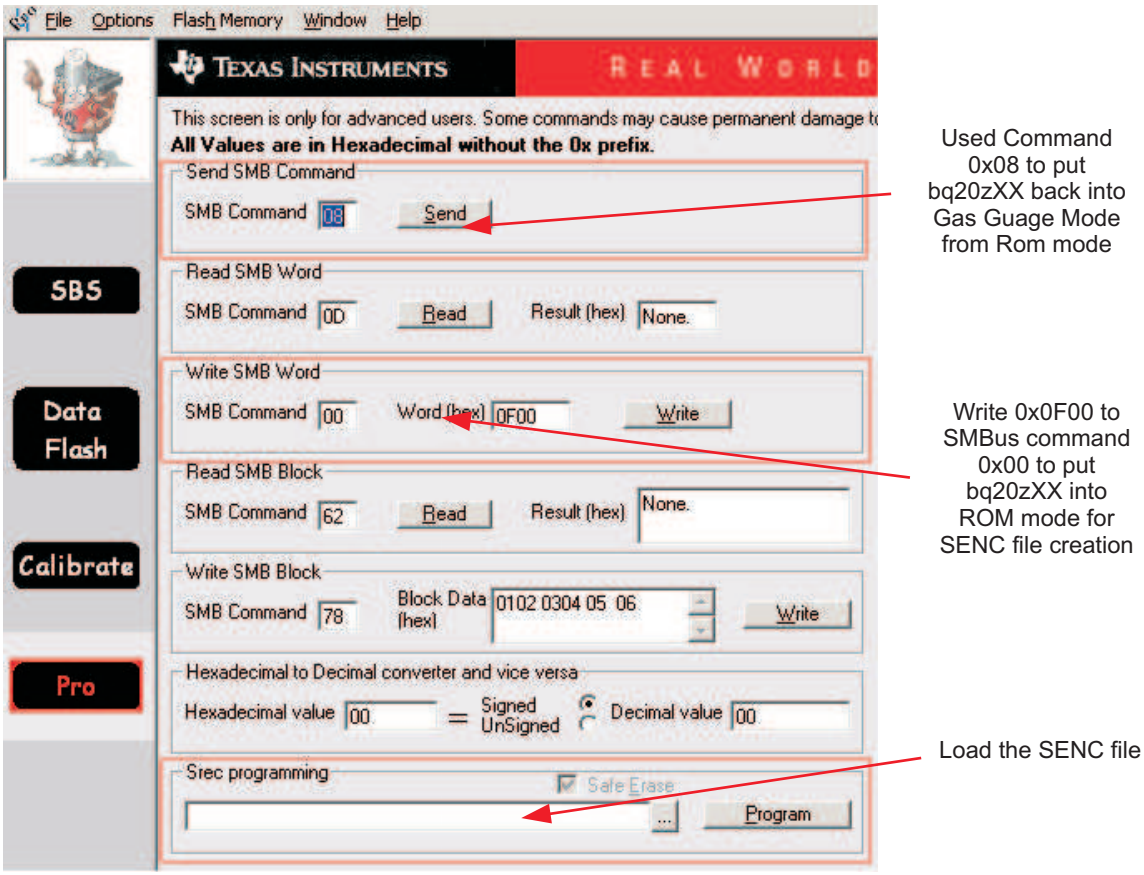


Figure 4. EV Software Pro Screen

5. Ensure that *Write SMB Word* frame has the SMBus Command set to 0x00 and the SMBus Word set to 0x0F00. If they are not then change them.
6. Then click Write. This puts the bq20zXX module into ROM mode to prepare for writing the SENC file created in the section above.
7. Write the SENC file to the *Engineering Perfect* pack by clicking the browse (...) button in the *Srec programming* frame.
8. In the file manager that pops up, locate and select the previously saved SENC file created previously in the above section.
9. Then click the **Program** button. The software will indicate when finished.
10. After it finishes writing then ensure that the **SMB Command** is 0x08 in the *Send SMB Command* frame. If it is not then change it to 0x08.
11. Then Click the **Send** button. This puts the bq20zXX back into Gas Gauge mode. Your factory default SENC file is now loaded.

Creating the Golden Image File

The final step in this process is creating the *Golden* Image file. This file will include all the static data in the data flash that is constant from one smart battery module to the next. It also has all the reserved data and *usage* data set to default states to insure that all production packs start out in a new state. This process is mandatory for new designs and is required for using both single station testing (bqTester.exe) and for Multi-Station Testing (MultiStationTester.exe). Without this process the Impedance Track Algorithm may not function properly. Follow these steps to create this file:

1. Insure that the *Engineering Perfect* battery pack is still connected to the EV2300 and that the EV software for the applicable device is open. Then go to the Data Flash screen and open the *File* pulldown menu and select **Import**.

2. Then in the file manager that pops up, locate and select the Golden GG file created in the above section and click the **Write All** button.
3. The *Engineering Perfect* battery pack now has all *Golden* data in it. The next step is to retrieve that data into a *Golden* image file.
4. Run the Data Flash reading software in the bqMTester suite by double clicking the TesterDFReader.exe file in the directory where the software was installed.

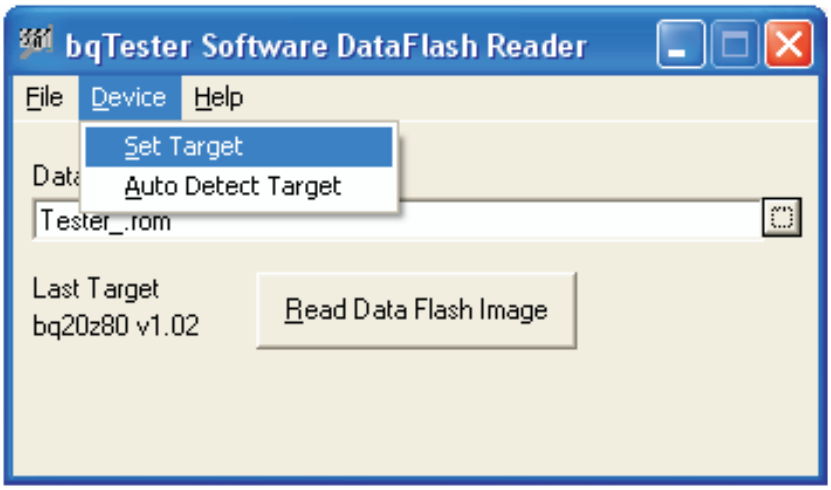


Figure 5. TesterDFReader.exe Software

5. Select the device type of device being read from the *Device* pulldown menu.
6. Type in a complete path and file name with a .rom extension in the dialog box or click the browse button ( ).
7. Click the *Read Data Flash Image* button. This will cause the software to read the data flash information from the bq20zXX based smart battery module and store it in this file.

This .rom file is now the *golden* data flash image file which will be used to program all other similar bq20zXX based smart battery modules in the production process.

Need to add description of Seal Pack check box. GTG 11-22-05

26.5 Multi-Station Testing (MultiStationTester.exe): Individual Station Interface Connections

bqMTester requires that the latest version of the EV2300 USB-Based PC Interface Board for Battery Fuel Gauge Evaluation interface from Texas Instruments be installed and running properly.

The HPA169 calibration board should be connected as shown in Figure 6. All four pins (Vout, SDA, SCL, and GND) on the I2C connector of the EV2300 should be connected to the calibration board I2C connector. The SMBus connector of the EV2300 should have the SMBD, SMBC, and GND connected between the EV2300 and the module under test.

It is VERY important that the 2 ground connections connected to 1N of the module under test be connected as close to the module as possible. This connection is very critical to ensure accurate voltage calibration.

Connect an isolated 5V/4A wall brick power supply to the bottom power connector and an isolated 24V/0.5A wall brick power supply to the top power connector. It is VERY important that these power supplies be ground isolated. There should be no ground plug on the wall connection. Our recommended part numbers for these supplies are:

24 volt supply: CUI Inc model no. EUA-101W-24

5 volt supply: CUI Inc model no. EPA-201DA-05

The Jumpers in Figure 6 are setup for a 4 cell module test. To Test 3 cells, first remove all jumpers. Then install a jumper at J7 labeled *1, 2, or 3 Cell* and another jumper at *3 Cell*. For a 2 cell application, remove all jumpers and then install a jumper at *1 or 2 Cell* and another jumper at *2 Cell*. While the HPA169 Calibration board includes an on board temperature sensor, it is recommended that you use external temperature sensors for the most accurate temperature calibration. For using an external temperature sensor use the TI TMP100 and connect per Figure 7. The Software will distinguish between the on board temperature sensor and any external temperature sensor because the on board sensor has I2C address 0x94 while the external temperature sensor is I2C address 0x90.

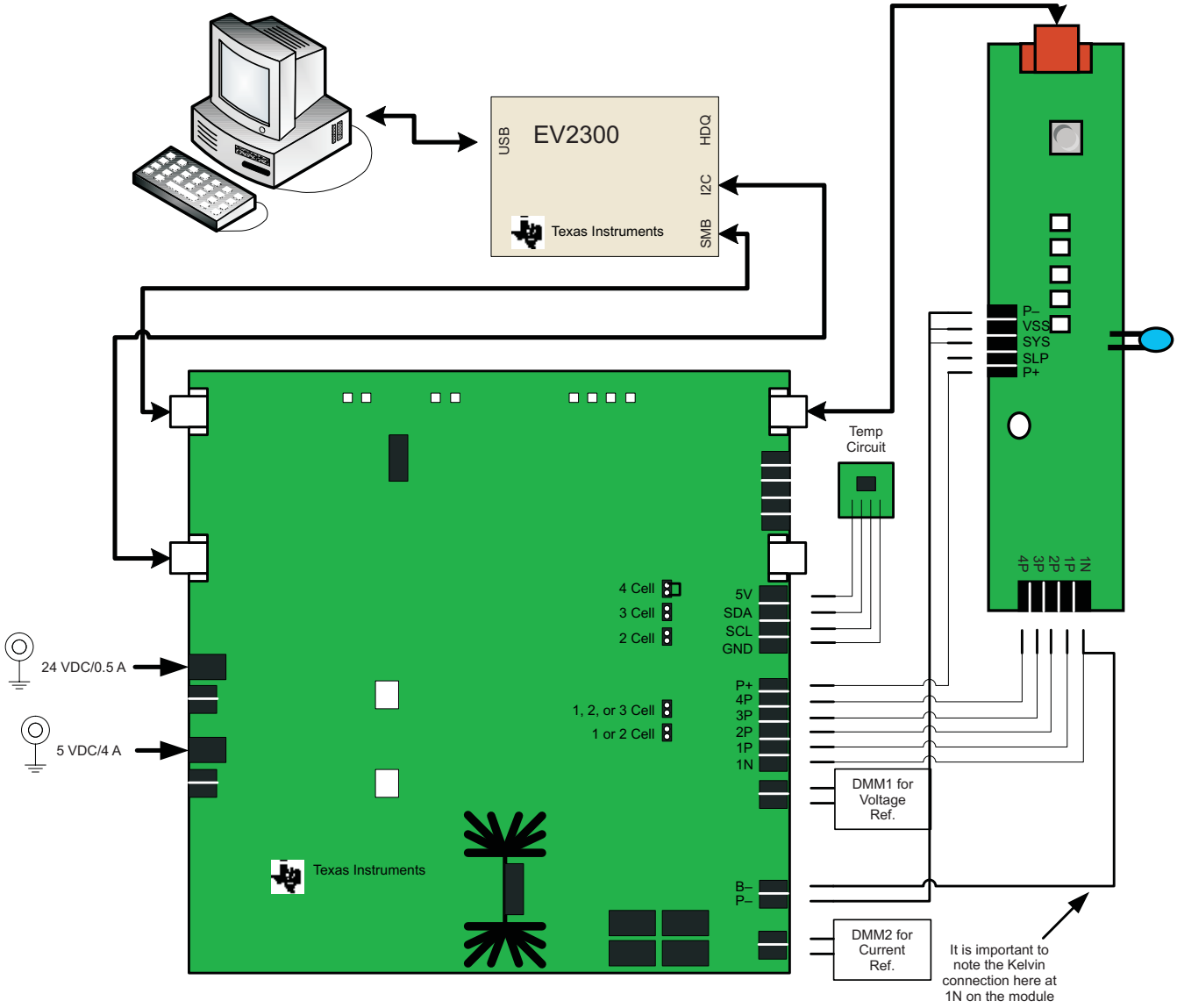


Figure 6. One Testing Station: EV2300/HPA169 Cal Board/Smart Battery Module Connections

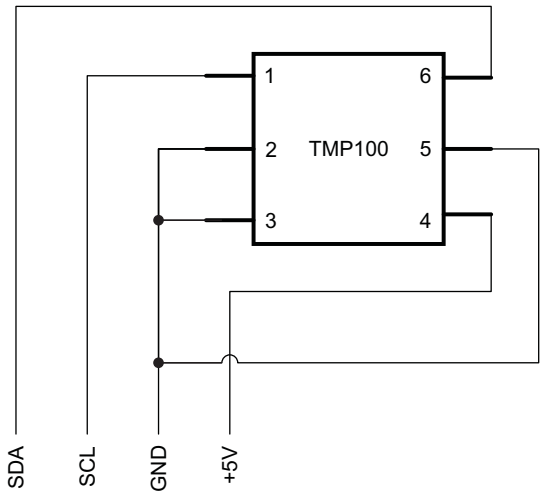


Figure 7. External Temperature Sensor Connection

26.6 Multiple Station Setup

When setting up for the first time or adding testing stations to the PC, run the StationSetup.exe program to identify and setup the configurations for all the test stations connected to the PC. Follow these steps to prepare all stations:

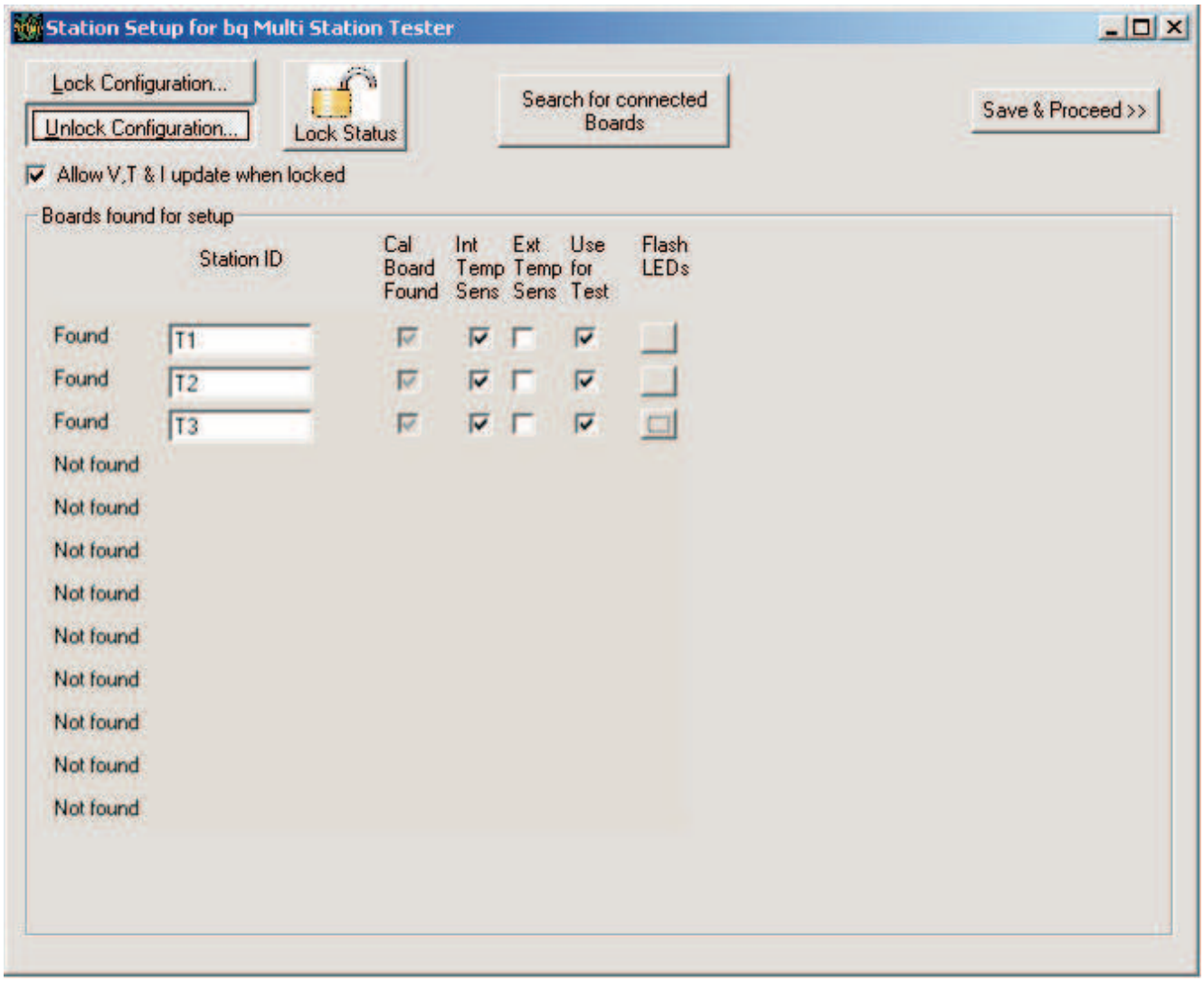


Figure 8. Station Setup Program

1. Connect all the stations to the PC. Up to 12 stations are supported. An 8 station configuration is shown in Figure 9.
2. Unlock the Station Setup program by clicking the *Unlock Configuration* button. You will be prompted to input a password. The default password is *bq20z80* without the quotes. Click **OK** next to the password input field after typing the password. When relocking the software you will be prompted to change the password.
3. Click the *Search for Connected Boards* button so the software can detect all the stations you have connected to the PC. The software will detect and display all stations connected to the PC. If a textbox appears with a message saying *Detected EV2300* with an old firmware version. Update the EV2300 to version 3.1k or later. If required, contact TI for assistance.
4. Type a unique text name in the *Station ID* field to help identify each station with a simple name.
5. Select which stations will have their internal or external temperature sensors available for use for calibration with the *Int Temp Sens* or *Ext Temp Sens* check boxes. If neither internal nor external are selected then that station will be required to either use a temperature probe from another station or manual input of the temperature.
6. Select the *Use for Test* checkbox to enable a station for use during testing. If the “Use for Test” is de-selected then that station will be disabled and will not perform testing. A disabled station’s temperature probe will be available to other stations however if it is selected from step 5 above.

7. Clicking the “Flash LED” button for each station will cause the corresponding calibration board to flash its LEDs and enable the current and voltage power supplies. This is useful for testing the power supplies and for identifying the corresponding hardware for each station.
8. Click the **Save and Proceed** button.

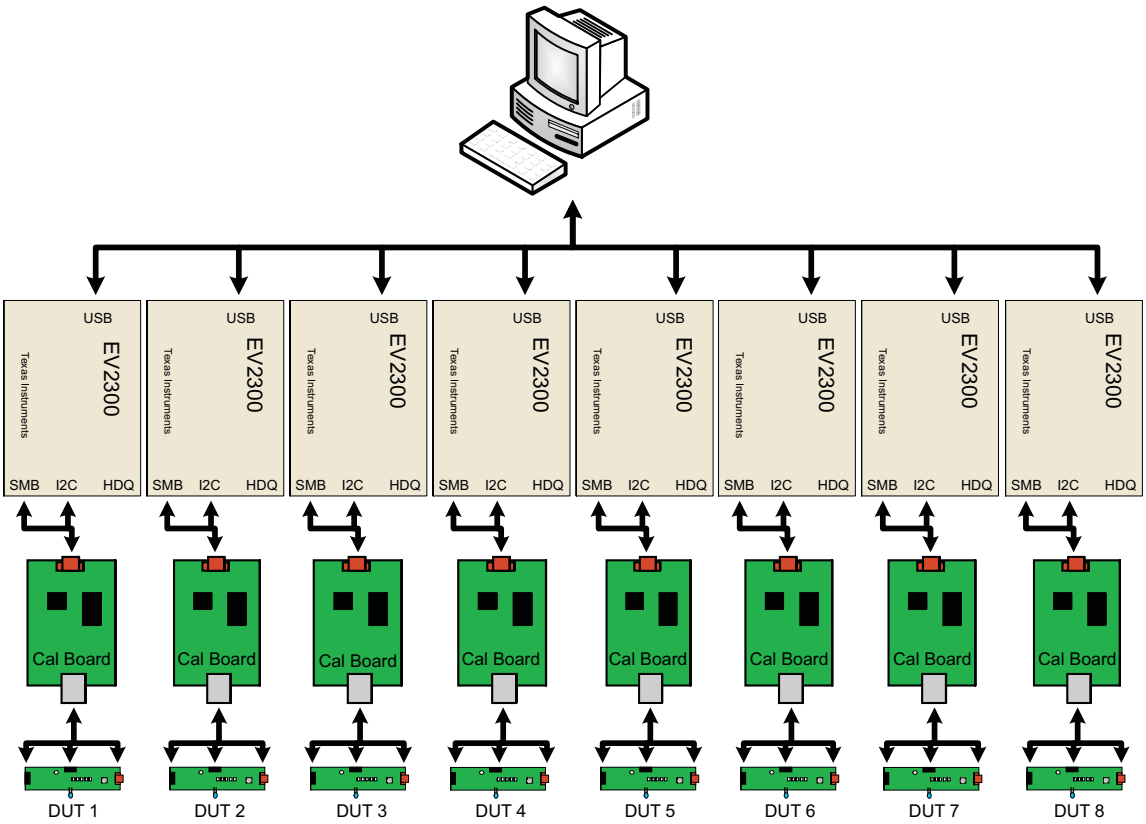


Figure 9. Multi-Station Setup

Temperature Probe Selection

Clicking the **Save and Proceed** button brings up the Temperature Probe Selection window. This window is used to configure the temperature probes. For each station there is the option of selecting either:

1. *No Tracking – Use entered value*
2. 2. The temperature probe measurements from any of the stations that had their temperature probes enabled from the *Use for Test* checkbox selection on the first screen.

For example: If only one temperature probe is required for all channels and it is to be an external temperature sensor and not the one installed on the calibration board for a station named *Station1* then the user would do the following:

1. Start the StationSetup.exe program.
2. Unlock and click the *Search for boards* button.
3. Name all stations using a unique Station ID but name one station *Station1* so that it can be referenced in the next couple of steps
4. Select *Ext. Temp Sense* checkbox for *Station 1*. All other stations select *Int Temp Sense*.
5. Select *Use for Test* checkbox for *Station 1* and all other stations.
6. Click *Save and Proceed*.
7. On the Temperature Probe Selection screen select *External Probe: Station1* for all the stations available in the list.
8. Click Next.

9. Configure global screen as described in section chapter 8

Now all stations will use the probe connected to the External Temperature Probe Terminal Block for the station named *Station1*.

Global Configuration Window

Clicking the *Next* button from the Temperature Probe Selection window brings up the Global Configuration window as shown in Figure 10. Here, all data that is *Global* to all stations connected to the PC can be configured. In this window, all numeric values are specified in signed decimal except for the serial number field which is unsigned with a max value of 65535.

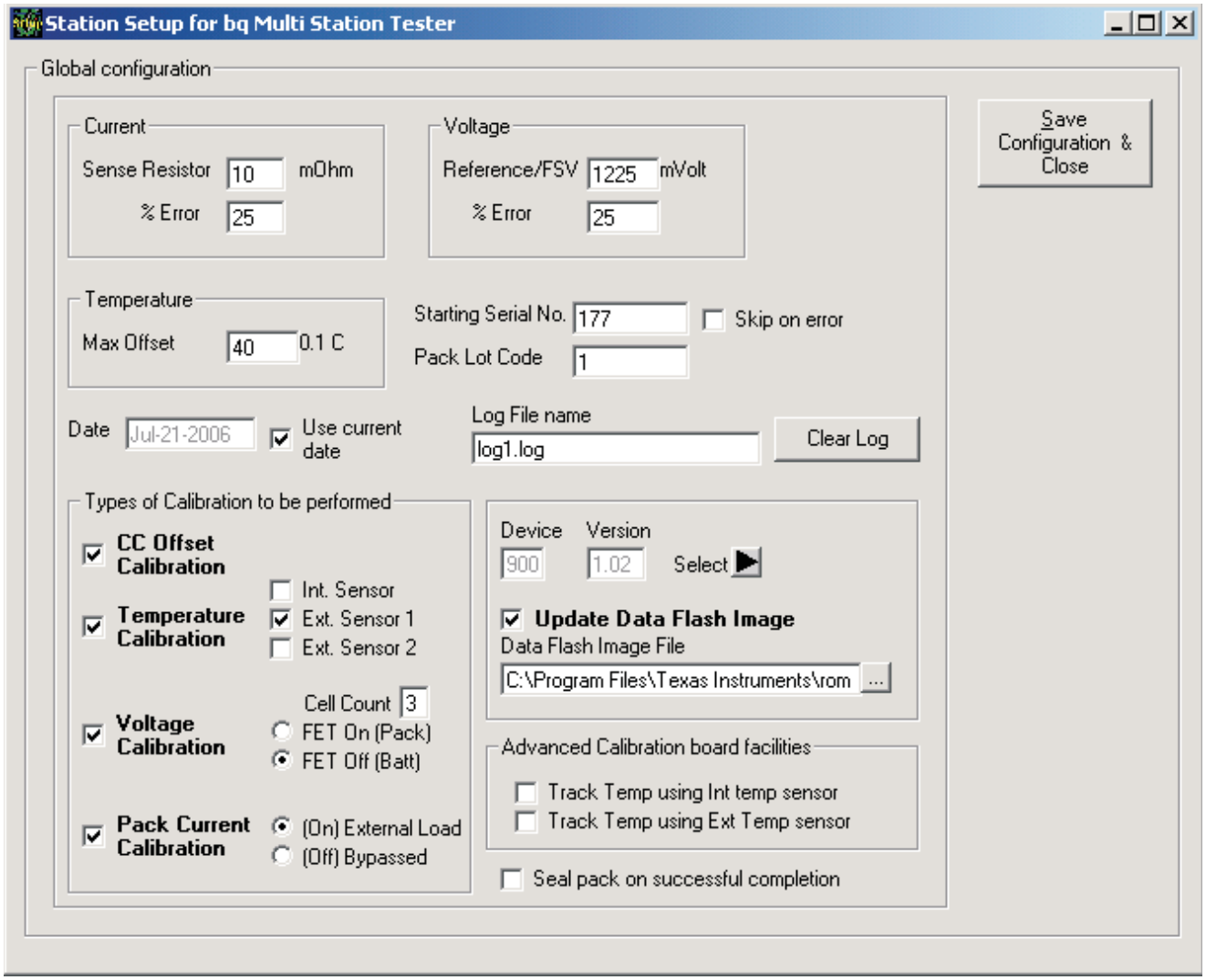


Figure 10. Global Configuration Screen

26.6.159.37 CC Offset Calibration This is the coulomb counter offset. There are no user definable values in this box. This calibration can be selected by placing a check in its selection box or deselected by removing the check. The default is checked. Note: if this test is disabled, the values from the *gold* data flash file will be used and not the values currently in the part.

26.6.159.38 Voltage Calibration Voltage calibration can be selected by placing a check in its selection box or deselected by removing the check. The default is checked. The voltage calibration area also has a box for the user to enter the number of series cells being simulated. The default number of cells is 4. It also has a FET Control selection area. *Off (Batt)* should be selected. *On (Pack)* should never be selected and is included only for possible future use. Note: if this test is disabled, the values from the *gold* data flash file will be used and not the values currently in the part.

26.6.159.39 Temperature Calibration Temperature calibration can be selected by placing a check in its selection box or deselected by removing the check. The default is checked. The temperature calibration area also offers three different temperature probe selections. The proper selections should be made depending on the application. Note: if this test is disabled, the values from the *gold* data flash file will be used and not the values currently in the part.

26.6.159.40 Pack Current Calibration Pack current calibration can be selected by placing a check in its selection box or deselected by removing the check. The default is checked. The pack current calibration area also allows FET control selection. *On (External Load)* should always be selected (this configuration is the default). *Off (Bypassed)* should never be selected and is only included for possible future use. Note: if this test is disabled, the values from the *gold* data flash file will be used and not the values currently in the part.

26.6.159.41 Current Frame This frame contains two values:

1. **Sense Resistor:** Enter the value of the sense resistor used in the bq20zXX based smart battery pack in the *Sense Resistor* field. This value is entered in units of milliohms
2. **% Error:** Enter the desired acceptable percent error that the sense resistor can differ from the value listed in the *Sense Resistor* field in the *% Error* field. Note: the default value for this field is 25%. The value of 25% may seem like a large number but this value is not related to the calibration accuracy that the bqMTester calibrates to. That calibration is highly accurate. This *% Error* field is used as a rough test to make sure the sense resistor is mounted correctly and not shorted. After the bqMtester calibrates the Sense Resister gain value then it compares the new calibration value to what is in the *Sense Resistor* field. If the percent difference between the 2 values is more than 25% then it fails the calibration because it assumes something must be grossly wrong to get a value more than 25% from the nominal *Sense Resistor Value* This value must be specified as a positive integer value.

26.6.159.42 Voltage Frame This frame contains two values:

1. **Reference/FSV:** The tester calibrates the voltage gain by manipulating the Full Scale Voltage Reference. Do not change the values in this field.
2. **% Error:** The *% Error* field is used as a rough test to check the Voltage Measurement Circuitry. After the bqMtester calibrates the bq20zXX voltage gain then it compares the new calibration value to what is in the *Reference/FSV* field. If the percent difference between the 2 values is more than 25% then it fails the calibration because it assumes something must be grossly wrong to get a value more than 25% from the nominal.

26.6.159.43 Temperature Frame This frame contains one value. Enter the maximum absolute value of offset that the bqMTester Software will be allowed to put into any of the data flash temperature offset registers for the module being tested. This is not an accuracy verify. This is a gross Error detection. The default value of this field is 40 meaning that the calibrated offset put in the data flash cannot exceed positive or negative 4°C. For internal Temperature Sensor calibration it is recommended to increase this value because internal temperature sensor offset accuracy commonly will exceed 4°.

26.6.159.44 Starting Serial Number Enter the value for the serial number of the first bq20zXX based smart battery module to be tested. This number will be incremented by one as each new module is tested. If the *Skip On Error* check box is checked, the number will not be incremented in the case of a module that fails the test. The default for this box is 1. This value must be specified as a positive integer value.

26.6.159.45 Date Enter the value for the desired date to be programmed into the bq20zXX based smart battery module. If the *Use Current Date* check box is checked, the system date from the PC running the bqMTester software will be used

26.6.159.46 Log File Name Enter the complete path and file name to be used for the log file. This file will contain all relevant test data for each bq20zXX based smart battery module tested. If the *Clear Log* button is pressed, the log file contents will be deleted.

26.6.159.47 Pack Lot Code Enter the value for the Lot Code of the group of bq20zXX based smart battery modules currently being tested. This number will not change until it is changed manually and will be programmed into each bq20zXX based smart battery module tested. This value must be specified as a positive integer value.

26.6.159.48 Save Clicking the *Save Configuration and Proceed* button will cause the current configuration settings to be saved.

26.6.159.49 Data Flash Image File Input the location of the data flash Golden file that will be stored in all parts that will be tested when running the bqMTester.exe program. Clicking the browse () button will give the option to browse for the Golden image file. If the *Update Data Flash Image* checkbox is not checked then no data flash image will be installed in any parts. It is always recommended that an Image file be used.

26.6.159.50 Device and Version The correct Device and Version must be selected using the select () button. Once the select button is pressed, select the proper device and firmware version of the modules to be tested form the dialog box that appears. If the device or version desired is not available, check the Texas Instruments web site for an updated version of the bqMTester software in the bqMtester Tool Folder on the www.ti.com web site. The Tool Folder is located at:

http://focus.ti.com/docs/toolsw/folders/print/bqmtester.html

Advanced Information: For special/custom parts, it is possible that the part can be added to the file that holds all allowed parts compatible with bqMTester. Using this option is sometimes tricky. It is recommended that TI be contacted before using this option to ensure that the bqMTester has been tested with the requested device. The file to be edited is called *Targets* and is located in the directory that bqMTester was installed.

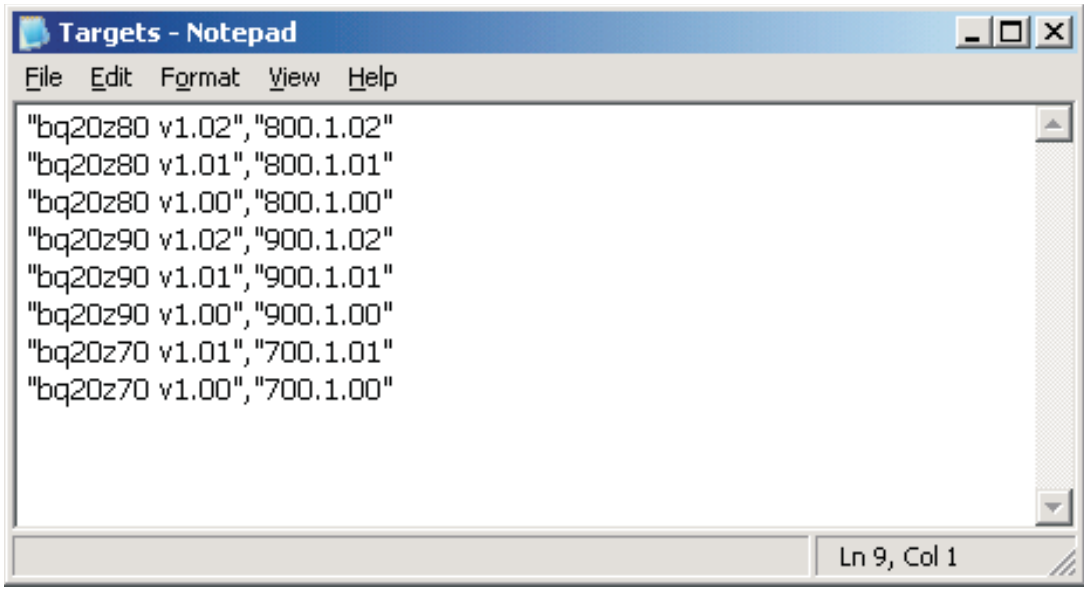


Figure 11. Example Targets File

When using this option please verify very carefully some modules tested and calibrated with bqMTester software for accuracy and DF compatibility prior to doing production testing to ensure the bqMTester is compatible with the custom device.

26.6.159.51 Advanced Calibration Board Facilities There are 2 checkboxes in this frame. Both should remain unchecked when using the Multi-site tester software. If these checkboxes are selected then they will override all selections made in the Temperature Probe Selection window. With either of these selected, every station will use its own Temperature Probe depending on whether Internal or External is selected.

26.6.159.52 Seal Pack on Successful Completion If checked then the pack will be sealed upon completion of the test.

26.7 MultiStation Testing

Preparing the Test Software

To start testing modules, run the MultiStationTester.exe file. This will bring up the main Multi-Station Tester window. This window keeps track of all tests being done at each station, then logs and displays the information from the stations that were initialized and setup in section 3 of this document.

When the software opens, the *Start* button will be disabled by default until the voltage, current and temperature of all the references are verified by clicking on the *Configure VTI* button. The purpose of this is to secure the configuration via engineering approval prior to testing modules and as a reminder to ensure that the reference data is accurate before allowing testing.

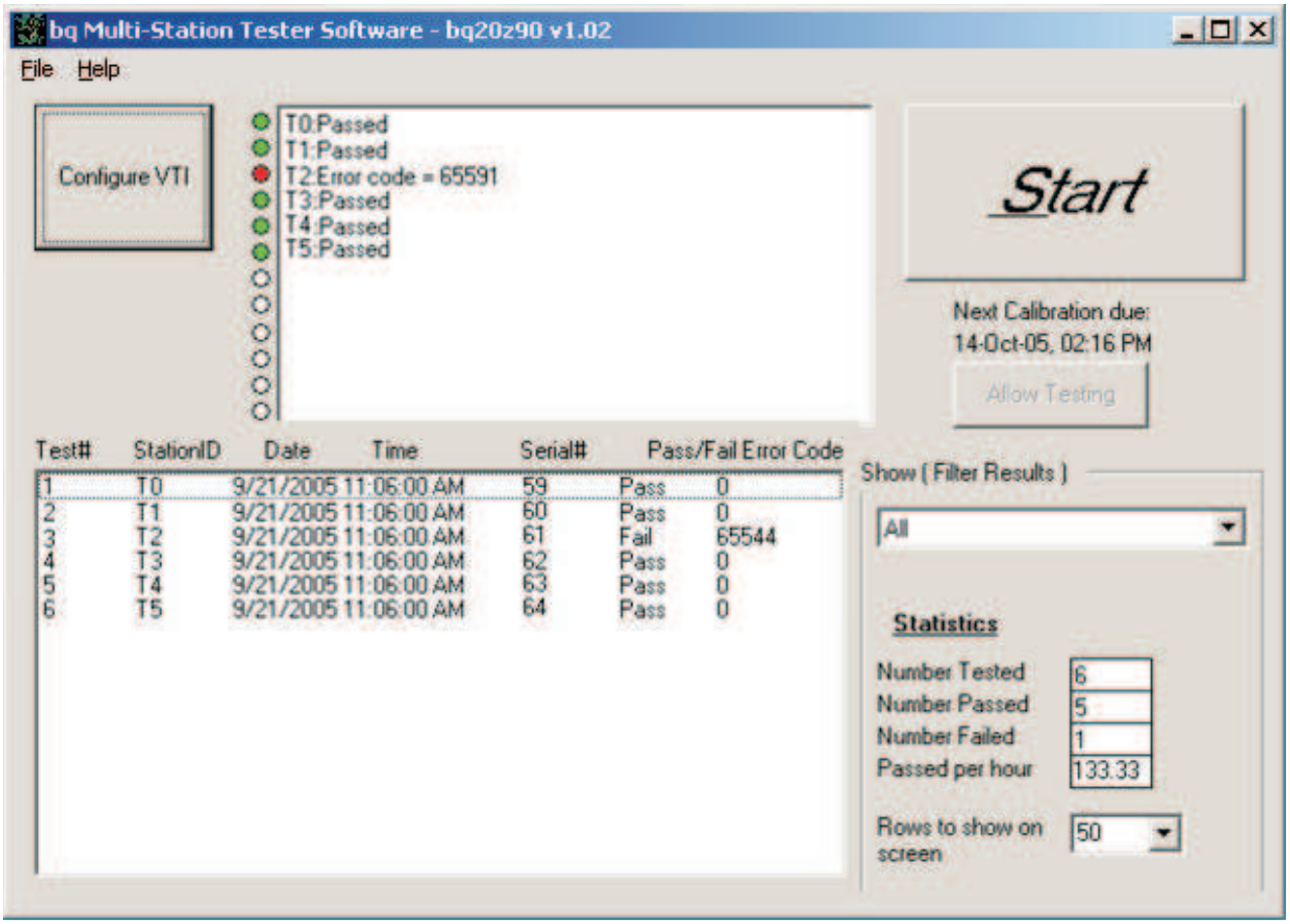


Figure 12. MultiStation Tester Window

26.7.160.53 Verifying V, T, I Configuration First, click on the *Configure VT*, Button. The *Update VTI* window will pop up as shown in Figure 13. If *Allow V, T, I while locked* is not selected then the *Unlock Configuration* button must be pressed to allow voltage, temperature, and current reference adjustment.

26.7.160.54 Reference Adjustments Once unlocked, the references can be adjusted as required. When any field is clicked on in a particular station row then the LEDs for that station will start flashing, and the voltage and current power sources will power up. Clicking the **Read Currently Calibrated Temperatures** button will display the temperatures read from temperature probes associated with each station.

To calibrate the references, use the following process.

1. Measure the voltage for the first station by connecting a traceable DMM to the *Reference V Meter* + and *Reference V Meter* – connections as shown in Figure 6 (shown as DMM1 in Figure 6) to measure the actual voltage of the cell simulation voltage supplied by the calibration board for the first station. Input this voltage in the voltage column for the first station. Repeat this step for each remaining station.
2. Setup the DMM for current measuring and connect the DMM to *Reference I Meter* + and *Reference I Meter* – as shown in Figure 6 (shown as DMM2 in Figure 6) for the first station being setup. Be sure and disconnect the wire that shorted these 2 connections so that current will flow through the meter. Input the current measured in the current column for this station. Repeat this step for each remaining station. Re-install the short from the *Reference I Meter* + to the *Reference I Meter* –.
3. Place the traceable temperature probe next to the temperature probe being used on the calibration board at the first station with a temperature probe being used for testing. Click the *Read the Currently Calibrated Temperatures* button. Compare the temperature from the traceable temperature probe to the calibration board temperature displayed. If the temperatures are different then type in the temperature from the traceable temperature probe into the corresponding temperature field. Type over the value displayed when the *Update VTI* button was pressed. Repeat this step for each station that has a temperature probe.

26.7.160.55 "Allow V, T, I While Locked" Selection If the software is unlocked then the *Allow V, T, I while locked* checkbox will be enabled. Otherwise it will be dimmed (disabled). If selected, the user will be able to adjust the actual values for voltage, temperature, and current references even though the configuration has been locked. If not selected, the user will be unable to alter these values without unlocking the configuration.

26.7.160.56 Locking and Unlocking the Configuration Once all information is updated as required then click *Update V, T, and I and Close*. This will lock the software and enable the *Start* button.

To unlock the software at any time, click the *Configure VTI* button on the main screen and then click the *Unlock Configuration* button. A password dialog window will be displayed. Supply the required password and click *OK*. The default password is *bq20z80*. This password should be changed after first use.

To change the password, click the *Lock Configuration* button. This will cause a password dialog window to appear. Enter a password and be sure to record it in a safe location for future reference. Re-enter the password to ensure it was not misspelled. Click on *OK*.

The software will always lock when the *Update VTI and Close* button is clicked. When either the *Update VTI and Close* button or the *Lock Configuration* buttons are pressed, notice that the *Lock Status* icon changes from an open lock to a closed lock.

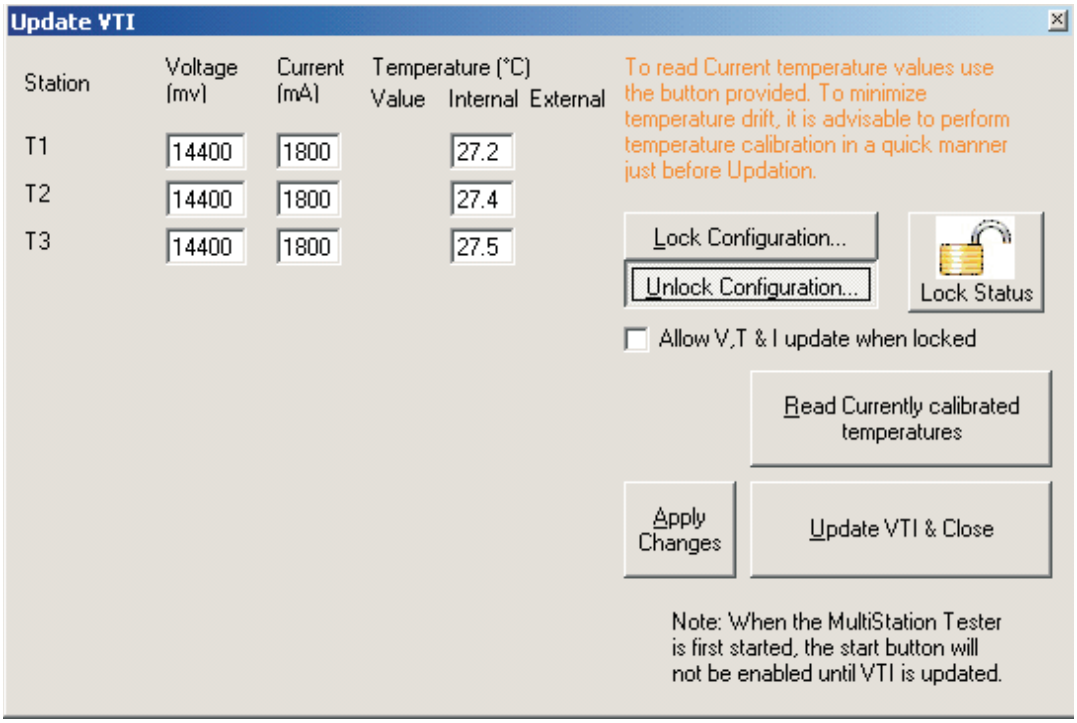


Figure 13. Update VTI Window

Testing Modules

Once setup is completed testing can begin. There are multiple indicators on the main screen of the Multi-site tester program and the *Start* button

26.7.161.57 Progress Text Box The software displays a description of the progress of the test for each station in the text box in the upper center of the main window (see Figure 12). Only stations enabled will be displayed in this window. Next to the Progress Text Box is a column of simulated LEDs adjacent to each station progress entry. After a test finishes, this simulated LED will turn red or green depending on a pass or fail.

The progress steps are:

1. **Verifying Device Version:** Powering up device, waiting for parameters to settle, and verifying the version of firmware to be tested.
2. **Writing Data Image:** Writing the *Golden* image file to the Data Flash of the device under test.
3. **Calibrating:** Calibrating voltage, temperature, and current.
4. **Verifying Calibration Limits:** Verify that the calibrated gain and offset values did not go out of the ranges selected in the Tester Setup program.
5. **Pass or Error Code = XXXXX:** If the test failed then an error code is reported. The error code displayed with a failed part in the Progress Text Box will be a more detailed code than the error code reported in the Statistics Log text box.

26.7.161.58 Statistics Log Text Box The Statistics Log Text box is located under the Progress Text Box. It shows the entire past statistical test data from all stations installed and selected. This data is also logged in a log file with the name entered in the Log File Name field on the Global Configuration screen of the Station Setup program. When more tests are performed than can fit in the Statistics Text Box then a scroll bar will appear on the right side of the box and only the most recent tests will be displayed. Past data can be seen by adjusting the scroll bar. Error codes reported here are of a more generic nature than the ones reported in the **Progress Test Box** as described above. Both error codes will be logged if a log file is open

26.7.161.59 Test# Test# is the number of tests since the software was opened.

26.7.161.60 StationID StationID is the name given to the station when the Station Setup software was run.

26.7.161.61 Date/Time Date and Time is the date and time the tests were performed.

26.7.161.62 Serial# Serial Number is the serial number given to the part. The serial number increments depending on the progress of the tests for each station. No two stations can have the same serial number even if they start at the same time because the software assigns serial numbers in such a way to prevent this. If Skip on Error is selected in the Station Setup software, a failed part will not be assigned a new serial number to help preserve serial numbers for parts that pass.

26.7.161.63 Pass/Fail Error Code This is a more generic error code than the one in the Progress Text Box. The error code given here will tell what test failed. The 2 error codes can be used together to give a better understanding of what caused the error. If the test passed then this will be 0.

26.7.161.64 Filter Results Pull-Down Menu This menu gives the option to filter the data shown in the Statistics Log Text Box to only show data for a specific station or for all stations at one time. It will list the stations by their Station ID.

26.7.161.65 Next Calibration Due The *Next Calibration Due* Indicator indicates when the Multi-Station software will require a calibration of the Voltage, Current, and Temperature references due to timeout of an adjustable software timer in the global.ini file as shown in Figure 14. There are 3 adjustable values of interest in this file under the [CalRemind] Header:

1. REM_Timed_CalInterval: This is the period in minutes between forced calibrations.
2. REM_SnoozeInterval: This is the approximate time between reminders.
3. REM_SnoozeCount: This is the number of reminders that will occur prior to forced calibration.

Default settings are shown in Figure 14. With these settings the interval time will be 70 minutes. There will be 2 reminders prior to the 70 minute expiration. Each of these reminders will be 5 minutes apart so one will be at 60 minutes and the next would be at 65. Then at 70 minutes the *Start* button will be disabled until *VTI* Calibration Verification is performed. Adjustments can be made to this file to modify these settings. Caution should be taken when modifying the global.ini file. Only change the numbers beside the values. Any other changes could cause unpredictable results.

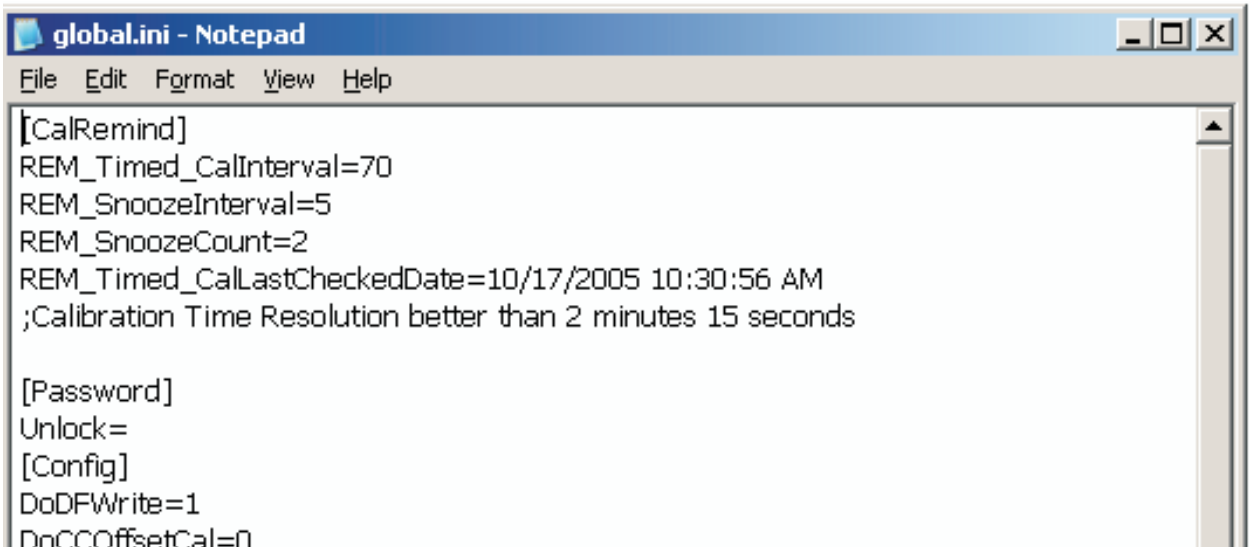


Figure 14. Global.ini file

26.7.161.66 "Allow Testing" Button The *Allow Testing* button is pressed by the user to continue testing if a forced calibration reminder expires as described in *Next Calibration Due* above.

26.7.161.67 Real Time "Statistics" The Statistics data displayed on the lower right corner of the main window displays real time test statistics for all stations combined.

26.7.161.68 Number Tested This text box displays the total number of devices that have been tested on all test stations.

26.7.161.69 Number Passed This text box displays the total number of devices that have passed the test on all test stations.

26.7.161.70 Number Failed This text box displays the total number of devices that have failed the test on all test stations.

26.7.161.71 Passed per Hour This text box displays the number of devices that have passed the test on average per hour.

26.7.161.72 Rows to Show on Screen The system only remembers the statistical data from the number of tests that are selected in the *Rows to show on screen* pull-down menu.

26.7.161.73 "Start" Button The start button is disabled every time the Multi-Station software is executed. VTI configuration must be verified to enable the *Start* button. Once this button is enabled, clicking it initiates testing at each of the installed stations that were setup and initialized with the Station Setup software. Each station performs its test independently of the others. The software tracks the test progress from each station.

26.8 Source Code

The bqMTester software has 4 executables. Two of them are used for testing. They are the bqTester.EXE file and the MultiStationTester.EXE. When running bqMultiStationTester.exe, there is a separate instance of bqTester.EXE running in the background for every testing station connected to the PC. There can be a maximum 12 instances of this program. MultiStationTester.EXE is only a data translation program for all the instances of bqTester running. Since MultiStationTester.exe is not involved in actual testing it is not necessary to modify. The inner workings of MultiStationTester.exe are extremely complicated to handle 12 station data all at one time . For these reasons we do not supply the source code for MultiStationTester.EXE. We supply the bqTester source code since it is directly involved in testing. It includes all that the user should ever need to modify.

The source code is also available for TesterDFReader.exe. This is primarily given as an example to the user on how the Golden Image File is created. This is a very common question from customers and therefore we supply this code as a reference.

Contact Texas Instruments for a copy of the source code. Texas Instruments does not supply technical support resources for code modifications and is not responsible for customer modified source code. The source code is given as-is.

- Unzip bqTester102SourceSetup.zip into a directory of your choice.
- Run the bqTester102SourceSetup.exe. This will install the source files into *C:\bqSource* directory (Replace *C:* with the label for your hard drive).
- Install Visual Basic 6.0 and Service Pack 5 according to the instructions which came with the software.
- Run Visual Basic 6.0 and select File:Open Project. When the dialog box opens, navigate to the *bqSource* directory and choose the file named bqTester.vbp.
- Make desired changes and recompile bqTester.EXE.
- Copy the new bqTester.EXE into the directory where bq Tester software was installed. (It is recommended to keep a copy of the original bqTester.exe file)

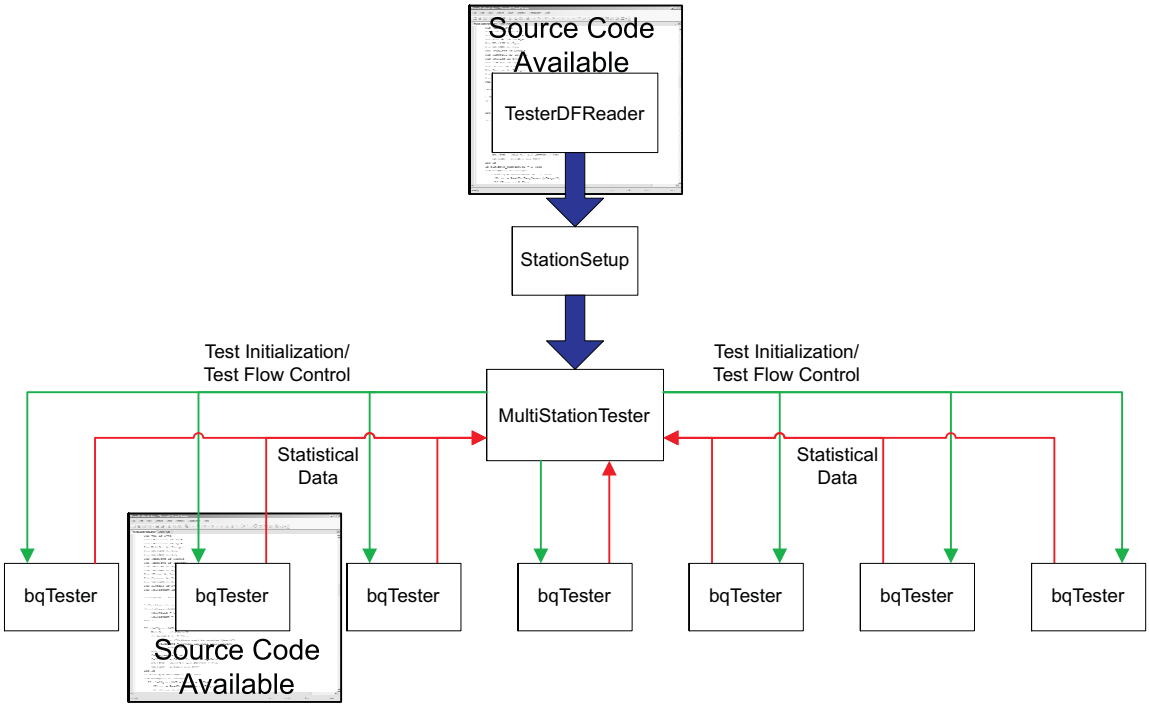


Figure 15. Source Code is Available for bqTester.exe and TesterDFReader.exe

Theory of Operation for HPA169 Calibration Board

The HPA169 multi-site tester board consists of three sections, a communication, control, and temperature section, a voltage supply section, and a current supply section. The board has been designed to be temperature independent. The board can be controlled through SMBUS via an EV2300 interface, or through a user designed custom interface supporting I2C. The board schematic shown below has been divided to show the three sections.

The communication, control, and temperature section consists of two ICs, a TMP100NA Digital Temperature Sensor with I2C interface, and a TPIC2810D 8-bit LED Driver with I2C interface. The TMP100NA is used to report the board temperature through SMBUS or I2C. The TPIC2810D is used not only to control board status LEDs, but also to enable and disable the voltage and current sections by controlling two optoisolators. Power for these two devices (5 VDC) is supplied from the EV2300 or custom user interface from the computers USB port. Headers have been provided on the board for the addition of an external I2C temperature sensor, an additional I2C communication port, and external status LEDs.

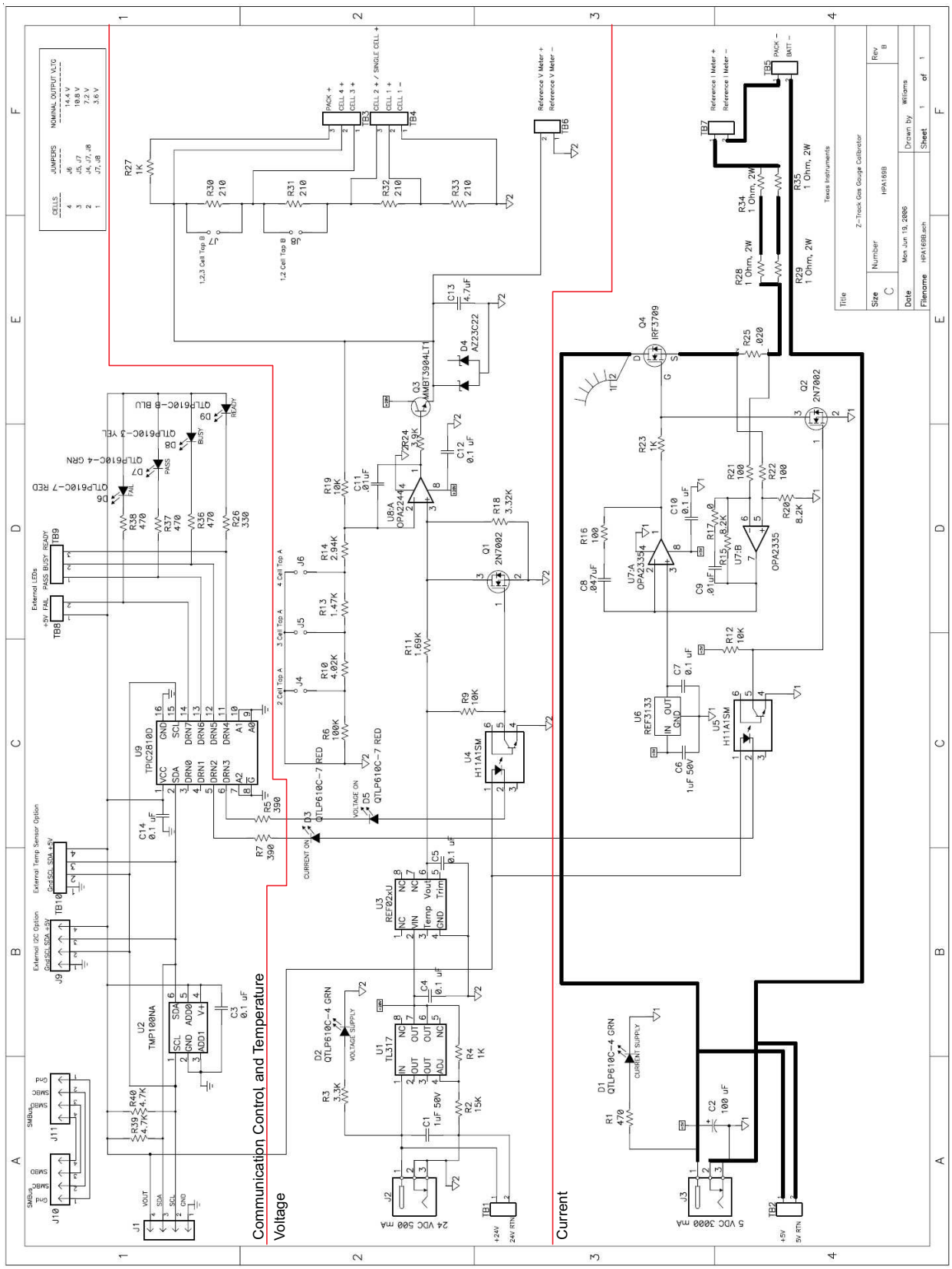
The voltage supply section consists of a TL317 100mA Adjustable Positive Voltage Regulator set to supply 20 VDC, a REF02 +5V Precision Voltage Reference, a H11A817B optoisolator, a 2N7002 N-channel FET, a OPA2244 dual op amp, a MMBT3904LT1 general purpose NPN transistor, and various capacitors, and resistors. Power is supplied to the voltage supply section with a 24V, 500mA wall mounted power supply. When power is supplied to the voltage supply section, the *Voltage Supply* LED will light, the TL317 will supply 20 V, and the REF02 will supply a 5 V reference. The REF02 is a high precision reference with very low temperature drift. The voltage divider formed by R11 and R18 will cause 3.3 V to appear on the positive input of the OPA2244 error amp. R11 and R18 are high precision 0.5% 25 PPM resistors. These values are critical to ensure 3.3 V is supplied to the positive input of the error amp. Resistors R6, R10, and R13 are selectable with jumpers J4, J5, and J6, and control the gain of the error amp so that its output is 14.4 V, 10.8 V, 7.2 V, or 3.6 V depending on the number of series cells being simulated. The MMBT3904LT1 FET provides current boost. R30, R31, R32, and R33 are the jumper selectable cell simulation resistors. Jumpers J7 and J8 are used to select 2, 3, or 4 series cells. The voltage selected by jumpers J4, J5, and J6 will be divided over the cell simulation resistors. Appropriate jumpers should be selected so that the supplied voltage divided by the number of cells simulated is equal to 3.6V. The H11A817B optoisolator and 2N7002 FET are used to enable or disable the voltage supply. An enable or disable command is sent via SMBUS from the EV2300 or user supplied I2C controller to the TPIC2810D LED driver which then enables or disables the appropriate output pin which is connected to the H11A817B optoisolator. This causes the optoisolator to turn on or turn off the 2N7002 FET which in turn will ground or unground the positive input of the OPA2244 error amp. Grounding the input will cause the output of the error amp to go to 0 V, which will disable the voltage supply. The transition of the TPIC2810D output pin will also cause the *Voltage On* LED to light or go out.

The current supply section consists of a REF3130 +3V Precision Voltage Reference, a H11A817B optoisolator, a 2N7002 N-channel FET, a OPA2335 dual op amp, a IRF3709 FET, a 20 milliohm sense resistor, 4 1 ohm 2W resistors, and various capacitors and resistors. Power is supplied to the current supply section with a 5V, 3A wall mounted power supply. When power is supplied to the current supply section, the *Current Supply* LED will light. Current flows from the power supply, through the IRF3709 FET, through the 20 milliohm sense resistor, through the 1 ohm 2 W heat dissipating resistors, through a user supplied reference meter, through the sense resistor in the unit under test, and back to the wall mounted power supply. This current will induce a voltage across the 20 milliohm sense resistor which is then amplified by the differential amplifier (U7:B). The voltage from the differential amplifier is then fed back into the error amp (U7:A). The error amp gets its reference voltage from the REF3133 +3.3V voltage reference. The REF 3133 is a high precision reference with very low temperature drift. The output of the error amp drives the gate of the IRF3709 FET. This feedback arrangement ensures that the current in the current loop remains exactly 2 A regardless of the temperature. The H11A817B optoisolator and 2N7002

FET are used to enable or disable the current supply. An enable or disable command is sent via SMBUS from the EV2300 or user supplied I2C controller to the TPIC2810D LED driver which then enables or disables the appropriate output pin which is connected to the H11A817B optoisolator. This causes the optoisolator to turn on or turn off the 2N7002 FET which in turn will ground or unground the gate of the IRF3709 FET. Grounding the gate will turn off the FET and disable the current supply. The transition of the TPIC2810D output pin will also cause the *Current On* LED to light or go out.

Appendix 28

HPA169 Schematic


Communication Control and Temperature
Voltage
Current
Z-Track Gas Gauge Calibrator
Texas Instruments
HPA169B
Mon Jun 19, 2006
HPA169B.sch
Williams
Rev B
Sheet 1 of 1
Size C
Number
Title
Filename
Drawn by
CELLS
JUMPERS
NOMINAL OUTPUT VLTG
14.4 V
10.8 V
7.2 V
3.6 V
PACK +
CELL 4 +
CELL 3 +
CELL 2 + / SINGLE CELL +
CELL 1 +
CELL 1 –
PACK – BATT –
Reference I Meter +
Reference I Meter –
Reference V Meter +
Reference V Meter –
1,2,3 Cell Top B
1,2 Cell Top B
4 Cell Top A
3 Cell Top A
2 Cell Top A
External LEDs
+5V FAIL PASS BUSY READY
External Temp Sensor Option
External I2C Option
SMBus
24 VDC 500 mA
5 VDC 3000 mA
+24V
24V RTN
+5V
5V RTN
VOUT SDA SCL GND
VOLTAGE ON
CURRENT ON
VOLTAGE SUPPLY
CURRENT SUPPLY
QTLP610C-7 RED
QTLP610C-3 YEL
QTLP610C-4 GRN
QTLP610C-8 BLU
FAIL
PASS
BUSY
READY
TPIC2810D
TMP100NA
REF02xU
TL317
REF3133
H11A1SM
OPA2335
OPA2244
OPA2334
MMBT3904LT1
2N7002
IRF3709
AZ23C22

HPA169 Cal Board Bill of Materials

Table 1. HPA169A Bill of Materials

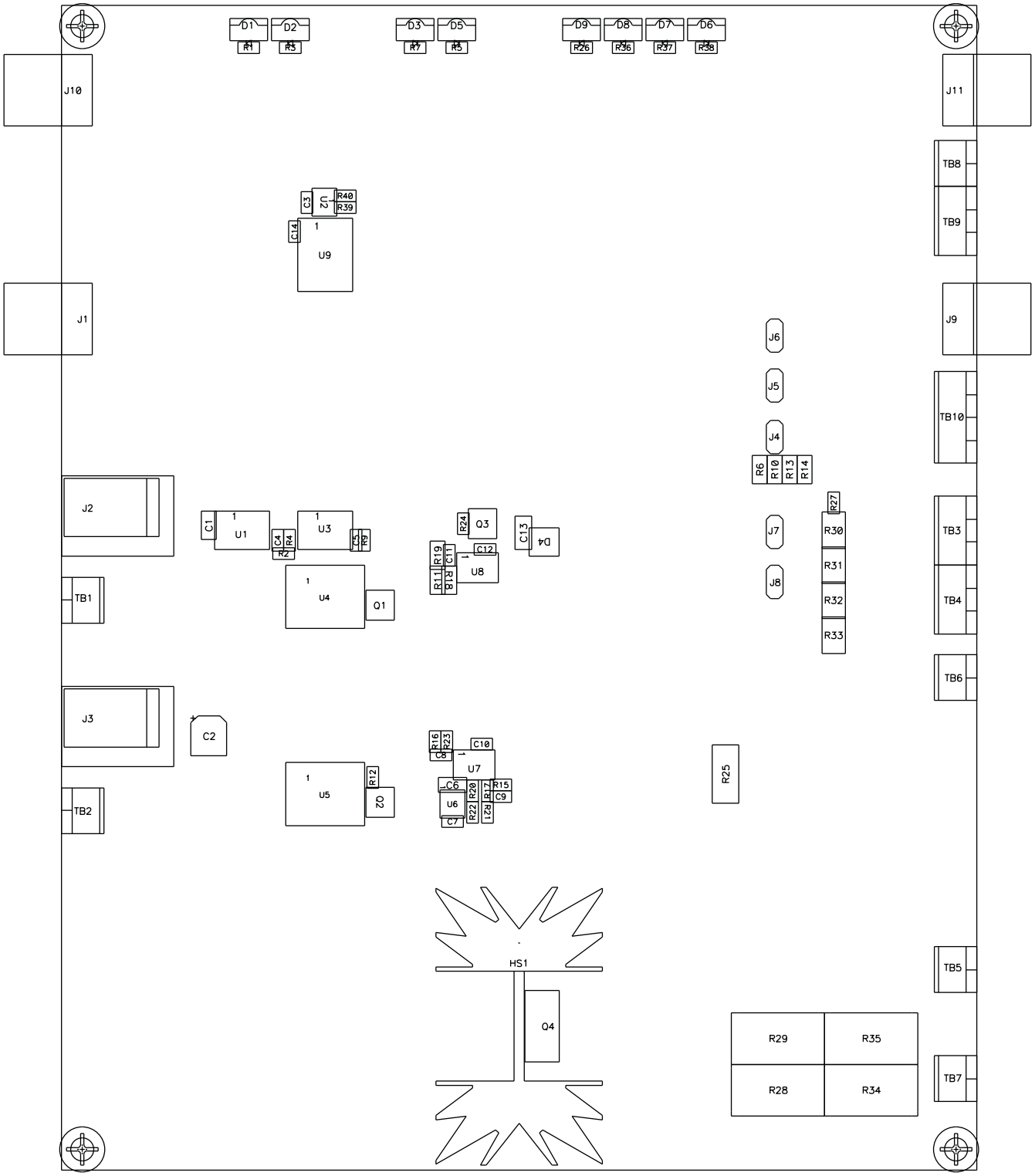
COUNT	REF DES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
2	C1, C6	1uF 50V	Capacitor, Ceramic, 1.0uF, 50-V, X7R, 15%	1206	STD	Any
1	C13	4.7uF	Capacitor, Ceramic, 4.7 uF, 25 V, X7R, 10%	1206	STD	Any
1	C2	100 uF	Capacitor, Aluminum, 100-uF, 10-V, 20%	0.177 x 0.177	ECE-V1AA1010WR	Panasonic
7	C3, C4, C5, C7, C10, C12, C14	0.1 uF	Capacitor, Ceramic, 0.1-uF, 50-V, X7R, 10%	0603	STD	Any
1	C8	0.047uF	Capacitor, Ceramic, 0.047 uF, 50 V, X7R, 10%	0603	STD	Any
2	C9, C11	.01uF	Capacitor, Ceramic, 0.01-uF, 25-V, X7R, 15%	0603	STD	Any
3	D1, D2, D7	QTLP610C-4 GRN	Diode, LED green, 30-mA, xx-mcd	0.126 x 0.087 inch	QTLP610C-4	Fairchild
3	D3, D5, D6	QTLP610C-7 RED	Diode, LED Red, 30-mA, 25-mcd	0.126 x 0.087 inch	QTLP610C-7	Fairchild
1	D4	AZ23C22	Diode, Dual, Zener, 22V, 300mW	SOT23	AZ23C22	Vishay-Telefunken
1	D8	QTLP610C-3 YEL	Diode, LED yellow, 30-mA, xx-mcd	0.126 x 0.087 inch	QTLP610C-3	Fairchild
1	D9	QTLP610C-B BLU	Diode, LED blue, 30-mA, xx-mcd	0.126 x 0.087 inch	QTLP610C-B	Fairchild
1	HS1	6298B	Heatsink, TO-220, Vertical-mount, 3.9*C/W	1.67 x 1.00	6298B	Thermalloy
4	J1, J9, J10, J11	22-05-3041	Header, Friction Lock Ass'y, 4-pin Right Angle	0.400 x 0.500	22-05-3041	Molex
1	J2	24 VDC 500 mA	Connector, 2,1mm, DC Jack w/Switch, TH	0.57 x 0.35	RAPC 722	Switchcraft
1	J3	5 VDC 3000 mA	Connector, 2,1mm, DC Jack w/Switch, TH	0.57 x 0.35	RAPC 722	Switchcraft
5	J4, J5, J6, J7, J8		Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2"	PTC36SAAN	Sullins
2	Q1, Q2	2N7002	MOSFET, N-ch, 60-V, 115-mA, 1.2-Ohms	SOT23	2N7002DICT	Vishay-Liteon
1	Q3	MMBT3904LT1	Bipolar, NPN, xx-V, yy-mA, zz-W	SOT23	MMBT3904LT1	On Semi
1	Q4	IRF3709	MOSFET, N-ch, 30V, 90A, 9 milliohm	TO-220AB	IRF3709	IR
4	R1, R36, R37, R38	470	Resistor, Chip, 470-Ohms, 1/16-W, 5%	0603	Std	Std
1	R10	4.02K	Resistor, Chip, 4.02K-Ohms, 1/10-W, 0.5%, 25PPM	0805	Panasonic ERA-6YHD	Panasonic
1	R11	1.69K	Resistor, Chip, 1.69K-Ohms, 1/10-W, 0.5%, 25PPM	0805	Panasonic ERA-6YHD	Panasonic
1	R13	1.47K	Resistor, Chip, 1.47K-Ohms, 1/10-W, 0.5%, 25PPM	0805	Panasonic ERA-6YHD	Panasonic
1	R14	2.94K	Resistor, Chip, 2.94K-Ohms, 1/10-W, 0.5%, 25PPM	0805	Panasonic ERA-6YHD	Panasonic
2	R15, R20	8.2K	Resistor, Chip, 8.2K-Ohms, 1/16-W, 0.1%, 25ppm	0603	Panasonic ERA-3YEB	Panasonic
1	R16	100	Resistor, Chip, 100-Ohms, 1/16-W, 5%	0603	Std	Std
1	R17	0	Resistor, Chip, 0-Ohms, 1/16-W, 5%	0603	Std	Std
1	R18	3.32K	Resistor, Chip, 3.32K-Ohms, 1/10-W, 0.5%, 25PPM	0805	Panasonic ERA-6YHD	Panasonic
1	R19	10K	Resistor, Chip, 10K-Ohms, 1/10-W, 0.5%, 25PPM	0805	Panasonic ERA-6YHD	Panasonic
1	R2	15K	Resistor, Chip, 15K-Ohms, 1/16-W, 5%	0603	Std	Std
2	R21, R22	100	Resistor, Chip, 100-Ohms, 1/16-W, 0.1%, 25ppm	0603	Panasonic ERA-3YEB	Panasonic
1	R24	3.9K	Resistor, Chip, 3.9K-Ohms, 1/16-W, 5%	0603	Std	Std
1	R25	0.02	Resistor, Chip, 0.02-Ohms, 1-W, 1%, 50ppm	2512	WSL-2512-010 1% R86	Vishay
1	R26	330	Resistor, Chip, 330-Ohms, 1/16-W, 5%	0603	Std	Std
4	R28, R29, R34, R35	1 Ohm, 2W	Resistor, Metal Strip, 1-Ohms, 2-W, 5%	4527	WSR21R000JEK	Vishay Dale
1	R3	3.3K	Resistor, Chip, 3.3K-Ohms, 1/16-W, 5%	0603	Std	Std

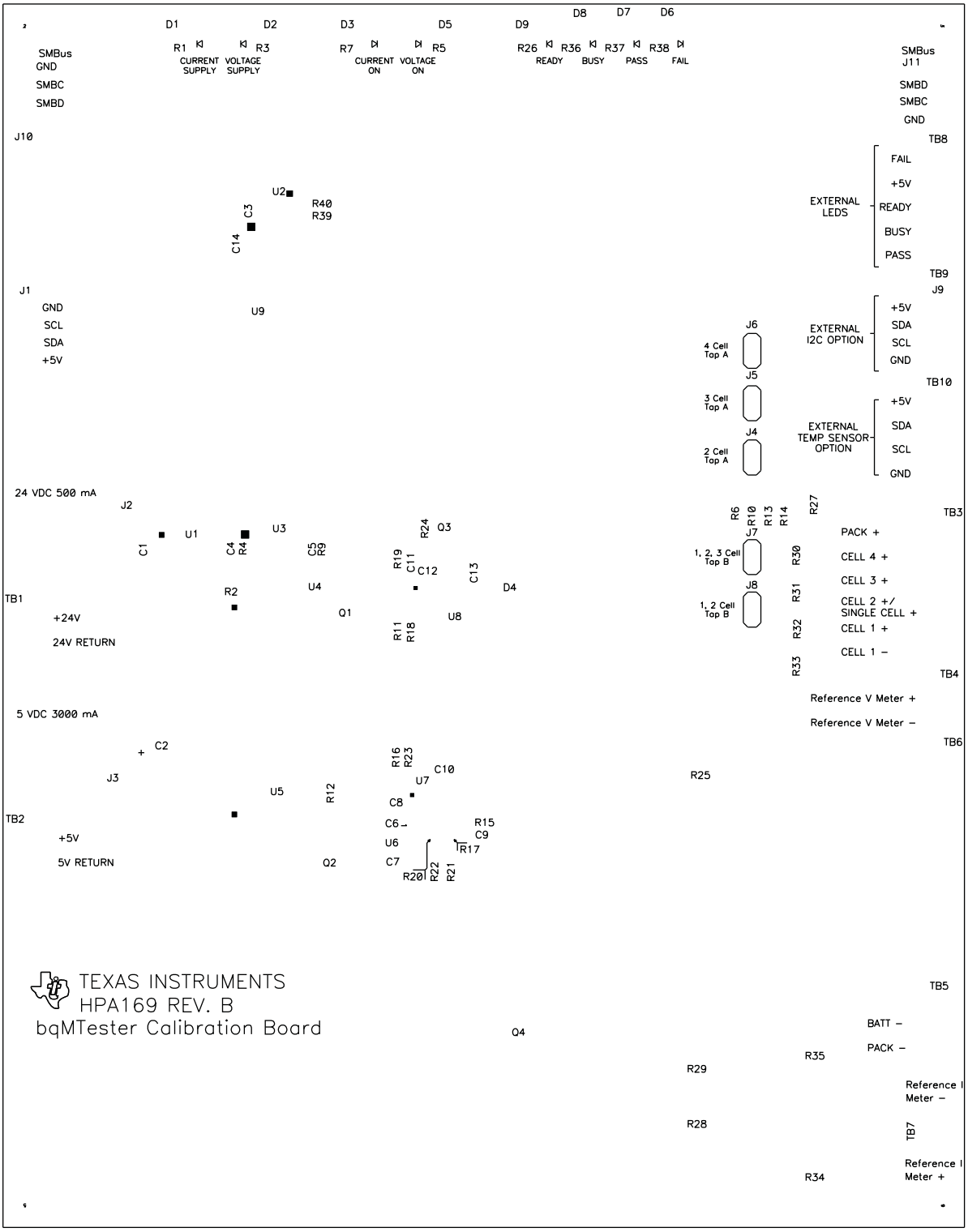
Table 1. HPA169A Bill of Materials (continued)

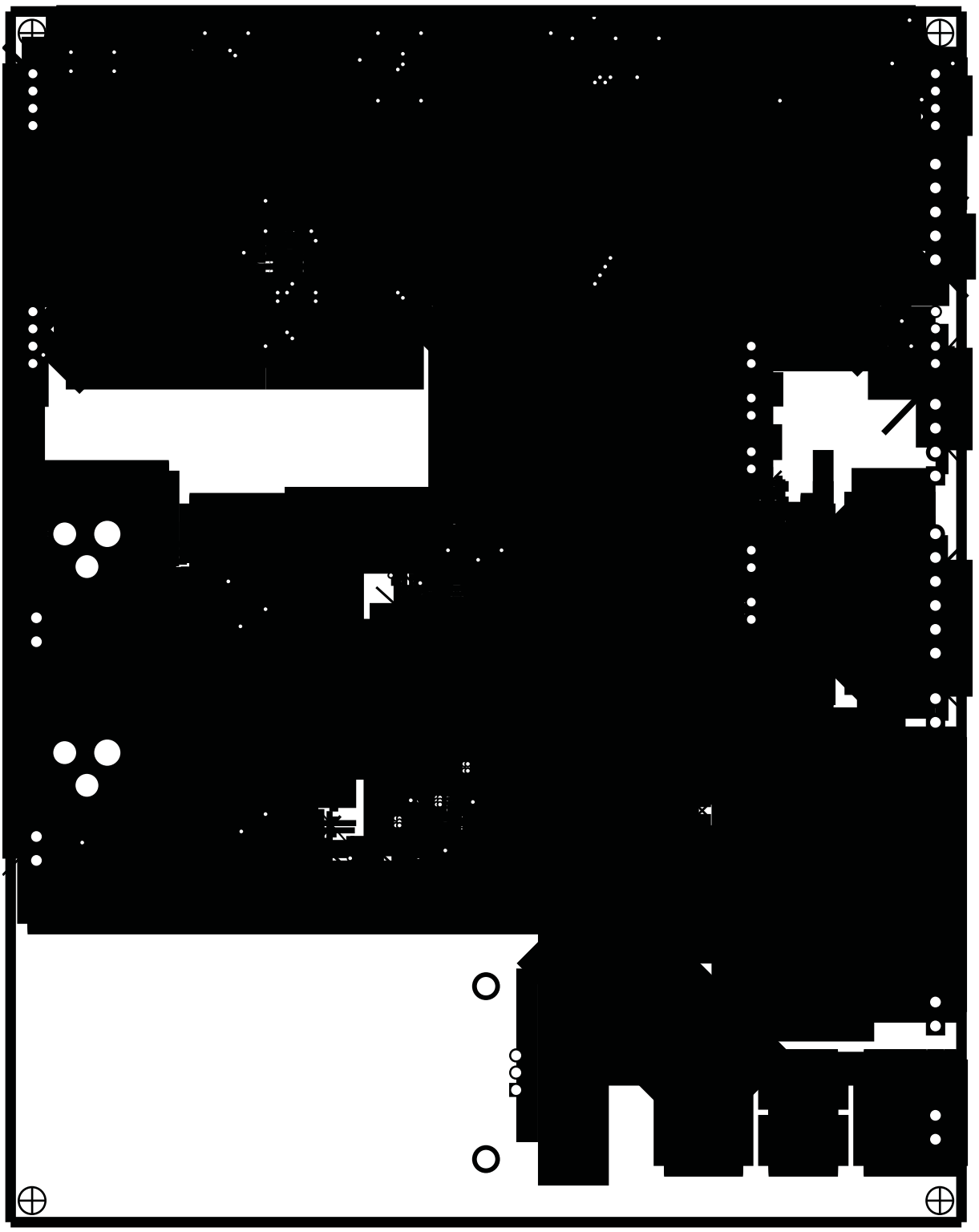
COUNT	REF DES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
4	R30, R31, R32, R33	210	Resistor, Chip, 210-Ohms, 1/4-W, 0.1%, 25-PPM	1210	Panasonic ERA-14EB	Panasonic
2	R39, R40	4.7K	Resistor, Chip, 4.7K-Ohms, 1/16-W, 5%	0603	Std	Std
3	R4, R23, R27	1K	Resistor, Chip, 1K-Ohms, 1/16-W, 5%	0603	Std	Std
2	R5, R7	390	Resistor, Chip, 390-Ohms, 1/16-W, 5%	0603	Std	Std
1	R6	100K	Resistor, Chip, 100K-Ohms, 1/10-W, 0.5%, 25PPM	0805	Panasonic ERA-6YHD	Panasonic
2	R9, R12	10K	Resistor, Chip, 10K-Ohms, 1/16-W, 5%	0603	Std	Std
6	TB1, TB2, TB5, TB6, TB7, TB8		Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25	ED1514	OST
1	TB10	ED1516	Terminal Block, 4-pin, 6-A, 3.5mm	0.55 x 0.25	ED1516	OST
3	TB3, TB4, TB9		Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25	ED1515	OST
1	U1	TL317	IC, 3-Terminal Adjustable Regulator	SO-8	TL317CD	TI
1	U2	TMP100NA	IC, Digital Temperature Sensor With I^2C Interface	SOT23-6	TMP100NA	TI
1	U3	REF02BU	IC, +5V Precision Voltage Reference	SO-8	REF02BU	TI
2	U4, U5	H11A817B	IC, OPTOISOLATOR, H11A817B	SOP-6	H11A817BS_NF098	Fairchild
1	U6	REF3133	IC, Voltage Reference, 15ppm/°C Max, 100uA	SOT23	REF3133AIDBZ	TI
1	U7	OPA2335	IC, Single Supply CMOS Op Amp, Dual, 0.05 V/ °C max,	MSOP-8	OPA2335AIDGK	TI
1	U8	OPA2244	IC Single Supply Dual Opamp	MSOP-8	Digikey OPA2244EACT-ND	TI
1	U9	TPIC2810D	IC, 8--Bit Led Drive With I^2C Interface	SO16	TPIC2810D	TI

Appendix 30

HPA169 Board Layout


D1
D2
D3
D5
D9
D8
D7
D6
J10
J11
TB8
TB9
U2
R40
R39
C3
C14
U9
J1
J9
J6
J5
J4
TB10
R6
R10
R13
R14
J2
C1
U1
U3
C4
R4
R2
C5
R9
R24
Q3
C13
D4
R19
C11
C12
R11
R18
U8
R27
J7
R30
R31
R32
R33
TB3
TB4
TB6
TB1
U4
Q1
J8
J3
C2
R16
R23
C8
C10
U7
C6
R20
R17
R15
C9
R22
R21
C7
U6
R12
U5
Q2
R25
HS1
Q4
TB5
R29
R35
R28
R34
TB7
TB2


D1
D2
D3
D5
D9
D8
D7
D6
R1
R3
R7
R5
R26
R36
R37
R38
CURRENT SUPPLY
VOLTAGE SUPPLY
CURRENT ON
VOLTAGE ON
READY
BUSY
PASS
FAIL
SMBus
GND
SMBC
SMBD
J10
SMBus
J11
SMBD
SMBC
GND
TB8
FAIL
+5V
READY
BUSY
PASS
EXTERNAL LEDS
TB9
J1
GND
SCL
SDA
+5V
U2
R40
R39
C3
C14
U9
J9
+5V
SDA
SCL
GND
EXTERNAL I2C OPTION
TB10
J6
4 Cell Top A
J5
3 Cell Top A
J4
2 Cell Top A
EXTERNAL TEMP SENSOR OPTION
+5V
SDA
SCL
GND
24 VDC 500 mA
J2
U1
U3
C1
C4
R4
C5
R9
R24
Q3
R19
C11
C12
C13
D4
U4
R2
Q1
U8
R11
R18
TB1
+24V
24V RETURN
R6
R10
R13
R14
R27
J7
1, 2, 3 Cell Top B
J8
1, 2 Cell Top B
R30
R31
R32
R33
TB3
PACK +
CELL 4 +
CELL 3 +
CELL 2 +/ SINGLE CELL +
CELL 1 +
CELL 1 –
TB4
Reference V Meter +
Reference V Meter –
TB6
5 VDC 3000 mA
C2
J3
U5
R12
R16
R23
C10
U7
C8
C6
R15
C9
R17
U6
C7
R20
R22
R21
Q2
TB2
+5V
5V RETURN
R25
TEXAS INSTRUMENTS
HPA169 REV. B
bqMTester Calibration Board
Q4
TB5
BATT –
PACK –
R35
R29
R28
R34
Reference I Meter –
Reference I Meter +
TB7



Error Code Definitions

Table 1. Error Code Definitions

Error Code	Error #	Description	Most Probable Cause	Possible Action
NO_ERROR	0	Successful (No errors)		
LOST_SYNC	1	EV2300 lost synchronization	EV2300 has outdated firmware or drivers are outdated.	Contact TI to get EV2300 with latest firmware. Ensure latest drivers for EV2300 installed.
NO_USB	2	USB Connection Missing	No EV2300 is connected.	Close program, reboot, and connect EV2300 first.
BAD_PEC	3	Bad PEC on SMBus	Possible Bad hardware.	Replace EV2300 / target board
WRONG_NUM_BYTES	5	Unexpected number of bytes sent/received	Unexpected hardware behavior.	May need assistance from TI
T2H_UNKNOWN	6	SMBus communication terminated unexpectedly / timed out or the bus was busy.	Wrong kind of target connected or target timing is off Trim oscillator	make sure that the target mode accepts the SMB command being sent
INCORRECT_PARAM	7	Invalid parameter type passed to function – especially Variant argument.	Incorrect parameter in call to function. Software Bug or overflow	Contact TI
TIMEOUT_ERROR	8	USB Timeout	No response on USB	EV2300 or driver problems or software is not supposed to wait for a response.
INVALID_DATA	9	AssemblePacket could not build a valid packet	Bad data / bad packet. Software found problem with data	Possible version incompatibility between BqTester and Module under test.
ERR_UNSOLICITED_PKT	10	Found an unsolicited non-error packet when looking for error packets	Unexpected packet received. The packet may be a response from a previous transaction that failed or that did not check the response.	Make corrections to software
COMPARE_DIFFERENT	11	Comparison failed and data read is different from srec	Flash comparison results in mismatch. Possible Flash failure or SMBus failure.	Module under test Flash failure
BQ80XRW_OCX_INTERNAL_ERROR	12	Problems with pointers being NULL etc.	Possible software bug or overflow.	Contact TI
USER_CANCELLED_OPERATION	34	User clicked on cancel button on progress bar dialog		
DF_CHECKSUM_MISMATCH	51	Data Flash checksum mismatch	Flash comparison results in mismatch. Possible Flash failure or SMBus failure.	Module under test Flash failure
IF_CHECKSUM_MISMATCH	52	Instruction Flash checksum mismatch	Flash comparison results in mismatch. Possible Flash failure or SMBus failure.	Module under test Flash failure
OPERATION_UNSUPPORTED	53	Unsupported type	Software problem	Check that Module under test and bqTester versions are compatible. Then contact TI
ERR_TOO_MANY_QUERIES	81	Not used		
ERR_BAD_QUERY_ID	82	Not used		

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
BAD_CRC	83	Packet was corrupted during USB communication	Too much noise or bad connection	
ERR_TOO_MANY_RESPONSES	84	Not used		
ERR_NO_QUERIES_TO_DELETE	85	Not used		
ERR_QUERY_UNAVAILABLE	86	Not used		
ERR_NO_RESPONSES_TO_DELETE	87	Not used		
ERR_RESPONSE_UNAVAILABLE	88	Not used		
ERR_TMMT_NO_RESPONSE	90	Not used		
T2H_ERR_TIMEOUT	92	SMBus communication terminated unexpectedly / timed out or the bus was busy.	Wrong kind of target connected or target timing is off Trim oscillator	make sure that the target mode accepts the SMB command being sent
BUS_BUSY	94	SMBus communication terminated unexpectedly / timed out or the bus was busy.	Wrong kind of target connected or target timing is off Trim oscillator	make sure that the target mode accepts the SMB command being sent
T2H_ERR_BAD_SIZE	95	SMBus communication terminated unexpectedly / timed out or the bus was busy.	Wrong kind of target connected or target timing is off Trim oscillator	make sure that the target mode accepts the SMB command being sent
ERR_BAD_PAYLOAD_LEN	97	Packet was corrupted during USB communication or software sent in a bad packet	Bad USB connection	Check Version Compatiblitiy and USB cable
ERR_TMMT_LIST_FULL	98	Not used		
ERR_TMMT_BAD_SELECTION	99	Not used		
UNKNOWN	100	Unexpected/unknown error		Outdated software Contact TI
UNEXPECTED_ERROR	110	Should not happen	Unexpected error	Hardware not expected to respond to this error
OUT_OF_MEMORY	111	Not enough memory on PC		Install more memory
SREC_OPEN_FAIL	221	Srec specified does not exist or cannot be opened	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqMtester softare and Module under Test.
SREC_BAD_START_RECORD	222	Srec not in expected format	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqMtester softare and Module under Test.
SREC_UNKNOWN_TYPE	223	Srec not in expected format	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqMtester softare and Module under Test.
SREC_BAD_CHECKSUM	224	Srec not in expected format	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqMtester softare and Module under Test.
SREC_BAD_RECORD_COUNT	225	Srec not in expected format	SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqMtester softare and Module under Test.
SREC_DEV_MISMATCH	226		SREC targets a different device than the one detected on the SMBus	Ensure version compatibility between bqMtester softare and Module under Test.
CONFIG_OPEN_FAIL	227	Config file not found / cannot be opened		Redo StationSetup.exe configuration
CONFIG_UNEXPECTED_EOF	228	Config file not found / cannot be opened		Redo StationSetup.exe configuration
CONFIG_BAD_FORMAT	229	Config file format incorrect		Redo StationSetup.exe configuration

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
PCFG_DEVVER_MISMATCH	231	Config file device version not compatible		Ensure version compatibility between bqMtester softare and Module under Test.
PCFG_DEV_MISMATCH	232	Config file device not compatible		Ensure version compatibility between bqMtester softare and Module under Test.
PCFG_SRECDEVVER_MISMATCH	233	Srec not compatible with current hardware device		Ensure version compatibility between bqMtester softare and Module under Test.
PCFG_SRECDEV_MISMATCH	234	Srec not compatible with current hardware device		Ensure version compatibility between bqMtester softare and Module under Test.
BCFG_DEVVER_MISMATCH	235	Srec not compatible with current hardware device		Ensure version compatibility between bqMtester softare and Module under Test.
BCFG_DEV_MISMATCH	236	Srec not compatible with current hardware device		Ensure version compatibility between bqMtester softare and Module under Test.
SMBC_LOCKED	260	Unused but reserved for backward compatibility		
	516	Unused but reserved for backward compatibility		
T2H_NACK	772	No response from target	Target not connected/not powered	Connect target and check is correct power is applied
SMBD_LOW	1028	Unused but reserved for backward compatibility		
SMB_LOCKED	1284	Unused but reserved for backward compatibility		
ERR_NOTHINGTODO	5001	Calling the function with specified values resulted in nothing being done		
ERR_VOLTAGE_LESSTHANZERO	5002	Specified Voltage must be greater than 0		
ERR_TEMPERATURE_LESSTHANZERO	5003	Specified temperature must be greater than 0		
ERR_CURRENT_EQUALSZERO	5004	Specified current cannot be 0		
ERR_NOT_IN_CAL_MODE	5010	Gas gauge was not in Calibration mode/ could not be put in calibration mode		
ERR_CALIBRATION_IN_FIRMWARE_ FLASHWRITE	5020	Error writing flash in calibration mode		
ERR_CALIBRATION_IN_FIRMWARE_AFE	5021	Error in AFE calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ PACKV	5022	Error in Pack voltage calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ PACKG	5023	Error in Pack gain calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ VGAIN	5024	Error in Voltage gain calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ CCIGAIN	5025	Error in Current gain calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ TMPOFFEXT1	5026	Error in external temperature 1 offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ TMPOFFEXT2	5027	Error in external temperature 2 offset calibration	Value too large (Overflow) in firmware	

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
ERR_CALIBRATION_IN_FIRMWARE_ TMPOFFINT	5028	Error in internal temperature offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ ADCOFF	5029	Error in ADC offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ BRDOFF	5030	Error in Board offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ CCIOFF	5031	Error in CC offset calibration	Value too large (Overflow) in firmware	
ERR_CALIBRATION_IN_FIRMWARE_ RSVD0	5032	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_ RSVD1	5033	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_ RSVD2	5034	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_ RSVD3	5035	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_ RSVD4	5036	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_ RSVD5	5037	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_ RSVD6	5038	Reserved for future use		
ERR_CALIBRATION_IN_FIRMWARE_ UNDEFINED	5039	Unknown error code returned by hardware	Software is obsolete	
ERR_DF_RD_REQ_B4_WR	5041	Data flash cannot be written before reading the remaining values in a given class		
ERR_INVALID_DATA_ENTERED	5042	Invalid data entered on screen		
ERR_USB_ACQUIRE	5043	EV2300 is locked by another thread	Attempting to do multiple transactions possibly from different windows in background at the same time. Could also be a software problem. Stop scanning in SBS.	
NVALID_FILENAME	65537			Check File Name for Rom File and Log File
DEVICE_VERSION_MISMATCH	65538	Incompatible device/version		Check Connections. Verify version compatibility between bqMtester softare and Module under Test.
RETURN_TO_ROM_FAILED	65539	Gas gauge could not be put in Rom mode	Hardware incompatibility	Check Connections. Verify version compatibility between bqMtester softare and Module under Test.
RUNGG_FAILED	65541	Gas gauge could not exit ROM mode	Hardware incompatibility	Check Connections. Verify version compatibility between bqMtester softare and Module under Test.
WRITEFLASH_GG_FAILED	65542	Writing to flash failed	Data Flash Failure	Module Repair
CALIBRATE_FAILED	65543	Calibration failed	Module hardware failure or Configuration failure	Module Repair or Check Testing Configuration Settings
POST_CAL_CHECKS_FAILED	65544	Post calibration checks failed	Module hardware failure or Configuration failure	Module Repair or Check Testing Configuration Settings
WRITESERIAL_FAILED	65545	Write serial number failed	Data Flash Failure	Module Repair/Retry Test
ERR_UNEXPECTED	65552	Unexpected value/response	Software does not know how to handle this	
ERR_FILE	65553	Error opening/processing File	Wrong File location settings.	Check all File location settings in bqMTester Software

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
ERR_NOT_IN_ROM	65554	GG not in ROM mode when expected – communication failure?	Gas gauge could not be put in ROM	Check Connections. Verify version compatibility between bqMtester softare and Module under Test.
ERR_ENTER_CALMODE	65555	Cannot put GG in Cal mode	Gas gauge could not be put in Calibration mode	Check Connections. Verify version compatibility between bqMtester softare and Module under Test.
ERR_CUSTOM_FUNC	65556	User defined function returned error		
BAD_FILE_FORMAT	65557	Header bad or format bad	Bad image file format	
ERR_WRITE_MFG_DATA	65558	Failed to write manufacturer data	Data Flash Failure	Module Repair/Retry Test
ERR_READ_DEV_VER	65559	Communication error reading device version	Hardware incompatibility	Check Connections. Verify version compatibility between bqMtester softare and Module under Test.
CAL_VOLT_LESSTHANZERO	65600	Calibration voltage must be greater than 0	On screen values incorrect	Verify VTI and Configuration Settings
CAL_TEMP_LESSTHANZERO	65601	Calibration current must be greater than 0	On screen values incorrect	Verify VTI and Configuration Settings
CAL_CURR_LESSTHANZERO	65602	Calibration current must be greater than 0	On screen values incorrect	Verify VTI and Configuration Settings
WRITEFLASH_ROM_FAILED	65560	Failed to write flash while in ROM mode		
SENSE_RES_CAL_HIGH	65570	Sense resistor value too high in post cal checks	Senser Resistor Hardware Failure, Connection Problem, Setting Problem, or HPA169 Power Supply Problem	Verify Sense Resistor Value, check current supply connections, and verify VTI and Configuration Settings. Try increasing tolerances if possible
SENSE_RES_CAL_LOW	65571	Sense resistor value too low in post cal checks	Senser Resistor Hardware Failure, Connection Problem, Setting Problem, or HPA169 Power Supply Problem	Verify Sense Resistor Value, check current supply connections, and verify VTI and Configuration Settings. Try increasing tolerances if possible
VOLT_CAL_HIGH	65580	voltage value too high in post cal checks	Module hardware failure, HPA169 Voltage power supply problem or Configuration failure	Verify Voltage circuit, voltage power supply, VTI, and Configuration Settings. Try increasing tolerances if possible
VOLT_CAL_LOW	65581	voltage value too low in post cal checks	Module hardware failure, HPA169 Voltage power supply problem or Configuration failure	Verify Voltage circuit, voltage power supply, VTI, and Configuration Settings. Try increasing tolerances if possible
TEMP_CAL_HIGH	65590	temperature value too high in post cal checks	Module hardware failure, HPA169 Temperature sensor Failure	Verify VTI settings, and Temperature sensor location
TEMP_CAL_LOW	65591	temperature value too low in post cal checks	Module hardware failure, HPA169 Temperature sensor Failure	Verify VTI settings, and Temperature sensor location
SEAL_CMD_FAILED	65610	Seal command failed	Communication Failure	Check Connections. Verify version compatibility between bqMtester softare and Module under Test.
ERR_READ_CB_INT_TEMP_SENSOR	65611	Error reading internal temperature sensor on HPA169 calibration board	Temperature sensor failure	Verify HPA169 calibration board temperature sensor connections or replace sensor
ERR_READ_CB_EXT_TEMP_SENSOR	65612	Error reading external temperature sensor on HPA169 calibration board	Temperature sensor failure	Verify HPA169 calibration board temperature sensor connections or replace sensor

Table 1. Error Code Definitions (continued)

Error Code	Error #	Description	Most Probable Cause	Possible Action
ERR_CALIBRATION_OUTOFSPEC	65613	Time to recalibrate HPA169 calibration board	VTI calibration Timer expired	Calibrate VTI settings
ERR_TEST_ROUTINE	65614	Reserved		

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 5 V to 24 V and the output voltage range of 3.6 V to 14.4 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 80°C. The EVM is designed to operate properly with certain components above 80°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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