Chapter 2: Cell Connections for PowerLAN Master Gateway Controller

BMS - HCE

The PowerLAN Master Gateway Controllers have a specific power up connection sequence. This refers to the order in which the three or four cell voltages are applied. The cell power up sequence is VSS, V2, V1, V4 and then V3. Following this sequence will insure reliable operation. A power down method is also presented.

2.0 Cell Voltage Pin Descriptions

There are five pins on the PowerLAN Master Gateway Controller that are the focus of this discussion: VSS, V1, V2, V3 and V4. See Figure 1 for a pin diagram of the device.

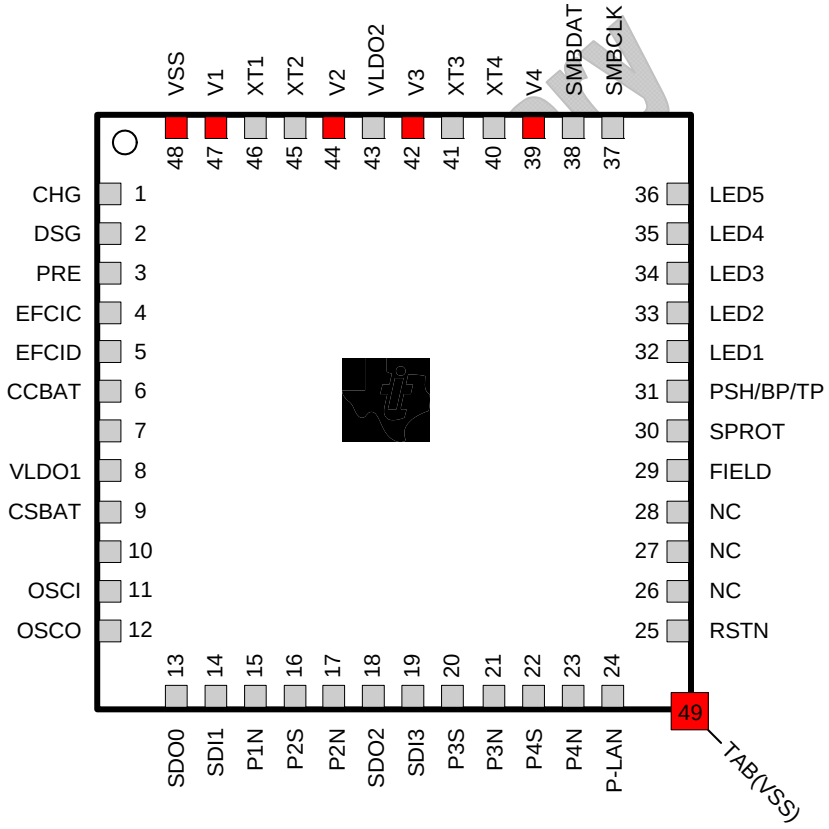

Figure 1. PowerLAN Master Gateway Controller

The following Table 1 describes the functions of the five cell connection pins. The cell whose reference is connected to the reference of the battery pack (B-) is cell 1. Then cell 2 is the one immediately above that cell and so forth. Figure 2 shows the connections for a 4S pack that explicitly includes the extra connections for the battery stack.

Table 1. Cell Voltage Pin Description

Pin Name	Description
VSS	Device ground and connection to Cell 1 reference
V1	Cell 1 Voltage
V2	Cell 2 Voltage
V3	Cell 3 Voltage
V4	Cell 4 Voltage

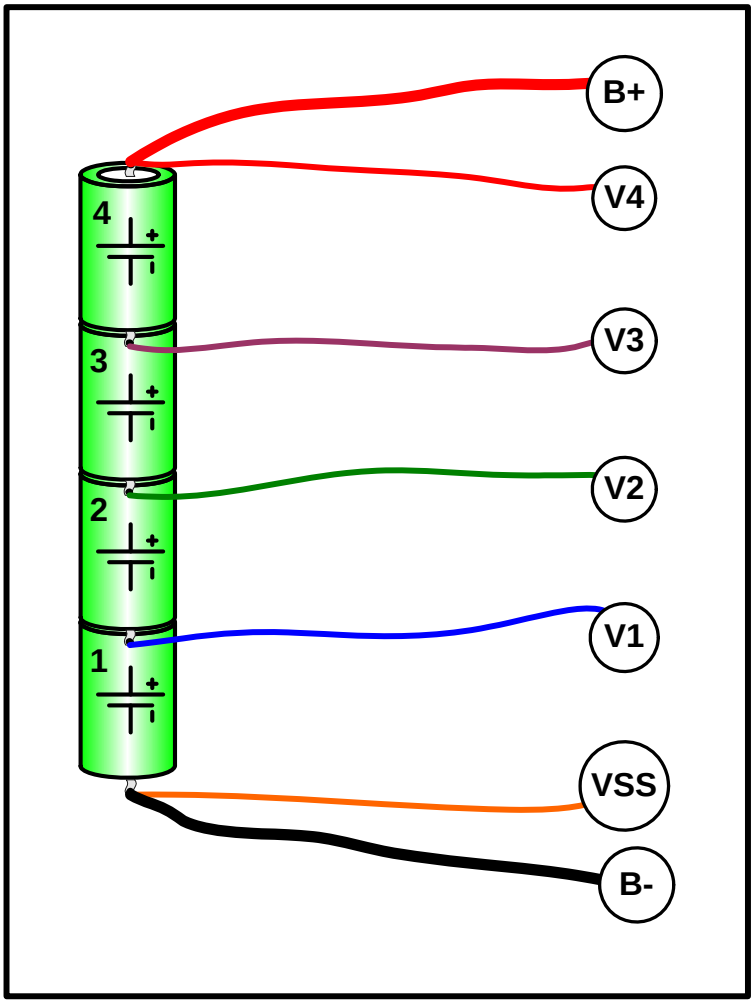

Figure 2. Battery Pack made of four series (4S) cells.

2.1 Cell Voltage Pin Functions

The cell connections to the device serve multiple purposes. These include providing power to the VLDOs, cell voltage measurement, driving PowerPump output control pins (P1N, P2S, P2N, etc) and control of the EUV mode. Figure 3 is a partial block diagram of the operation of the bq78PL116 showing interaction of cell connections and internal circuitry. Not all circuit block interactions are shown – only the ones pertinent to this discussion. For instance, the interaction of the VLDO with the delta-sigma converters is not explicitly shown.

The connections between the device and the cells should be very low impedance. Any significant voltage drop (> than a few mV) in these lines can have a direct effect on the performance of the device.

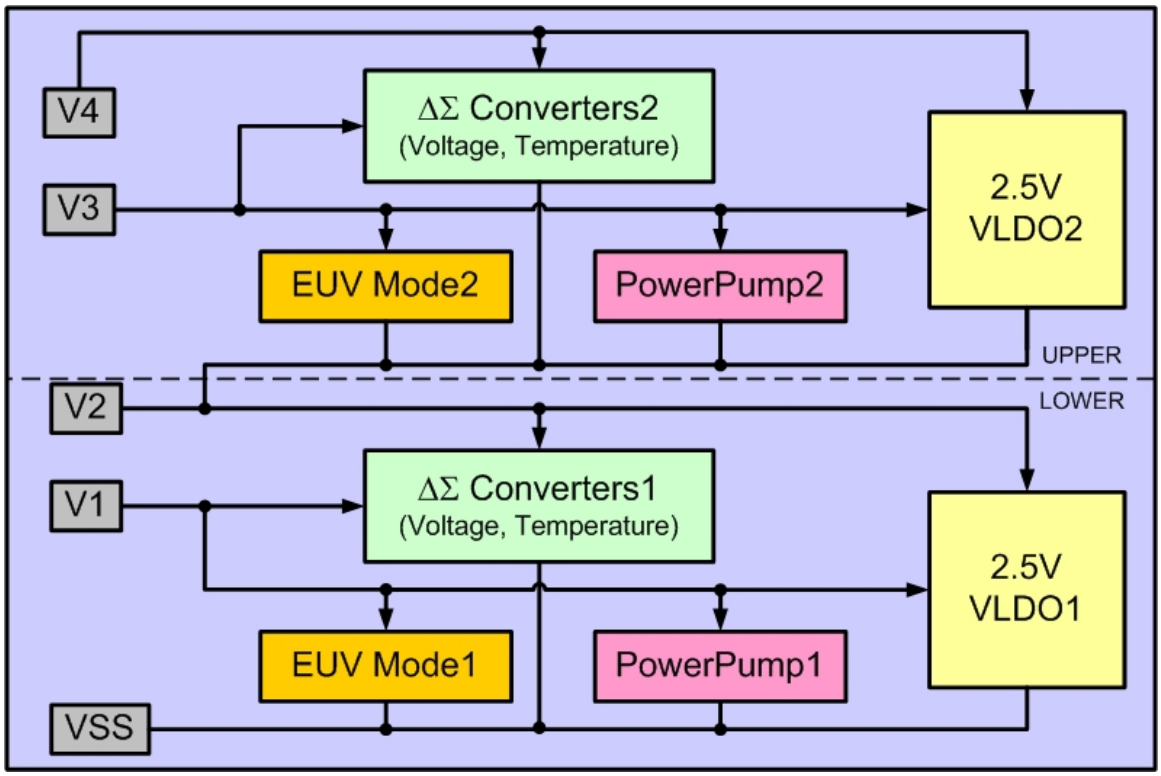

Figure 3. Cell Connection to Internal Circuits

2.1.1 Power to VLDO1, VLDO2

There are two identical, low drop out (LDO) regulators in the bq78PL116 that are called VLDO1 and VLDO2. They both are rated at 2.5V with respect to their grounds.

The majority of power from VLDO1 is used for the microcontroller that is inside the bq78PL116. Secondarily, the lower (1) delta-sigma modulators, PowerPump and EUV circuitry are also powered by VLDO1. Since the PowerLAN system is always three or more series cells, the power for VLDO1 is always sourced between V2 and VSS. V1 has a connection to the VLDO1 but, current from V1 to the VLDO1 is negligible.

The second LDO, called VLDO2, strictly provides power to the upper (2) delta-sigma modulators, PowerPump and EUV circuitry. Its power source is dependent on the series cell count. For three series cell applications pins V3 and V4 are shorted together externally on the printed circuit board (PCB) and power is provided between V3 and V2. For four cell applications, power is sourced between V4 and V2.

Figure 2 shows that each VLDO has both a lower and an upper cell voltage input. Specifically, VLDO1 has inputs from V1 and V2 and VLDO2 has inputs from V3 and V4. It is important that the upper cell voltage connection always be connected first to the VLDO and the lower voltage second. This order of connection insures proper initialization of the VLDO circuit. A symptom of an improper connection sequence is the VLDO being out of regulation. The only way to restore VLDO regulation in this case is to remove power and apply the cell voltages in the correct order.

2.1.2 Cell Voltage and Temperature Measurement

The five cell connections are used by the bq78PL116 to measure each cell voltage. Cell 1 is measured between VSS and V1, cell 2 is measured between V1 and V2, cell three is measured between V2 and V3 and cell 4 is measured between V3 and V4. Any series impedance in these connections will contribute to cell voltage measurement inaccuracy in proportion to the device current on that input pin.

Temperature sensors can be connected to device pins XT1, XT2, XT3 and XT4. The cell voltages are used in the internal generation of the temperature measurements. Temperature measurements can also be effected by series impedance in the cell voltage connections.

2.1.3 PowerPump Control Pin Drive

The PowerPump control outputs are at pins P1N, P2S, P2N, P3S, P3N, P4S and P4N. The lower three outputs (P1N, P2S and P2N) are at cell 1 voltage level. The upper four outputs (P3S, P3N, P4S and P4N) are at the cell 3 voltage level. Any series impedance in these connections (VSS, V1, V2 and V3) will contribute to a reduction in the PowerPump gate drive current capability.

2.1.4 EUV Mode

EUV mode is determined by both firmware parameter settings and the inherent characteristics of the hardware. Entry into EUV mode puts the device in the lowest possible power consumption state.

In the case of firmware, the EUV Threshold setting (mV) and EUV Time (seconds) specifies when the microcontroller (firmware) should request to turn off all of the VLDOs in the system. The EUV Threshold setting is compared to all cell voltages in the system. If any cell is below this threshold for a time greater than the EUV Time setting, the microcontroller issues a shutdown request to the VLDOs. The request to shut down persists until all of the VLDOs shut down or all of the cell voltages go above $V_{STARTUP}$.

The firmware shutdown request is honored based on the status of the EUV Mode hardware circuit blocks connected to cells V1 and V3 and shown in Figure 3. If the cell input to the EUV Mode circuit is below 2.8V, then the shutdown request from the firmware will be honored by the VLDO associated with that EUV circuit. If the cell is above 2.8V, the VLDO associated with that cell will not honor the request to shut down. VLDO1 is associated with V1 and VLDO2 is associated with V3.

Since the EUV Mode hardware is based on independent cell voltages which can be at different levels, a case can happen where some VLDOs will shut down and other won't honor the shutdown command. The PowerLAN network will then fault because one or more nodes in the network are not operating. (A node is equivalent to a cell in the battery.) Symptoms of a PowerLAN fault are cell voltages reporting back as 2000mV and the Number of Poll Errors steadily increasing.

The exit from EUV and return to normal or standby mode is strictly governed by the hardware characteristic called $V_{STARTUP}$. This parameter has a minimum value of 2.9V. This means that the bq78PL116 will not exit EUV mode until all cells are above 2.9V.

2.2 Power Up Sequence

The PowerLAN Master Gateway Controller should be connected to the cells in a specific sequence. The impetus behind this connection order is achievement of a stable power up of the VLDOs in the system. For this reason, VLDO ground should be connected first followed by the cell powering the VLDO second and then the cell under it third. This is detailed in the following Table 2.

Table 2. Connection order of PowerLAN Master Gateway Controller Cell Voltages

Battery Series Cell Count	Connection Order of PowerLAN Master Gateway Controller Pins				
	VSS	V1	V2	V3	V4
3S	1	3	2	4	4
4S	1	3	2	5	4

In the 3S application, pins V3 and V4 can be connected simultaneously because they are shorted together on the circuit board.

WARNING:
Connecting the cell voltages in an order other than the one listed in Table 2 can cause the PowerLAN Master Gateway Controller to not operate properly.

2.2.1 Power Up Method

One possible method to achieve this connection sequence is to employ a two step connection. This involves first terminating the cell connections into a five position plug that can be mated in a random sequence to a set of electrically isolated cell voltage nets on a PCB. Then these isolated nets can be connected to the rest of the circuit through four solder bridges on the PCB. The following Figure 4 shows the arrangement. Battery connections (B+ and B-) are not shown.

The solder bridges are used to link four of the five pins of the header to the device pins V1, V2, V3 and V4. Then each solder bridge is made in the required order V2, V1, V4 and V3. The VSS device pin does not need a solder bridge because it is always connected first.

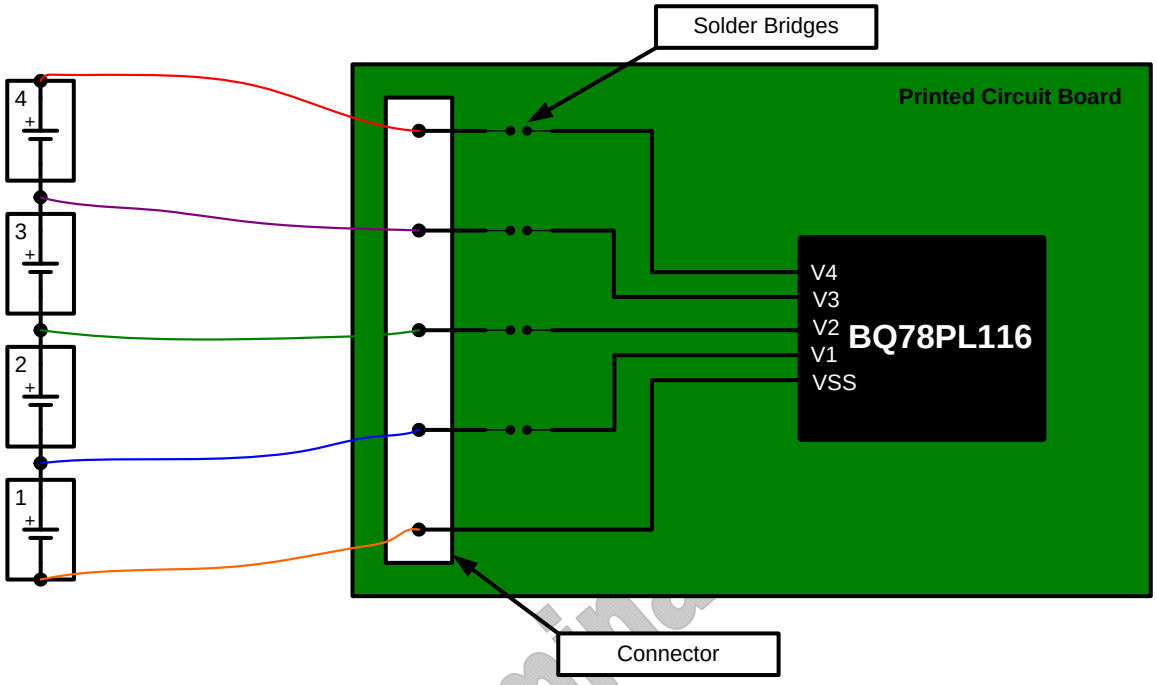

Figure 4. Cell Connection Method

2.2.2 Wired Command

The default setting for the bq78PL116 is un-wired. This means that a bit in the Algorithm Enable Register called the Wired Bit is cleared. The status of Wired or Un-Wired refers to the whether or not the cells are connected, or wired, to the PowerLAN Gateway Controller.

After all of the cells are properly connected to the bq78PL116 and communication is established with the device on the SMBus, the wired bit should be set. This puts the bq78PL116 into a level of operation that allows PowerPump to be turned on and Flash memory to be changed. There is a dedicated command called Toggle the Wired Bit that allows the Wired Bit to be set/cleared.

2.3 Battery Systems with More than Four Series Cells

The PowerLAN Master Gateway Controller can build a battery management system for up to sixteen cells if an appropriate number of bq76PL102 PowerLAN Dual Cell Monitors are added (1 to 6). Each bq76PL102 enables the addition of one or two series cells. The aforementioned rules that govern the power up sequence of the bq78PL116 also apply to the bq76PL102.

The first four cells are always connected to the bq78PL116 in 4S to 16S packs. The bq76PL102 are then connected to cells 5 to 16 in order. For instance, the first bq76PL102 is connected to cells 5 and 6.

2.3.1 Power Up Sequence for bq76PL102

The bq76PL102 has three cell connections: VSS, V1 and V2. Just like the bq78PL116, the connection sequence for the bq76PL102 is VSS, V2 and then V1. Figure 5 shows the internal diagram of the bq76PL102. It is identical to the lower section of the bq78PL116. One at a time the bq76PL102s in the system are connected to its cells after the bq78PL116 has been connected to its cells.

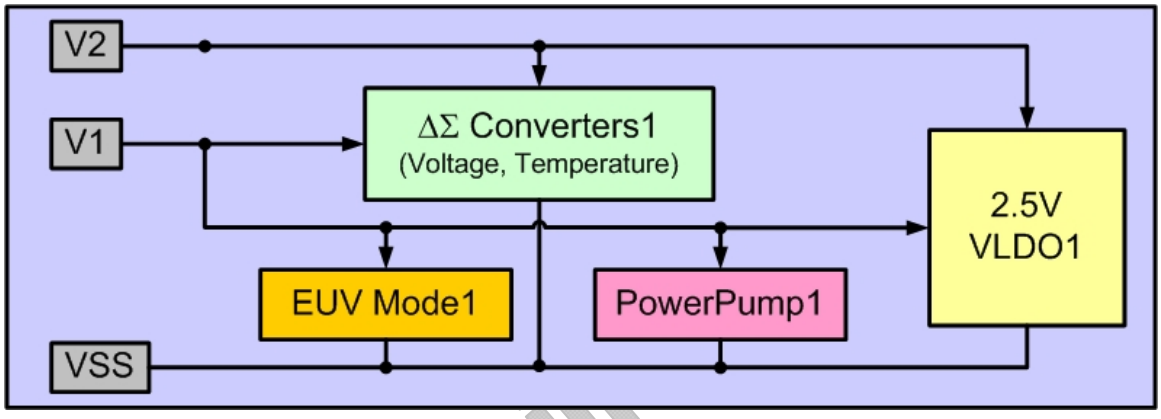

Figure 5. bq76PL102 Cell Connection and Internal Circuits

2.3.2 Power Up Method with bq76PL102

Figure 6 is an 8S system. It is very similar to Figure 4 which shows a 4S system. The power up method utilizes the sample "bulk" cell connector and then individual solder bridges to establish the cell connection sequence.

This connection principle should be applied to the other system sizes (5S, 6S, 7S, 9S, etc)

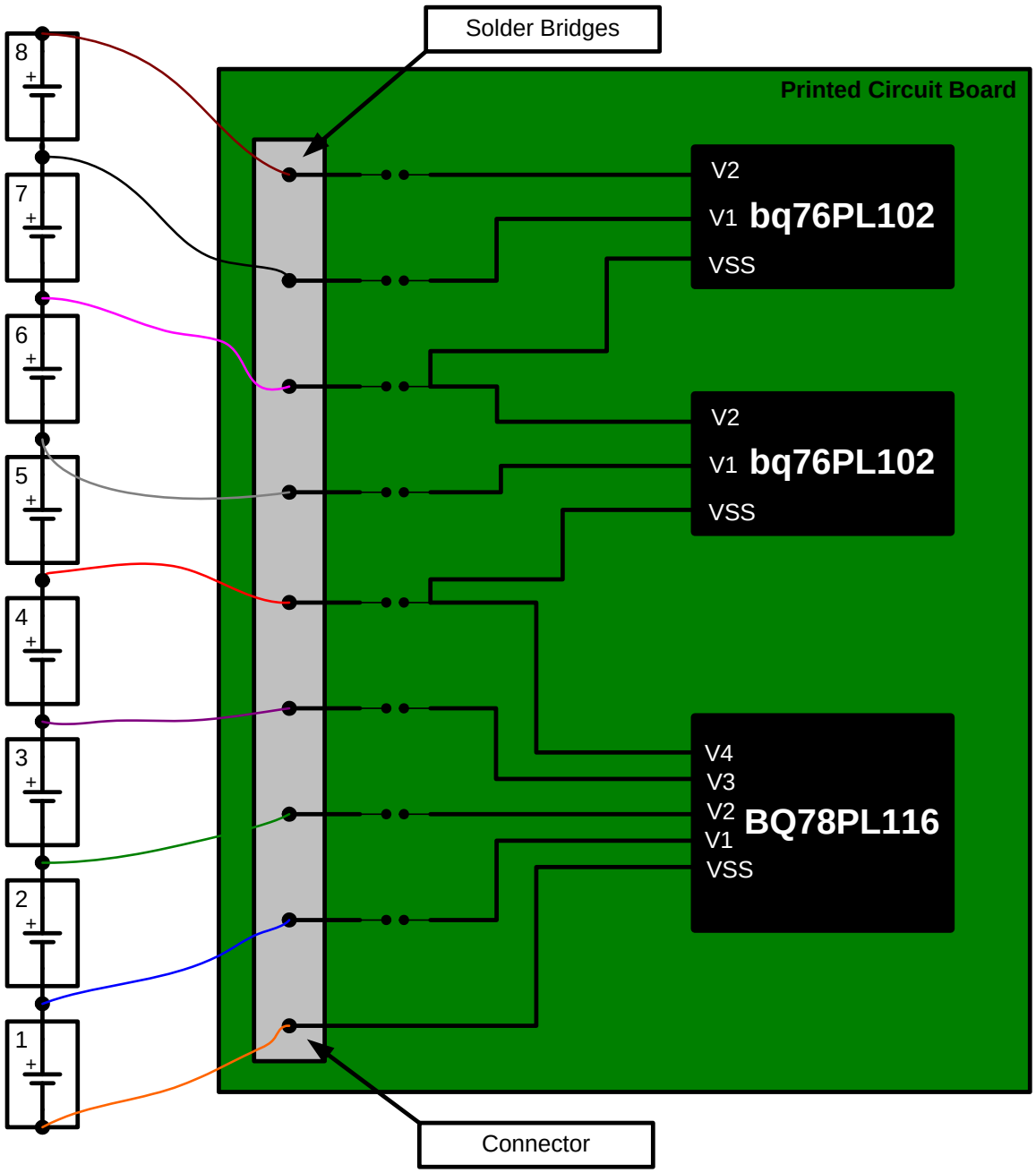

Figure 6. Cell Connection Method

2.4 Power Down Sequence

PowerLAN Master Gateway Controller systems are typically connected to the cells once in the lifetime of the battery pack so a disconnect sequence is not usually needed. However, disconnection is likely needed during the prototyping, production rework or repair processes.

There are two reasons to have a disconnection sequence: (1) Protection against interruptions of writes to flash memory and (2) Protection against instability in the PowerPump circuit.

Interruption of power during a flash write could cause memory corruption.

The PowerPump circuit operates in a safe, open loop mode. The presence of the low impedance cells as well as a less than 50% duty cycle on the control signal prevent the circuit from becoming unstable or going into a continuous current mode. If the cells were disconnected while PowerPump was running, the current in a charged up inductor would have no place to send its energy. This would result in the inductor voltage going to a level that would exceed the Abs. Max. rating of the cell inputs for the bq78PL116.

2.4.1 Power Down Method

There is a command called Safe Disconnect that permits safe cell (power) disconnection. The cell connections can be randomly removed after this command is issued. In the example shown in Figure 4 the single cell connector could be removed to power down the bq78PL116. The separate battery connections would also have to be removed to fully power down the circuit.