bq20z655 Changes vs bq20z65-R1

Overview

The bq20z655 is a firmware feature change compared to the bq20z65-R1 utilizing the same hardware platform. The bq20z655 offers additional LCD display option and charge enable features.

LCD Display Support

The bq20z655 can be configured to support one of two display modes. LED display or LCD display. The related display pins are:

Pin #	Name	Description
27	LED5/SEG5	Output / open drain: LED 5 current sink. LCD segment 5.
26	LED4/SEG4	Output / open drain: LED 4 current sink. LCD segment 4.
25	LED3/SEG3	Output / open drain: LED 3 current sink. LCD segment 3.
24	LED2/SEG2	Output / open drain: LED 2 current sink. LCD segment 2.
23	LED1/SEG1	Output / open drain: LED 1 current sink. LCD segment 1.
12	COM/TP	Output / open drain: LCD common connection
21	DISP	Input: In LED mode this is the display enable input.

The LED display functions differs slightly from the bq20z65-R1 when in a PF state. When the bq20z655 is in the PF state then the LED display always indicates the PF display when activated. It doesn't activate the display of SOC/RSOC first.
The bq20z65-R1 configuration bits [PFD0], [PFD1] in operation Cfg B are no longer used and are changed to [RSVD] in bq20z655.

The LCD display function is activated all the time during operation except shutdown. The LCD refresh frequency is configurable through data flash.

The related data flash:

LED Support → LCD Freq: default is 35 Hz. From 20 to 100 Hz
Configuration→Operation Cfg C: bits [DSPLY1],[DSPLY0] to configure the display mode.
When [DSPLY1]=0, [DSPLY0]=0, it supports LED display.
When [DSPLY1]=0, [DSPLY0]=1, it supports LCD display. Default is to support LED.

Charge Enable(CE) pin

The new Charge Enable (CE) pin is configured as an input. A logic high on this pin only affects the normal operation on the charge FET when the battery is in charge/relax mode (*OperationStatus( ) [DSG]* = 0).

If the battery is in charge mode and the charge current is less than the Chg Inhibit Threshold, the charge FET still works as normal. When the charge current exceeds the Chg Inhibit Threshold for Chg Inhibit Hold Time, the charge FET will be turned off if the CE pin is HIGH. The charge FET does not turn back again unless the CE pin changes to logic LOW or battery changes to discharge mode or the CE function is disabled.

The CE function is disabled once the Chg Inhibit Threshold is set to 0.

The related data flash:

Charge Control → External Charge Control
Chg Inhibit Threshold: default is 0 mA. From 0 ~ 20000mA.
Chg Inhibit Hold Time: default is 0 sec. From 0 ~ 240 sec.