DDR VTT Termination LDOs

How Much Power do I Need for DDR?

VDDQ

- In Datasheet
  - Datasheets list IDDQ for every mode
    - Not all IC/DIMMS in highest current mode at once
  - Typical estimate highest IDDQ mode for 1 IC/DIMM + 50% for each additional IC/DIMM
  - Given in “No Load” condition
    - Does not include VTT current
  - Must Source VTT current to output Logic 1s
    - Increase by VTT current for I/O when Output All 1s.
  - $IDDQ_{MAX} = IDDQ_{(datasheet)} + VTT_{MAX}$

VTT

- **Typically NOT given in datasheet**
- Depends on Address & Data lines

$$ITT_{MAX} = \#bits\left(VTT / R_{TERM}\right)$$

  - DDR
    - Can be as high as 20mA / data/address bit channel
  - DDR2
    - Can be as high as 18mA / data/address bit
  - DDR3
    - Can be as high as 15mA / data/address bit
- Can have up to 2x start-up current due to Active Termination / Capacitive Load

DDR Memory Active Bus Termination

Part Number	Topology	Vin (V)	Iout (A)	Provides	DDR
PTH03010/50/60 PTH05010/50/60 PTH12010/50/60	Plug-In Module	2.95 to 3.65	6,10,15	VTT	1, 2, 3
		4.5 to 5.5	6,10,15	VTT	1, 2, 3
		10.8 to 13.2	6,10,12	VTT	1, 2, 3
TPS40042 TPS40056 TPS51116 TPS51020	Controller	2.25 to 5.5	Up to 15	VTT	1, 2, 3
		8 to 40	Up to 20	VTT	1, 2, 3
	Controller + LDO	3 to 28[1]	Up to 15, 3	VTT, VDDQ, VREF	1, 2, 3
	Dual Controller	4.5 to 28	Up to 15, 15	VTT, VDDQ, VREF	1, 2
TPS51100 TPS51200 TPS51206	LDO	1.2 to 3.6[2]	Up to 3	VTT, VREF	1, 2, 3
		1.1 to 3.5[3] VTT + 0.4V to 3.5V[4]	Up to 2	VTT, VREF	1, 2, 3 4
TPS54372 TPS54672 TPS54972	Switcher with integrated FETs SWIFT	3 to 6	3	VTT	1, 2, 3
		3 to 6	6	VTT	1, 2, 3
		3 to 4	9	VTT	1, 2, 3

1) Needs 4.5 to 5.5V bias
2) Needs 4.75 to 5.25V bias
3) Needs 2.4 to 3.5V bias
4) Needs 3.3V or 5V bias

TPS51100

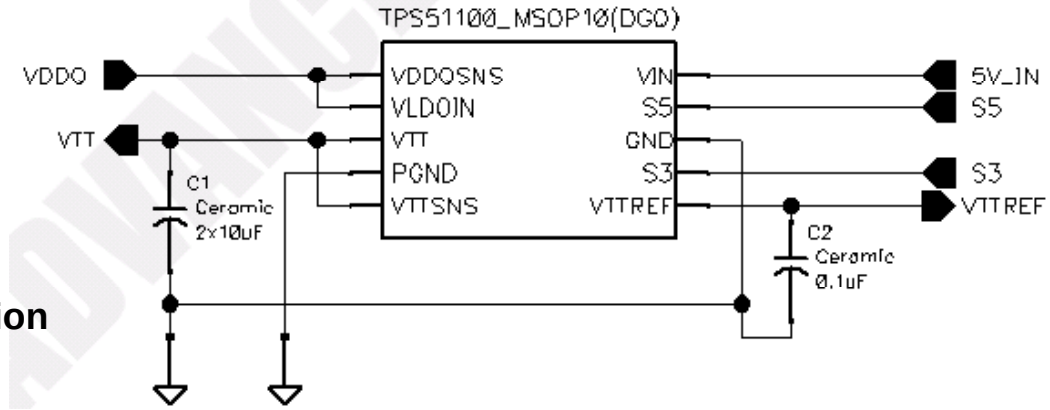
3A Sink/Source Termination Regulator

Features

- Input Voltage Range: 4.75V to 5.25V
- VLDOIN Voltage Range: 1.2V to 3.6V
- 3A Sink/Source Termination Regulator includes Droop Compensation
- Requires only 20uF Ceramic Output Capacitance
- Supports High-Z in S3 and Soft-Off in S5
- Supports 1.2V Input (VLDOIN) helps Reduce total Power Dissipation
- Integrated Resistor Divider Tracks ½ VDDQSNS for VTT and VTTREF
- Remote Sensing available (VTTSNS)
- +/-20mV Accuracy for VTT and VTTREF

Features

- 10mA Buffered Reference (VTTREF)
- Built in Soft Start, UVLO and OCL
- Thermal Shutdown
- Supports JEDEC specification
- Thermally Efficient 10 Pin MSOP POWERPAD Package



Applications

- DDR / DDR II / DDRIII Memory Termination
- SSTL-2, SSTL-3, HSTL Termination

EVM

TPS51100EVM-001

Texas Instruments

TPS51200

3A Source-Sink DDR Termination Regulator

Features

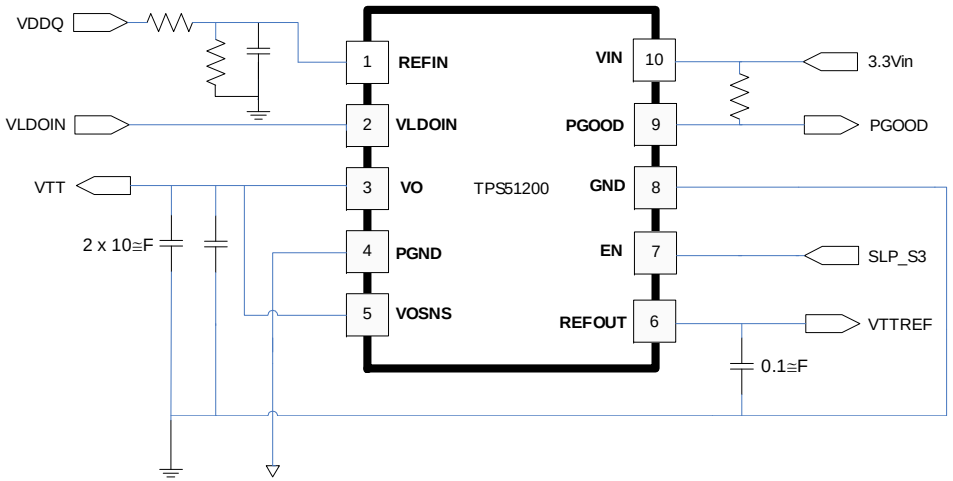
- Requires only 20uF of ceramic output capacitance
- Direct interface to S3 and sensing of S5 control signals
- Supports high-Z in S3 and soft-off in S5
- LDO input can be reduced to 1.2V
- SS, UVLO, OCL and thermal shutdown
- Enable input and Power Good output
- 10-pin SON package

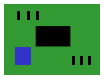
Benefits

- Lower cost and size than competing parts requiring 600uF or more of electrolytic capacitance
- Ease of use
- Fewer external components and lower cost
- Lower power dissipation
- System protection
- Controlled turn-on and monitored output regulation
- Enables small form factor designs

Applications

- DDR, DDR2, DDR3, and low-power DDR3/DDR4 VTT Memory Termination
- Graphics Processors
- Core Supplies
- Chipset/RAM supplies as low as 0.5V

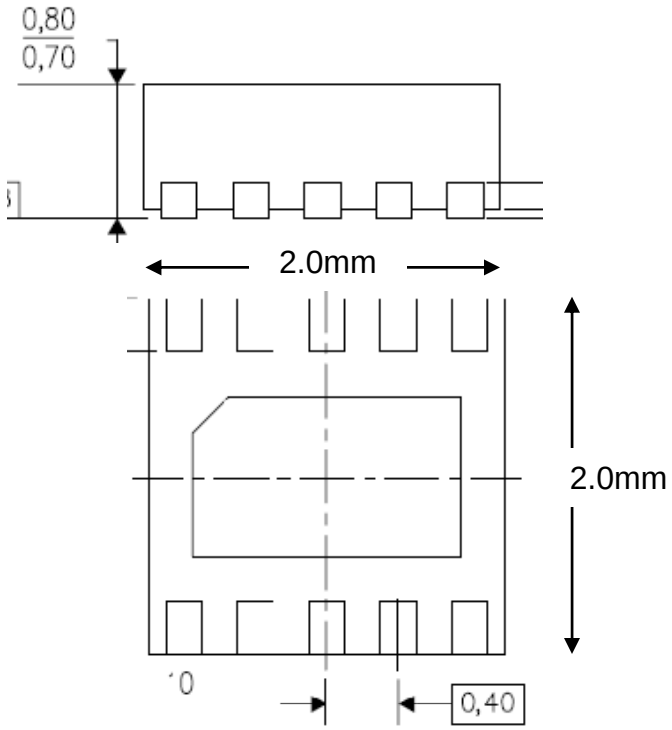




TPS51206 – new, smaller, cost-optimized DDT termination LDO

VTT / VTTREF

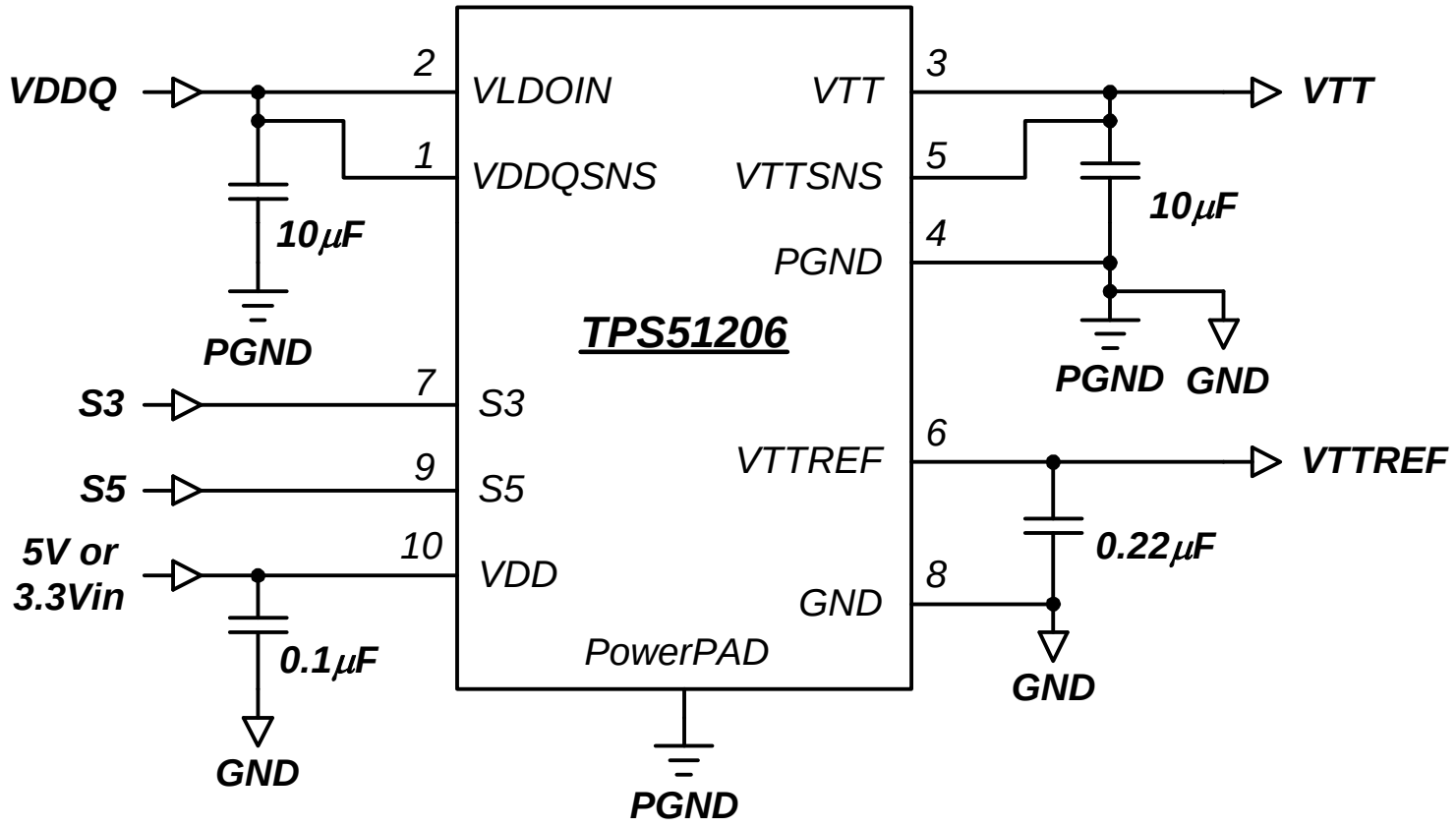
- **1A DC, 2A peak sink/source VTT LDO**
- **10mA buffered VTTREF LDO**
- **1x10uF VTT output capacitance (50% reduction of VTT Cap footprint & cost)**
- **2.0x2.0mm SON Package (73% reduction of IC footprint vs. TPS51100)**
- **Supports high-Z in S3, soft-off in S4/S5**
- **Supports 5V and 3.3V VDD**



STATE	S3	S5	VTTREF	VTT
S0	H	H	ON	ON
S3	L	H	ON	OFF (high-Z)
S4/S5	L	L	OFF (discharge)	OFF (discharge)

➢ ***Samples Now***
➢ ***RTM 02/28/11***

Schematic



TPS51206 App Circuit

Features

VTT / VTTREF

- 1A TDC, 2A peak sink/source VTT LDO
- 10mA buffered VTTREF LDO
- Supports high-Z in S3, soft-off discharge in S4/S5
- 1x10uF VTT output capacitance
- Supports 5V and 3.3V Vdd
- 2.0x2.0mm SON Package
- Pin Integrity with TPS51100

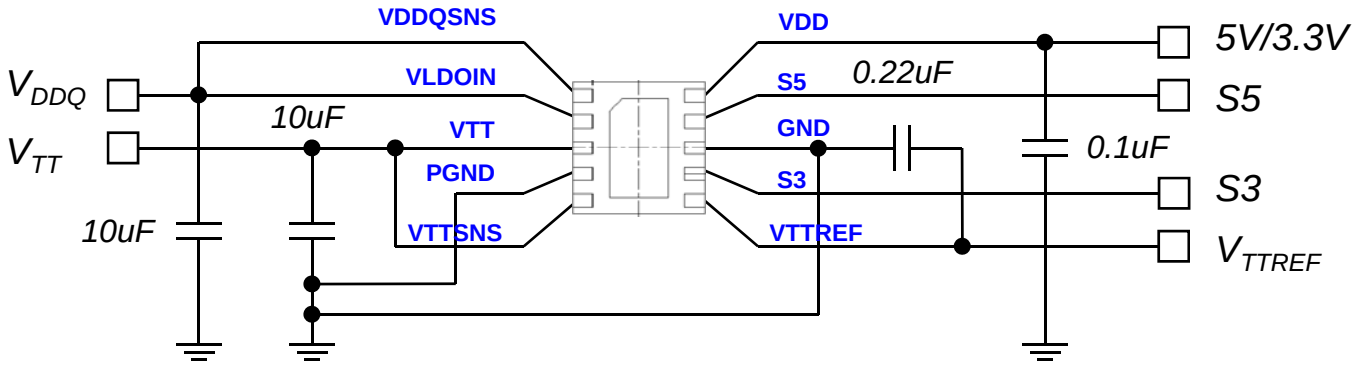
Benefits

VTT / VTTREF

- Compact solution size
- Support DDR2, DDR3, LPDDR3
- 50% reduction of VTT Cap footprint & cost
- Flexible for many platforms
- 73% reduction of IC footprint vs. TPS51100

SON10 (DSQ)

2.0x2.0mm^{2}x H:0.8mm

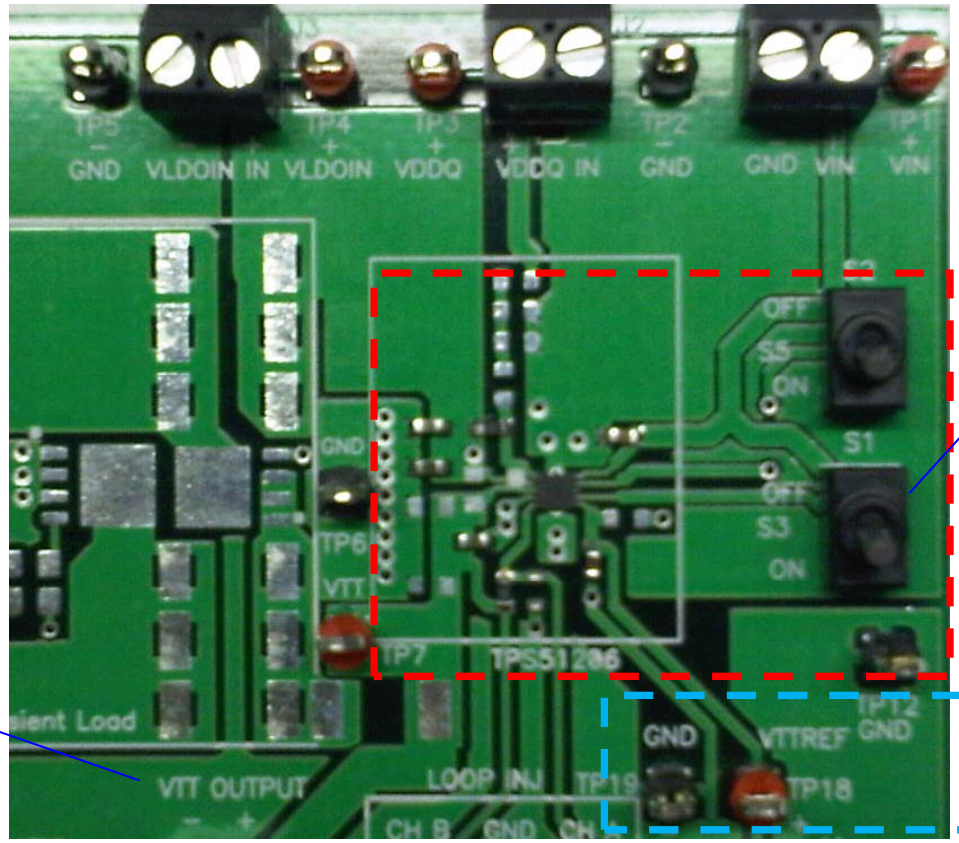


STATE	S3	S5	VTTREF	VTT
S0	H	H	ON	ON
S3	L	H	ON	OFF (high-Z)
S4/S5	L	L	OFF (discharge)	OFF (discharge)

TPS51206 EVM - New DDR2/3/3L +/-2A VTT Solution

Features

- Complete DDR2/DDR3/LVDDR3 VTT (termination) evaluation platform
- VIN, VLDOIN, VDDQ IN, VOUT connections and all DDR VTT-relevant test points



VTT

S1, S2, S3, S5 state test switches

VTT Transient Load Testing

VTTREF