

# THE LOAD DUMP

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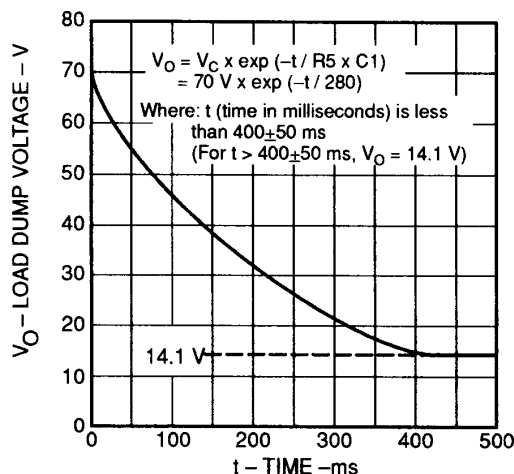
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## ABSTRACT

*Recently the Load-Dump transient condition has been receiving more attention. This paper discusses testing and design issues associated with manufacturing semiconductor devices which are required to withstand various load dump specifications.*

## INTRODUCTION

Load Dump is a condition observed in automobiles when the battery is disconnected from the rest of the power supply circuit while the alternator is generating, as shown in Figure 1. The voltage output from the alternator can then rise to as high as 120 V (depending upon the alternator's speed, excitation current and load current) then decay over a period of several hundred milliseconds. A typical waveform is shown in figure 1.



**Figure 1: Typical Load Dump Waveform**  
(Equation refers to test circuit shown in figure 5).

Only a few years ago the automotive load dump condition was not considered important in the design of most integrated circuits. When protection was first required this was often

quoted to be as low as 40 V, with an external transient protection device (metal oxide varistor, surge voltage protector or transient absorption zener) to absorb energy over 40 V, as described in ref 1. The International Standards Organization (ISO) and other specifications of only two or three years ago suggest load dump protection to around 50 V, but by degrees, this limit has increased and is now routinely quoted at almost 100 V.

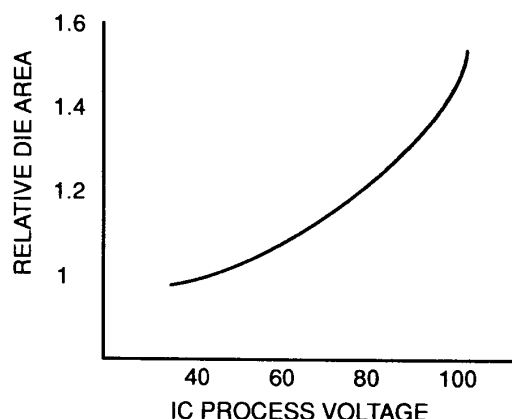
Automotive manufacturers are requesting these increases because, as the load dump voltage which must be sustained by the IC increases, the external protection device can be dispensed with or can be replaced by one of much lower energy rating and higher voltage.

A further factor which causes device design problems is the non-standard test configurations which vary between customers. This leads to many designs having to support virtually DC conditions to the load dump voltage maximum, not just the transient load dump specification itself.

Semiconductor manufacturers have answered the request for higher voltage load dump specifications in several ways, including the incorporation of external resistors or other series element to limit the transient current or some form of internal IC protection and controlled internal IC breakdown, or most often the use of higher voltage IC processes.

However, the increase in IC voltage capability and protection generally requires an increase in integrated circuit die size to achieve this additional protection. The increase has been minimized by continuing improvements in technology. This, together with cost reductions through manufacturing optimizations and circuitry developments, have hidden the real cost of the trend. Figure 2 shows the relative die size of a 5 A high side driver, with increasing load dump requirement. The die area may typically be nearly 50% larger for a 100 V IC process, than for a 40 V process. This in turn would convert to a 20 to 30% packaged device cost penalty to the customer. In

reality, it is unlikely that the automotive market would accept a return to the 40 V specification of load-dump, but a 60 V to 70 V specification would in the majority of cases be acceptable. This would still provide substantial cost savings on the higher voltage alternatives and permit IC designers to use the more recently developed IC processes rather than the very early and often inefficient 30 to 50 V Power IC technologies.



**Figure 2: Relative die size for 40 to 100V processes.**

There has been very little discussion in the technical literature of the load dump specification, and that which there is has normally been considered with other types of voltage transient. Although the load dump has been described and understood for many years (ref 2,3), it has only been relatively recently that more attention has been given to the condition, as the increasing level of electronics in automobiles has led to a desire for self-protection of IC's, rather than the use of external protection circuitry.

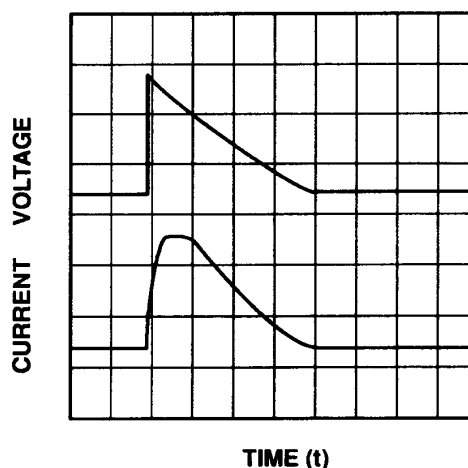
### CIRCUIT TECHNIQUES

Simple survivability is not the only requirement of an IC enduring load dump transients. Peripheral IC's, and components connected to the IC experiencing load dump transients, must also survive. For instance, high voltage load dump transients must be decoupled from low voltage logic signals. Power output transistors are often specified to stay OFF (high impedance) or turn OFF independent of external logic input signals.

All necessary load dump I/O characteristics can be achieved with minimal circuit design effort if a rugged, very high voltage process is used. Unfortunately, this process choice sacrifices IC performance and unduly increases die area and cost. To allow

the use of a lower voltage and higher performance process, simple circuit techniques may be employed without significantly increasing die area and cost.

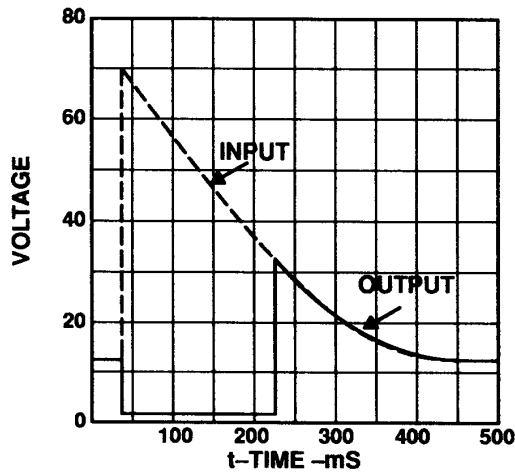
To prevent destruction of an IC, output transistors must operate within their safe operating area (SOA). Power transistors conducting during a load dump transient may operate in regions outside the SOA curve, resulting in destruction. Inductive output impedances may improve load dump performance by "filtering" the current transient, preventing simultaneous high current and high voltage conditions figure 3. If the power output transistor does not have adequate SOA capability for its range of output impedances, an over-voltage shutdown circuit may be employed. This turns-off the output transistor during the transient ensuring it remains within the SOA characteristic, figure 4.



**Figure 3: Current and Voltage waveforms for a high-side driver automotive switch subject to load dump.**

Regardless of SOA, transistor and component breakdown is usually not tolerated in an IC undergoing load dump transients. Components in a breakdown condition often inject holes and electrons into the isolating silicon substrate, causing SCR latching which may destroy the IC. Circuit techniques are therefore used to prevent breakdown by placing susceptible transistors in a CER or CES mode during the transient. To achieve this CER/CES mode, an over-voltage sense circuit may trigger components which shunt a low impedance across the base-emitter junction of the HV transistors. Another circuit approach used to gain load dump performance is to use an internally regulated voltage rail, protecting most of the circuit components from the load dump transient. Such techniques allow designers to use the lowest voltage and highest performance process possible. Although the added circuitry

consumes die area, much more area would be consumed by simply designing in a higher voltage process.



**Figure 4: Output over-voltage shutdown implementation for a high-side driver configuration, showing turn-off of the output device for excessive voltage transients.**

## **PROPOSED TEST METHOD FOR ALTERNATOR LOAD DUMP**

### **Measurement Philosophy**

The alternator load dump transient occurs infrequently, but it can occur suddenly and repetitively in certain vehicles, and under specific conditions. Most commonly this occurs as the result of a loose or corroded battery contact, which causes the battery loading to be suddenly removed from the charging circuit or disconnection of a jumper battery from a vehicle with a dead battery. In either case a large positive voltage propagates throughout the vehicle electrical system, which can have catastrophic consequences on devices not designed to withstand such transients, and not protected by nearby external voltage clamping components.

The vehicle effects of alternator load dump depend on the impedance of the electrical system at the moment the transient occurs, the electrical location of the components relative to the alternator, and the characteristics of the components and their operating temperatures.

The intent of this test is to provide a standard means of simulating non-repetitive transients in order to verify that a

given component will survive a certain known transient level or to determine the susceptibility of the component to failure.

### **Apparatus requirements**

a. One-shot pulse generator capable of delivering a 70 V positive voltage pulse with an exponential decay extending over a time period of  $400 \pm 50$  mS, across a resistive load of 7 Ohms. A schematic diagram for such a pulse generator is shown in figure 5. Some environments may require higher voltages and/or longer durations.

b. DC voltmeter and a digital storage oscilloscope for monitoring the power source and pulse generator.

c. Equipment as may be required to perform a functional test of the component following transient application.

### **Test Setup and Procedure**

a. Connect a known functional device—under-test as shown in figure 5.

b. Ensure that the ambient temperature and supply  $V_s$  are maintained as required by the appropriate test specification,  $V_s = 14.8$  V recommended.

c. Set up the pulse-generator to provide the polarity, amplitude and pulse duration as specified in the appropriate test specification,  $V_c = 72$  V recommended.

d. Generate the test pulse with switch S2 open, see figure 1.

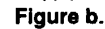
e. Close switch S2 and perform 10 load dumps, at 10 second intervals to determine whether failure has occurred and record results. This requires cycling of S2 open and closed.

f. Repeat steps (a) through (e) for additional devices of the same test components until the statistical requirements of the test specification have been met.

### **PRACTICAL TEST CONSIDERATIONS**

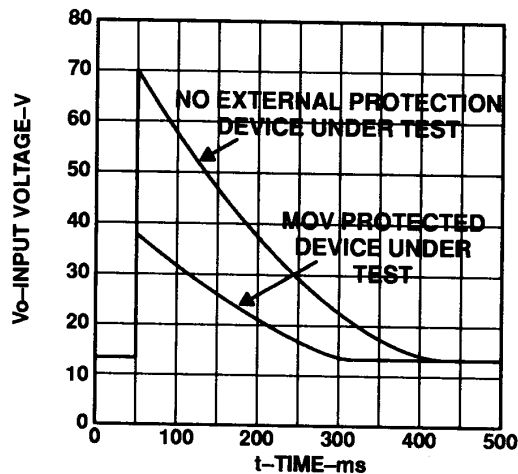
Caution should be taken during the initial test set-up because of possible destructive transients induced by the test circuitry. The following example is cited. When examining the characteristic on a 450 ms time scale during setup, transient spikes occurring from test components and layout may not be seen. Figure 6a exhibits a response characteristic of an under damped circuit with a very large over-shoot associated with the turn-off time. This transient occurs in approximately  $2-3 \mu\text{sec}$ . The ringing effect is likely caused by the stray series and

loading ( $3.3 \mu\text{F}$ ) was added across test point  $V_O$  of the tester (figure 5) relieving the circuit of the under damped condition and yielding a smooth transitional rise time, figure 6b.



**Figure 6: Load dump waveform (a) illustrating an overshoot condition and (b) showing dumping with small capacitor.**

External components between the tester and DUT existing in the actual application circuit should be specified in the application specification. A complete understanding of the application and external circuitry loading on the device is crucial to the integrity and reliability of the test set up. For example, one application may have an external capacitor to hold off fast voltage transients; another may have a zener or MOV for over-voltage protection schemes. An example of MOV protection is shown in figure 7.

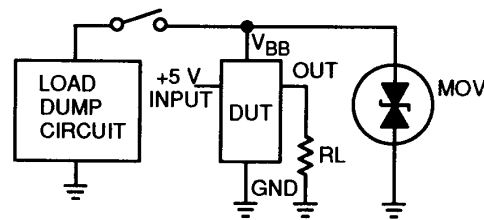


**Figure 7: Load-dump voltages with and without external protection.**

Another problem occurring at test time is understanding the state of the device during testing, for example: Is the device on or off during the test? Does the device have the load attached during test? What are the worst case load-dump conditions? Should the load dump test be performed over temperature? Are there any status conditions that have to be met during load dump? etc. These are questions that should be answered in the application specification, otherwise; again the testing may give spurious results. See figure 8 for three common circuit configurations of device under test during load dump test. Figure 4 shows a high-side driver being subjected to load dump while the output is on. The device's internal over-voltage protection is shown to activate, turning the load off for the duration of the transient.

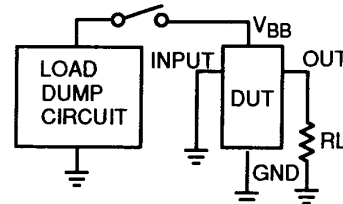
Taking the testing at various temperatures as an example, consider the following scenario. Assume a load dump characteristic of the device under test having internal voltage shutdown protection as shown in figure 4 (the device input is ON). Additional heat is generated in the device between the settling point back to 14 volts and over-voltage protection

point. At high temperature after 1 or 2 load dump pulse there is very likely to be enough heat generated to send the device into thermal shut down (the device input is OFF). Once in thermal shutdown the remainder of the pulses would only test the governing breakdown mechanism of the circuit since the device would not pass any current. In this case is the test valid?; is it the worst case? Probably not. It would appear that a test set-up at room temperature where the device could not go into thermal shutdown would be the worst case condition. In this situation the device would have to dissipate the greatest combination of both thermal and electrically generated power. In the actual application the device may be mounted on a large heat sink which effectively reduces the heat dissipation problem. The application must therefore be well understood to ensure reliable testing.



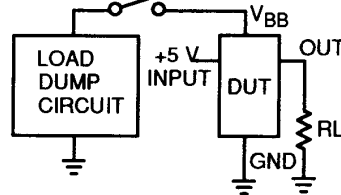
**Figure 8a**

**EXTERNAL MOV PROTECTED DUT WITHOUT CONDUCTING RATED LOAD**



**Figure 8b**

**NO EXTERNAL PROTECTION WITH DUT TURNED -OFF**



**Figure 8c**

**NO EXTERNAL PROTECTION WITH DUT TURNED -ON**

**Figure 8: Common circuit configuration of device under test during Load Dump test**

## **SUMMARY**

This paper has considered the history of the load dump transient. The trend towards higher load dump specifications has led to increased complexity of IC design and more costly devices, a trend hidden by technology improvements. A load dump test standard has been proposed, which aims at an optimization of the automotive manufacturer's requirements and the IC manufacturer's process technology, to give the best protection at a limited cost per device. Example applications have been described which emphasize the need to completely understand the application so that the load dump test is reliable and meaningful.

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