# Changes/Enhancements

| | UCD90120A | UCD90120 |
|---|---|---|
| Errata | - Most UCD90120 Errata fixed | |
| Sequencing | - Added Sequence Off dependencies<br>- Max time between Re-sequences is 32s<br>- Power Good state of rail is only dependent upon voltage | - Rails only sequenced off based on time<br>- Max time between re-sequences is ~1s<br>- Power good depended on voltage and state of EN pin for that rail |
| Shutdown Slaves Behavior | - Shutdown Slaves always shut down “with delay” meaning that they will always be shut down based on their sequence off dependencies and any delay time added | - Shutdown slaves were shut down either immediately or with delay according to the fault response of the faulty rail |
| Voltage Margining and Trim | - Option to have PWM go Hi-Z when not margining<br>- Support for “active trim” – uses Vout Nominal as the target set point | When margining is turned off, the PWM changes duty cycle using Vout nominal as target set point and then continues to run at that fixed duty cycle |
| Error Logs | -TBD # of faults in Flash<br>- Ability to log GPI faults to Flash<br>- Ability to log WDT timeout to Flash | - Up to 18 faults in Flash |
| Logic Controlled GPOs | - 2 AND Paths feed to a gate that can be an OR or AND<br>- GPO can have a delay before changing state<br>- GPO can be fed as an internal GPI to another GPO | - 4 AND paths feed to an OR gate |
| Watchdog Timer | - WDI and WDO pins are now optional | - WDI and WDO pins must be configured even if you are using I2C to reset the WDT |
| System Reset | -Added use of GPIs as dependencies<br><br>-Option to re-assert RESET signal if any rails or GPIs go “power bad”<br><br>-Reset Signal can be a pulse with configurable pulse width | -System Reset signal only dependent upon rail power good status<br>-System RESET signal only released once after initial power up of dependent rails |