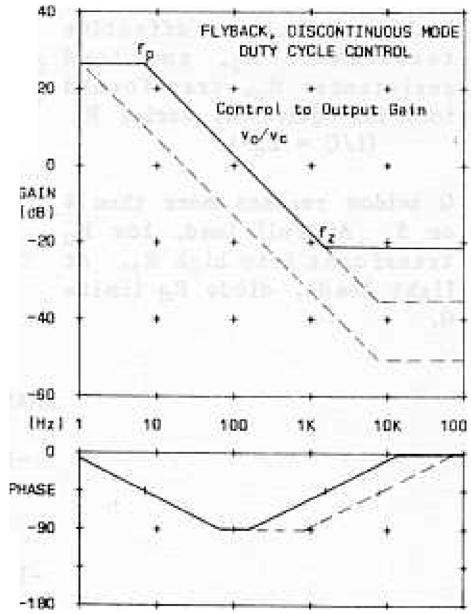
APPENDIX C

FLYBACK - DISCONTINUOUS INDUCTOR CURRENT - DIRECT DUTY CYCLE CONTROL



Example 1: 12 Volt, 60 Watt Output

f_s = 80 kHz, T = 12.5 μsec

V_{in} = 12 to 24 V

V_o = 12 V, I_o = 0.5 to 5 A

R_o = 24 to 2.4 Ohms

I_{sc} = 6 A Short Circuit Limit

Discontinuous Current Mode Boundary Duty Cycle Limit at I_{sc}, min V_{in}:

$D_{max} = 1/(1+V_{in}/V_o) = 0.5$

Max. $t_d = (1-D)T = 6.25$ μsec

Max. $I_p = 2I_{sc}/(1-D) = 2x6/0.5 = 24$ A

$L = (V_o+V_f)t_d/I_p = 13x6.25/24 = 3.4$ μH

ESR Max for 0.1 V_{pp} Ripple at I_o = 5A:

$R_c = 0.1/20A = 5$ mΩ max (1 mΩ min).

C = 20,000 μF

Basic Equations — Duty Cycle Control:

$D = V_c/V_s$:

DC Relationships:

(1) $V_o = V_{in}D\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} = V_{in}\frac{V_c}{V_s}\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}}$ (1a) $V_c = \frac{V_oV_s}{V_{in}}\left(\frac{2Lf}{R_o}\right)^{\frac{1}{2}}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{V_{in}}{V_s}\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} H_e(s)$. $H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p}$, $\omega_p = \frac{2}{R_oC}$, $\omega_z = \frac{1}{R_cC}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_c}{V_s}\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} H_e(s) = \frac{V_o}{V_{in}} H_e(s)$

Corner Frequencies from Equation (2):

$f_p = 2/(2\pi R_oC) = 15.92/R_o$ = 6.63 Hz at 2.4 Ω, .663 at 24 Ω

$f_z = 1/(2\pi R_cC) = 7.95/R_c$ = 1590 Hz at 5 mΩ, 7950 Hz at 1 mΩ

Low Frequency Gain from Equation (2) (V_s = 2.5 V for UC1524A)

$v_o/v_c = .542V_{in}\sqrt{R_o}$ = 20.2 (26.7 dB) at 24 V, 2.4 Ω

= 31.9 (30.1 dB) at 12 V, 24 Ω

V_c must be clamped to 1.25 V to limit Duty Cycle to 0.5 max.

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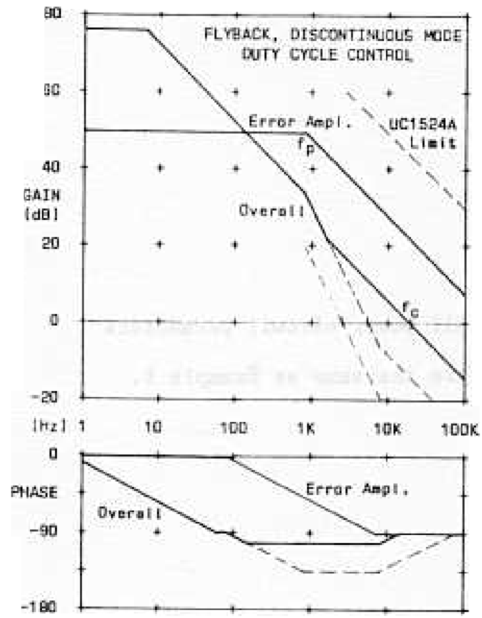


<u>Error Amplifier Compensation:</u>

Control I.C.: UC1524A

Crossover frequency (0 dB loop gain):

$f_c = f_s/4 = 20$ kHz

E/A gain needed at 20 kHz = 21.5 dB

ESR zero, f_z, cancelled by pole f_p at $\max f_z/10$. This increases low frequency gain and adds 45° more phase lag, still leaving a phase margin of 45°:

$f_p = \max f_z/10 = 795$ Hz

E/A gain required below f_p is:

$21.5 + 20\log(20{,}000/795) = 49.5$ dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_O with worst case line and load variation is (from Eq. 1a):

(1a) $V_C = \dfrac{V_O V_S}{V_{in}}\left(\dfrac{2Lf}{R_O}\right)^{\frac{1}{2}} = \dfrac{12x2.5\sqrt{3.4x.08}}{V_{in}\sqrt{R_O}}$ = 0.188 to 1.19 V. $\Delta V_C = 1.0$ V

Output voltage error with actual E/A DC gain of 298 (49.5 dB):

$\Delta V_O = \Delta V_c/298 = 3.4$ mV (120 mV = 1% regulation)

<u>Implementation:</u> Circuit of Appendix A-1 (omit R_p and C_p)

UC1524A has transconductance error amplifier (gm = .002)

With $R_f = 3M\Omega$, max. gain = $gmR_f = 6000$ (75.6 dB, > 64 dB required, OK)

Gain required below f_p = 298 (49.5 dB) = R_f/R_i.

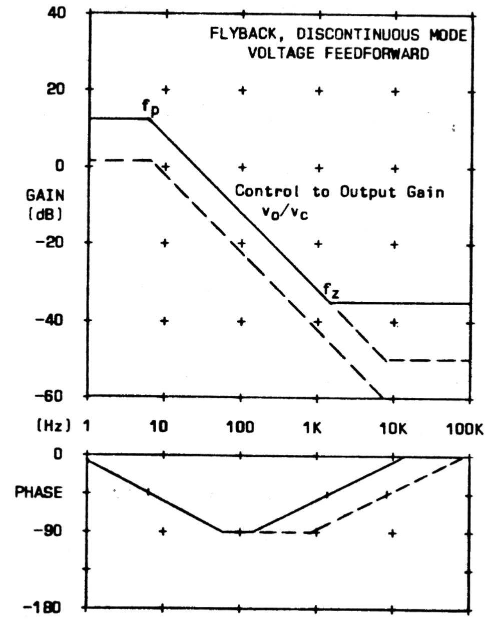
$R_i = 3M/298 = 10K$

Pole at 795 Hz:

$C_f = 1/(2\pi f_p R_f) = 67$ pF

Example 2: 12 Volt, 60 Watt Output

All power circuit parameters are the same as Example 1.



Basic Equations — Voltage Feedforward:

$D = V_c/V_s$, $V_s = V_{in}/K$, $K = V_{in}D/\max V_c$

DC Relationships:

(1) $V_o = V_{in}D\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} = KV_c\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}}$ (1a) $V_c = \frac{V_o}{K}\left(\frac{2Lf}{R_o}\right)^{\frac{1}{2}}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = K\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} H_e(s)$. $H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p}$, $\omega_p = \frac{2}{R_oC}$, $\omega_z = \frac{1}{R_cC}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = 0$ Inherent good line regulation and audio susceptibility.

Corner Frequencies from Equation (2):

$f_p = 2/(2\pi R_oC) = 15.92/R_o$ = 6.63 Hz at 2.4 Ω, .663 at 24 Ω

$f_z = 1/(2\pi R_cC) = 7.95/R_c$ = 1590 Hz at 5 mΩ, 7950 Hz at 1 mΩ

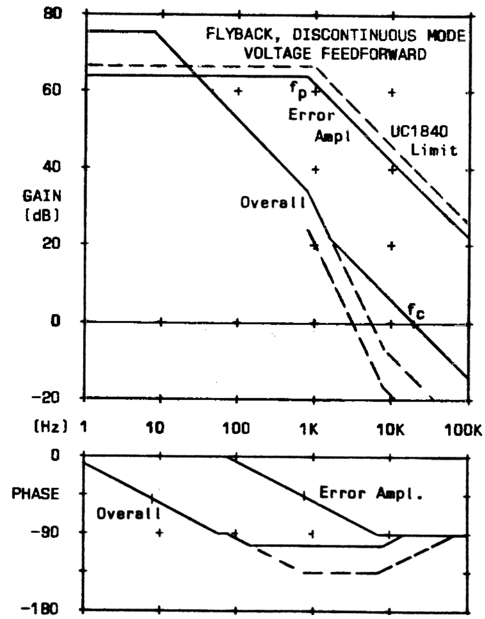
Low Frequency Gain from Equation (2) (max V_c = 3.5 V for UC1840)

$K = V_{in}D/\max V_c = 12\text{x}0.5/3.5 = 1.71$ (feedforward factor)

$v_o/v_c = 2.52\sqrt{R_o}$ = 3.91 (11.8 dB) at 2.4 Ω

= 12.35 (21.8 dB) at 24 Ω

V_{in} = 12 to 24 V



Error Amplifier Compensation:

Control I.C.: UC1840

Crossover frequency (0 dB loop gain)

$f_c = f_s/4 = 20$ kHz

E/A gain needed at 20 kHz = 35.8 dB

ESR zero, f_z, is cancelled by pole f_p at max $f_z/10$. This increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

$f_p = \max f_z/10 = 795$ Hz

E/A gain required below f_p is:

$35.8 + 20\log(20{,}000/795) = 63.8$ dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \frac{V_o}{K}\left(\frac{2Lf}{R_o}\right)^{\frac{1}{2}} = \frac{12\sqrt{2x3.4x.08}}{1.71\sqrt{R_o}}$ = 1.05 to 3.33 V. $\Delta V_c = 2.28$ V

Output voltage error with actual E/A DC gain of 1550 (63.8 dB):

$\Delta V_o = \Delta V_c/1550 = 1.5$ mV (120 mV = 1% regulation)

Implementation: Circuit of Appendix A-1 (omit R_p and C_p)

Voltage feedforward factor, K, in UC1840 is set by an independent ramp generator whose slope varies directly with V_{in}. A minimum ramp charging current of 36 µA is chosen (near the bottom end of the optimum range).

$R_r = \min V_{in}/\min I_r = 12/36\mu A = 330K$

$dv/dt = I_r/C_r = V_{in}/R_rC_r = \max v_c/t_{on}$. $R_rC_r = V_{in}t_{on}/\max V_c = K/f$

$C_r = K/fR_r = 1.71/(80K x 330K) = 65$ pF

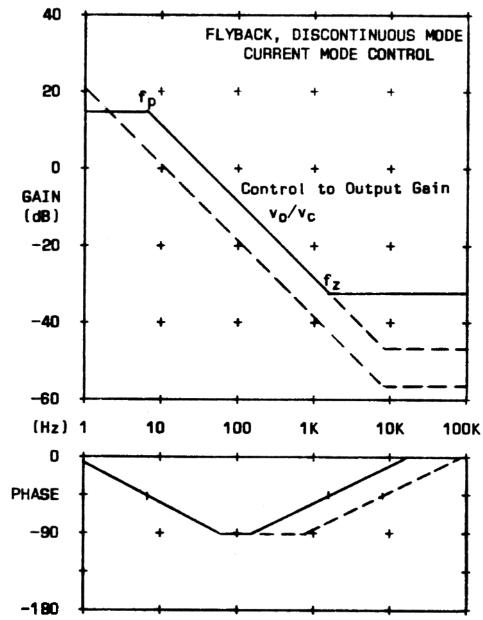
UC1840 has voltage mode amplifier with 65 dB gain, > 63.8 dB required, OK.

$R_f = 3M$, chosen somewhat arbitrarily because of high gain required.

Gain required below f_p = 1550 (64 dB) = R_f/R_i. $R_i = 3M/1550 = 2K$.

Pole at $f_p = 795$ Hz: $C_f = 1/(2\pi f_p R_f) = 67$ pF

Example 3: 12 Volt, 60 Watt Output



All power circuit parameters are the same as Example 1.

Basic Equations — Current Mode Control:

$I_p = KV_c$, $\quad K = \max I_p / \max V_c$

DC Relationships:

(1) $\quad V_o = V_{in} D \left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} = KV_c \sqrt{R_o L f / 2}$ $\qquad$ (1a) $\quad V_c = \frac{V_o \sqrt{2}}{K \sqrt{L f R_o}}$

Control to Output Gain:

(2) $\quad \frac{v_o}{v_c} = K \sqrt{R_o L f / 2}\; H_e(s)$. $\qquad H_e(s) = \frac{1 + s/\omega_z}{1 + s/\omega_p}$, $\quad \omega_p = \frac{2}{R_o C}$, $\quad \omega_z = \frac{1}{R_c C}$

Line to Output Gain:

(3) $\quad \frac{v_o}{v_{in}} = 0$ $\qquad$ Inherent good line regulation and audio susceptibility.

Corner Frequencies from Equation (2):

$f_p = 2/(2\pi R_o C) = 15.92/R_o \quad = 6.63$ Hz at 2.4 Ω, .663 at 24 Ω

$f_z = 1/(2\pi R_c C) = 7.95/R_c \quad = 1590$ Hz at 5 mΩ, 7950 Hz at 1 mΩ

Low Frequency Gain from Equation (2) $\quad$ (V_c clamped to 2.4 V for 24 A I_{sc})

$K = \max I_p / \max V_c = 24/2.4 = 10$

$v_o/v_c = 3.7\sqrt{R_o} \quad = 5.73$ (15.2 dB) at 2.4 Ω

$= 18.1$ (25.2 dB) at 24 Ω

$V_{in} = 12$ to 24 V

Error Amplifier Compensation:

Control I.C.: UC1846

Crossover frequency (0 dB loop gain)

$$f_c = f_s/4 = 20\ \text{kHz}$$

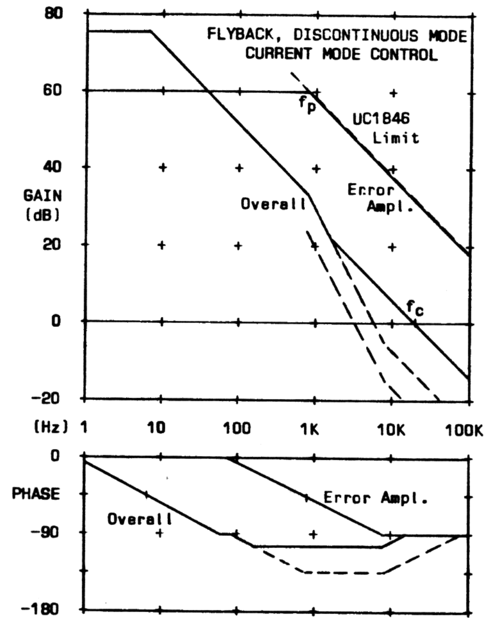
E/A gain needed at 20 kHz = 32 dB

ESR zero, f_z, is cancelled by pole f_p at max $f_z/10$. This decade offset increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

$$f_p = \max f_z/10 = 795\ \text{Hz}$$

E/A gain required at and below f_p is:

$$32 + 20\log(20{,}000/795) = 60\ \text{dB}$$



Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

$$\text{(1a)}\quad V_c = \frac{V_o\sqrt{2}}{K\sqrt{LfR_o}} = \frac{12\sqrt{2}}{10\sqrt{3.4x.08R_o}} = 3.25/\sqrt{R_o} = 0.664\ \text{to}\ 2.1\ \text{V}. \qquad \Delta V_c = 1.44\ \text{V}$$

Output voltage error with actual E/A DC gain of 1000 (60 dB):

$$\Delta V_o = \Delta V_c/1000 = 1.44\ \text{mV} \quad (120\ \text{mV} = 1\%\ \text{regulation})$$

Implementation: Circuit of Appendix A-1 (omit R_p and C_p)

Current control factor (K = 10) is set with the UC1846 by the fixed gain (3X) of the current amplifier and the current sampling resistor, R_s:

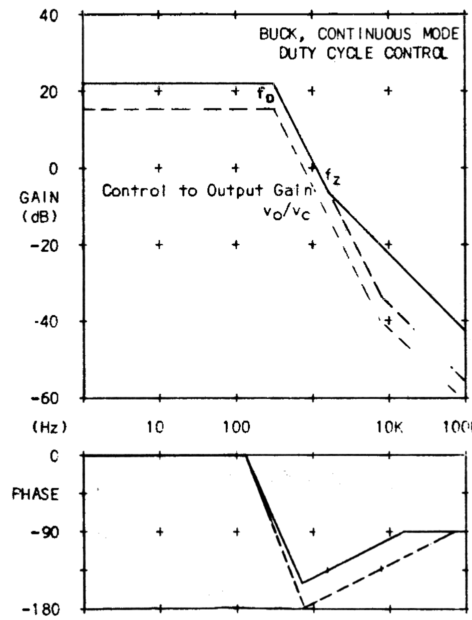
$$K = I_p/V_c = 10 = 1/(3R_s). \qquad R_s = 1/(30) = .033\ \Omega$$

UC1846 error amplifier gain limit >80 dB with R_f>30K, > 60 dB required, OK.

R_f = 3 M, chosen somewhat arbitrarily because of high gain required.

Gain required below f_p = 1000 (60 dB) = R_f/R_i. $\quad R_i$ = 3M/1000 = 3K.

Pole at f_p = 795 Hz: $\quad C_f = 1/(2\pi f_p R_f) = 67$ pF



Example 4: 12 Volt, 240 Watt Output

f_s = 40 kHz, T = 25 µsec

V_{in} = 30 to 60 V

V_o = 12 V, I_o = 2 to 20 A

R_o = 6 to 0.6 Ohms

I_{sc} = 24 A Short Circuit Limit

Continuous Current Mode Boundary:

Min. I_o = 2 A

Max. $\Delta I_L = 2(\min I_o)$ = 4 A

$D = V_o/V_{in}$ = 0.2 to 0.4

t_{off} = 0.8x25 = 20 µs max

$L = V_o t_{off}/\Delta I_L$ = 12x20/4 = 60 µH

ESR Max for 0.1 V_{pp} Ripple at ΔI_L = 4 A:

R_c = 25 mΩ max (5 mΩ min)

C = 4000 µF

Basic Equations — Duty Cycle Control:

$D = V_c/V_s$:

DC Relationships:

(1) $V_o = V_{in}D = V_{in}\dfrac{V_c}{V_s}$ (1a) $V_c = \dfrac{V_oV_s}{V_{in}}$

Control to Output Gain:

(2) $\dfrac{v_o}{v_c} = \dfrac{V_{in}}{V_s}H_e(s)$. $H_e(s) = \dfrac{1 + s/\omega_z}{1 + (s/\omega_o)/Q + (s/\omega_o)^2}$, $\omega_o = \dfrac{1}{\sqrt{LC}}$, $\omega_z = \dfrac{1}{R_cC}$

Line to Output Gain:

(3) $\dfrac{v_o}{v_{in}} = \dfrac{V_c}{V_s}H_e(s) = \dfrac{V_o}{V_{in}}H_e(s)$ $Q = \dfrac{R_o}{\omega_o L}$

Corner Frequencies from Equation (2):

$f_o = 1/(2\pi\sqrt{LC})$ = 325 Hz

$f_z = 1/(2\pi R_cC) = 39.8/R_c$ = 1590 Hz at 25 mΩ, 7950 Hz at 5 mΩ

UC1524A ramp is 2.5 V at 80 kHz. One output is not used which limits duty cycle to 50% max. at 40kHz. V_s projects to 5 V over the full 40 kHz cycle.

Low Frequency Gain from Equation (2):

$v_o/v_c = V_{in}/5$ = 12 (21.6 dB) at 60 V

= 6 (15.6 dB) at 30 V

Error Amplifier Compensation:

Control I.C.: UC1524A
Crossover frequency (0 dB loop gain):

$f_c = f_s/4 = 10$ kHz

E/A gain needed at 10 kHz = 21.5 dB

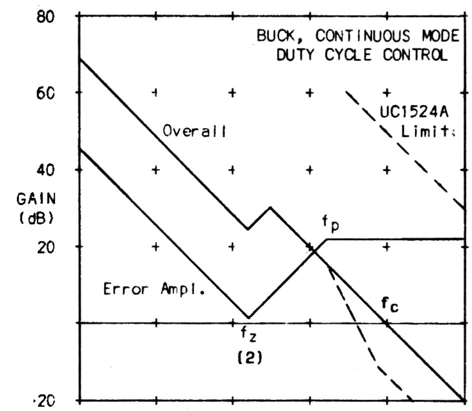
A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

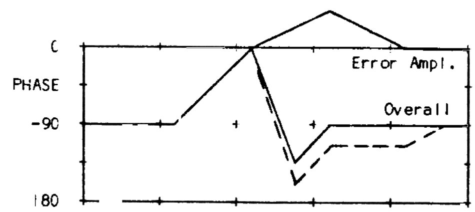
Two second order filter poles at f_o are compensated by two zeros at $f_z = f_o/2$. This provides additional phase shift at f_o for sudden second order transition.

$f_z = 325/2 = 162$ Hz

ESR zero, f_z, is canceled by pole f_p at least 5 times above f_o to avoid adding more phase lag at f_o. This happens to coincide with min. ESR zero, f_z.

$f_p = 1590$ Hz with 21.5 dB gain





E/A gain required at f_z is: $21.5 - 20\log(1590/162) = 1.7$ dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \frac{V_o V_s}{V_{in}} = \frac{12 \times 5}{V_{in}} = 1$ to 2 V. $\Delta V_c = 1$ V

Output voltage error with actual E/A DC gain of 180 (45 dB at 1 Hz):

$\Delta V_o = \Delta V_c/180 = 5.5$ mV (120 mV = 1% regulation)

Implementation: Circuit of Appendix A-2 (omit R_p, C_p and R_{fp})

UC1524A has transconductance error amplifier (gm = .002). Min. load resistance (min R_{fz}) is 30K. R_{iz} is appx. $1 \times R_{fz}$ (gain is 1.7 dB at f_z).

Set $R_{iz} = 50K$

Zero 2 at 162 Hz: $C_i = 1/(\omega_{z2} R_{iz}) = 1/2\pi\, 162 \times 50K = .02\ \mu F$

Pole 2 at 1590 Hz: $R_{ip} = R_{iz}/(R_{iz}\omega_{p2}C_i - 1) = 50K/(50K \times 2\pi\, 1590 \times .02) = 5.6K$

1.7 dB (1.22) gain at 162 Hz: $R_{fz} = 1.22(R_{ip} + R_{iz}) = 68K$

Zero 1 at 162 Hz: $C_f = 1/(\omega_{z1} R_{fz}) = 1/(2\pi\, 162 \times 68K) = .0144\ \mu F$

Pole 1 at 0 Hz: Omitting R_{fp} (open), $\omega_{p1} = 0$. Actual pole occurs at 80 dB gain limit of UC1524A error amplifier at a frequency well below 1 Hz.

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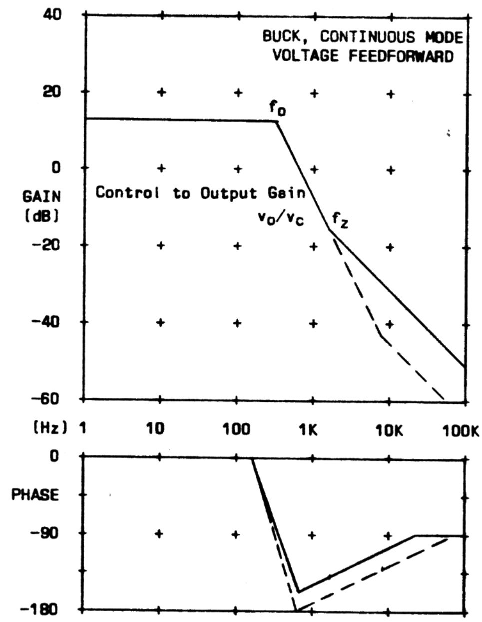
Example 5: 12 Volt, 240 Watt Output



All power circuit parameters are the same as Example 4.

Basic Equations — Voltage Feedforward

$D = V_c/V_s$, $V_s = V_{in}/K$, $K = V_{in}D/\max V_c$

DC Relationships:

(1) $V_o = V_{in}D = KV_c$ (1a) $V_c = \frac{V_o}{K}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = K\ H_e(s)$. $H_e(s) = \frac{1 + s/\omega_o}{1 + (s/\omega_o)/Q + (s/\omega_o)^2}$, $\omega_o = \frac{1}{\sqrt{LC}}$, $\omega_z = \frac{1}{R_cC}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = 0$ Inherent good line regulation $Q = \frac{R_o}{\omega_o L}$

Corner Frequencies from Equation (2):

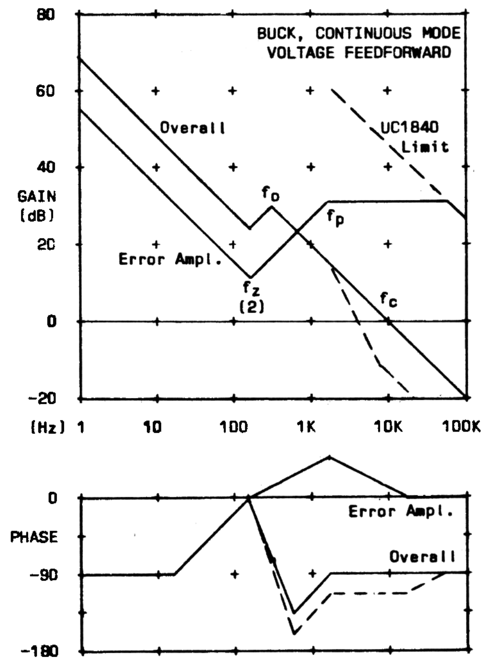
$f_o = 1/(2\pi\sqrt{LC}) = 325$ Hz

$f_z = 1/(2\pi R_c C) = 39.8/R_c$ = 1590 Hz at 25 mΩ, 7950 Hz at 5 mΩ

Low Frequency Gain from Equation (2) (max V_c = 3.5 V for UC1840):

$K = V_{in}D/\max V_c = 30 \times 0.5/3.5 = 4.29$ (feedforward factor)

$v_o/v_c = V_{in}/5 = 4.29$ (12.6 dB) at 30 to 60 V in.



Error Amplifier Compensation:

Control I.C.: UC1840
Crossover frequency (0 dB loop gain):

$f_c = f_s/4 = 10$ kHz

E/A gain needed at 10 kHz = 31 dB

A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

Two second order filter poles at f_o are compensated by two zeros at $f_z = f_o/2$. This provides additional phase shift at f_o for sudden second order transition.

$f_z = 325/2 = 162$ Hz

ESR zero, f_z, is canceled by pole f_p at least 5 times above f_o to avoid adding more phase lag at f_o. This happens to coincide with min. ESR zero, f_z.

$f_p = 1590$ Hz with 31 dB gain

E/A gain required at f_z is: $31 - 20\log(1590/162) = 11.2$ dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \frac{V_o}{V} = \frac{12}{4.29} = 2.8$ V constant DC. $\Delta V_c = 0$

DC Output voltage error is theoretically zero. Loop gain is required only for good dynamic response.

Implementation: Circuit of Appendix A-2 (omit R_p, C_p and R_{fp})

Voltage feedforward factor, K, in UC1840 is set by an independent ramp generator whose slope varies proportional to V_{in}. Minimum ramp charging current of 30 µA is chosen, near the bottom of the optimum range.

$R_r = \min V_{in}/\min I_r = 30/30\mu A = 1M$

$dv/dt = I_r/C_r = V_{in}/R_rC_r = \max v_c/t_{on}$. $R_rC_r = V_{in}t_{on}/\max v_c = K/f$

$C_r = K/fR_r = 4.29/(40K \times 1M) = 107$ pF

Set $R_{iz} = 50K$. With gain appx. 4 at 162 Hz (f_z), R_f of 200K is OK to drive.

Zero 2 at 162 Hz: $C_i = 1/(\omega_{z2}R_{iz}) = 1/2\pi\, 162 \times 50K = .02$ µF

Pole 2 at 1590 Hz: $R_{ip} = R_{iz}/(R_{iz}\omega_{p2}C_i - 1) = 50K/(50K \times 2\pi\, 1590 \times .02) = 5.6K$

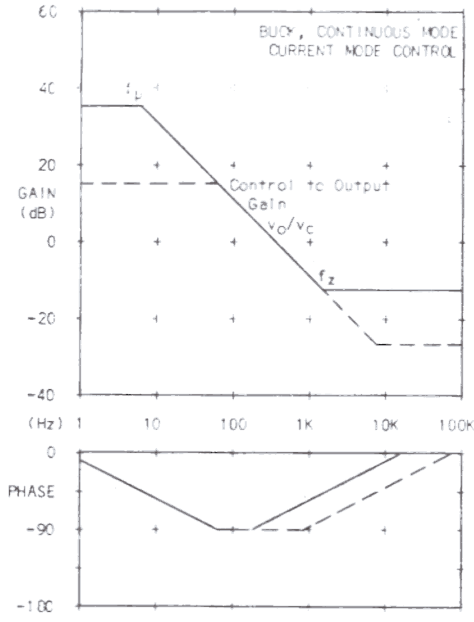
11.2 dB (3.63) gain at 162 Hz: $R_{fz} = 3.63(R_{ip} + R_{iz}) = 202K$

Zero 1 at 162 Hz: $C_f = 1/(\omega_{z1}R_{fz}) = 1/(2\pi\, 162 \times 200K) = .0049$ µF

Pole 1 at 0 Hz: Omitting R_{fp} (open), $\omega_{p1} = 0$. Actual pole occurs at 80 dB gain limit of UC1840 error amplifier at a frequency below 1 Hz.

BUCK - CONTINUOUS INDUCTOR CURRENT - CURRENT MODE CONTROL

Example 6: 12 Volt, 240 Watt Output



All power circuit parameters are the same as Example 4.

Basic Equations — Current Mode Control:

$I_L = KV_c$, $K = \max I_L / \max V_c$

DC Relationships:

(1) $V_o = I_L R_o = KV_c R_o$ (1a) $V_c = \dfrac{V_o}{KR_o}$

Control to Output Gain:

(2) $\dfrac{v_o}{v_c} = KR_o\, H_e(s)$. $H_e(s) = \dfrac{1 + s/\omega_z}{1 + s/\omega_p}$, $\omega_p = \dfrac{1}{R_o C}$, $\omega_z = \dfrac{1}{R_c C}$

Line to Output Gain:

(3) $\dfrac{v_o}{v_{in}} = 0$ Inherent good line regulation and audio susceptibility

Corner Frequencies from Equation (2):

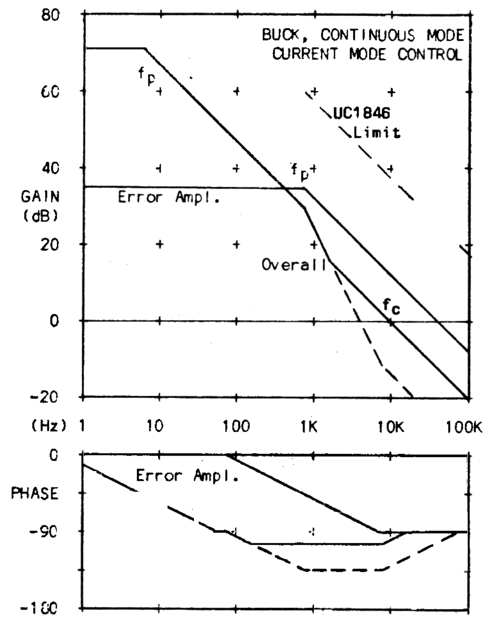
$f_p = 1/(2\pi R_o C)$ = 66.3 Hz at 0.6 Ω, 6.63 Hz at 6 Ω

$f_z = 1/(2\pi R_c C) = 39.8/R_c$ = 1590 Hz at 25 mΩ, 7950 Hz at 5 mΩ

Low Frequency Gain from Equation (2) (max V_c clamped to 2.5 V for 25 A I_{sc}):

$K = \max I_L / \max V_c = 25/2.5 = 10$

$v_o/v_c = KR_o$ = 6 (15.6 dB) at 0.6 Ω, 60 (35.6 dB) at 6 Ω



Error Amplifier Compensation:

Control I.C.: UC1846

Crossover frequency (0 dB loop gain):

$f_c = f_s/4 = 10$ kHz

E/A gain needed at 10 kHz = 12 dB

ESR zero, f_{zc}, is canceled by pole f_p at max $f_z/10$. This decade offset increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

$f_p = \max f_z/10 = 795$ Hz

E/A gain required at and below f_p is:

$12 + 20\log(10000/795) = 34$ dB (50)

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \dfrac{V_O}{KR_O} = \dfrac{12}{10R_O} = 0.2$ to 2 V. $\Delta V_c = 1.8$ V

Output voltage error with actual E/A gain of 50 (34 dB)

$\Delta V_o = \Delta V_c/50 = 36$ mV (0.3% regulation)

Implementation: Circuit of Appendix A-1 (omit R_p and C_p)

Current control factor, K = 10, in the UC1846 is set by the fixed gain (3X) of the current sense amplifier together with current sampling resistor R_s.

$K = I_L/V_c = 10 = 1/(3R_s)$. $R_s = 1/30 = .033\ \Omega$

UC1846 error amplifier gain limit is >80 dB with R_f >30K. 34 dB needed, OK

Gain required at and below f_p = 795 Hz is 50 (34 dB) = R_f/R_i.

Let R_f = 500K, $R_i = R_f/50$ = 10K

1 Pole at f_p = 795 Hz. $C_f = 1/(2\pi f_p R_f) = 400$ pF

Slope compensation: Current downslope is 4A/20µs, or 5A projected over 25 µs period, equating to 5x.033 = .165 volts p-p at input of current sense amplifier. Compensation ramp should be .165/2 = .082 V positive ramp. UC1846 oscillator ramp is 2 V. A 24:1 divider provides .083 V. Put 1K between current sense R_s and current sense amplifier input, and 24K from timing capacitor C_t to current sense ampl. input.

Example 7: 12 Volt, 60 Watt Output

f_s = 80 kHz, T = 12.5 µsec

V_{in} = 12 to 24 V

V_O = 12 V, I_O = 0.5 to 5 A

R_O = 24 to 2.4 Ohms

I_{sc} = 6 A Short Circuit Limit

Continuous Current Mode Boundary:

Min. I_O = 0.5 A

$D = V_O/V_O+V_i)$ = 0.33 to 0.5

Max. $\Delta I_L = 2(\min I_O)/(1-D\min)$ = 1.5 A

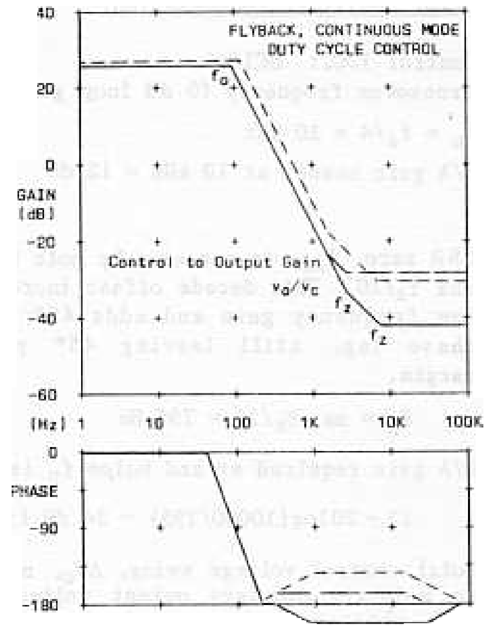
t_{off} = 12.5(1–D) = 8.33 µs max

$L = V_O t_{off}/\Delta I_L$ = 12x8.33/1.5 = 72 µH

$I_L\max = \max I_O/(1-D\max)$ = 10 A

ESR Max for 0.1 V_{pp} Ripple at I_L= 10 A:

R_c = 10 mΩ max (2 mΩ min), C = 10,000 µF



Basic Equations — Duty Cycle Control:

$D = V_c/V_s$: $\omega_o = \frac{1-D}{\sqrt{LC}}$, $\omega_z = \frac{1}{R_c C}$, $Q = \frac{R_o}{\omega_o L}$

DC Relationships:

(1) $V_o = V_{in}D/(1-D) = V_{in}/(V_s/V_c-1)$ (1a) $V_c = V_s\frac{V_o}{V_i+V_o}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{V_{in}}{V_s}(1+V_o/V_i)^2 f1(s)\ H_e(s)$. $H_e(s) = \frac{1+s/\omega_z}{1+(s/\omega_o)/Q+(s/\omega_o)^2}$,

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_c}{V_s} H_e(s) = \frac{V_o}{V_{in}} H_e(s)$ RHP zero: $f1(s) = 1 - \frac{sL}{R}\frac{V_o(V_o+V_i)}{V_i^2}$

Corner Frequencies:

$f_o = (1-D)/(2\pi\sqrt{LC})$ = 94 Hz at 12 V, 125 Hz at 24 V

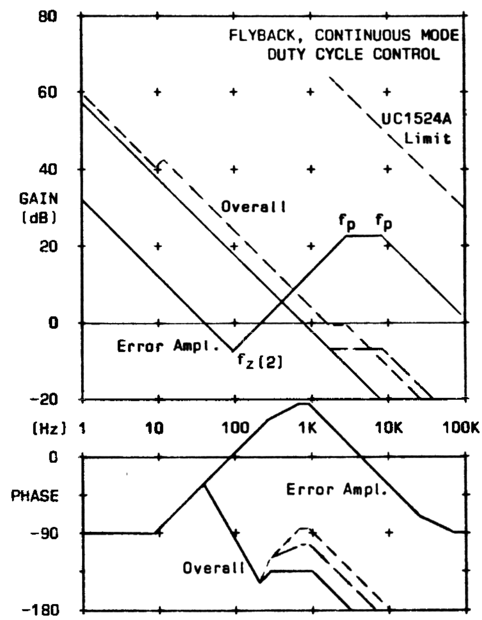
f_z (ESR) = $1/(2\pi R_c C)$ = 1590 Hz at 10 mΩ, 7950 Hz at 2 mΩ

f_z (RHP) = 2728 Hz at 12 V and 2.4 Ω, = 7275 Hz at 24 V and 2.4 Ω

UC1524A ramp V_s = 2.5 V. The two outputs of the UC1524A are paralleled.

Low Frequency Gain from Equation (2):

v_o/v_c = 19.2 (25.6 dB) at 12 V, = 21.6 (26.7 dB) at 24 V



Error Amplifier Compensation:

Control I.C.: UC1524A
Crossover frequency (0 dB loop gain):

f_c = 800 Hz (best achievable - RHPzero)

E/A gain needed at 800 Hz = 11.6 dB

A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

Two second order filter poles at f_o are compensated by two zeros at $f_z = f_o$.

f_z = 94 Hz

E/A gain required at f_z: -7 dB

Two additional poles cancel the ESR zero and right-half-plane zero. The location of these two poles is adjusted by trail and error. Although above the crossover frequency these poles are necessary or the gain would stay flat or even rise, causing instability at higher frequency.

f_p = 2700 Hz at 22.2 dB gain, f_p = 8000 Hz also at 22.2 dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = V_s \frac{V_o}{V_{in}+V_o}$ = 0.833 to 1.25 V. ΔV_c = .417 V

Output voltage error with actual E/A DC gain of 40 (32 dB at 1 Hz):

$\Delta V_o = \Delta V_c/40$ = 10 mV (0.1% regulation)

Implementation: Circuit of Appendix A-2 (omit R_{fp})

UC1524A has transconductance error amplifier (gm = .002). Min. load resistance (min R_{fz}) is 30K. R_{iz} is appx. $2xR_{fz}$ (gain is -7 dB at f_z).

Set R_{iz} = 100K

Zero 2 at 94 Hz: $C_i = 1/(\omega_{z2}R_{iz}) = 1/2\pi\ 94 \times 100K$ = .017 µF

Pole 2 at 2700 Hz: $R_{ip} = R_{iz}/(R_{iz}\omega_{p2}C_i - 1)$ = 100K/(100K x 2π 2700 x .017-1) = 3.6K

-7 dB (.45) gain at 94 Hz: $R_{fz} = .45(R_{ip} + R_{iz})$ = 47K

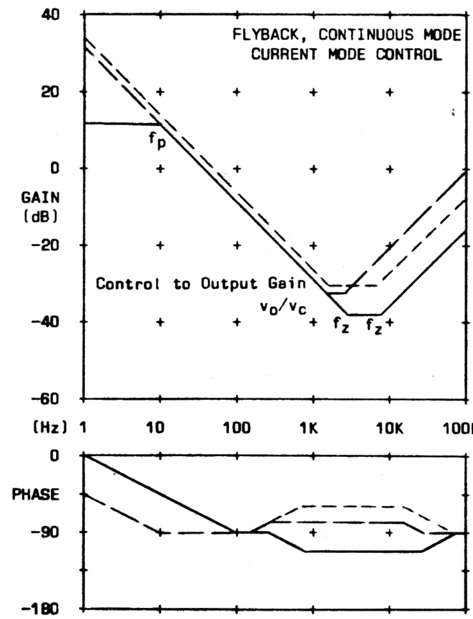
Zero 1 at 94 Hz: $C_f = 1/(\omega_{z1}R_{fz}) = 1/(2\pi\ 94 \times 47K)$ = .036 µF

Pole 1 at 0 Hz: Omitting R_{fp} (open), $\omega_{p1} = 0$. Actual pole occurs at 80 dB gain limit of UC1524A error amplifier at a frequency well below 1 Hz.

Pole 3 at 8000 Hz. $R_p = R_{ip}/10$ = 360 Ω. $C_p = 1/(2\pi f_{p3}R_p)$ = .055 µF

FLYBACK - CONTINUOUS INDUCTOR CURRENT - CURRENT MODE CONTROL

Example 8: 12 Volt, 60 Watt Output



All power circuit parameters are the same as Example 7.

Basic Equations — Duty Cycle Control:

$I_O = I_L(1-D)$, $I_L = KV_C$, $K = \max I_L/\max V_C$, $\omega_z = \dfrac{1}{R_cC}$, $\omega_p = \dfrac{1+D}{R_OC}$, $D = \dfrac{V_{in}}{V_O + V_{in}}$

DC Relationships:

(1) $V_O = V_{in} D/(1-D) = K V_C R_O \dfrac{V_{in}}{V_O+V_{in}}$ (1a) $V_C = \dfrac{V_O(V_O+V_{in})}{KR_O\ V_{in}}$

Control to Output Gain:

(2) $\dfrac{v_o}{v_c} = K R_O \dfrac{V_{in}}{(2V_O + V_{in})}\ f1(s)\ H_e(s)$. $H_e(s) = \dfrac{1 + s/\omega_z}{1 + s/\omega_p}$

Line to Output Gain:

(3) $\dfrac{v_o}{v_{in}} = \dfrac{V_O^2}{2V_OV_{in} + V_{in}^2} H_e(s)$ RHP zero: $f1(s) = 1 - \dfrac{sL}{R}\dfrac{V_O(V_O + V_{in})}{V_{in}^2}$

Corner Frequencies:

$f_p = (1+D)/(2\pi R_OC) = 0.884$ Hz at 24 V, 24 Ω, $= 9.95$ Hz at 12 V, 2.4 Ω

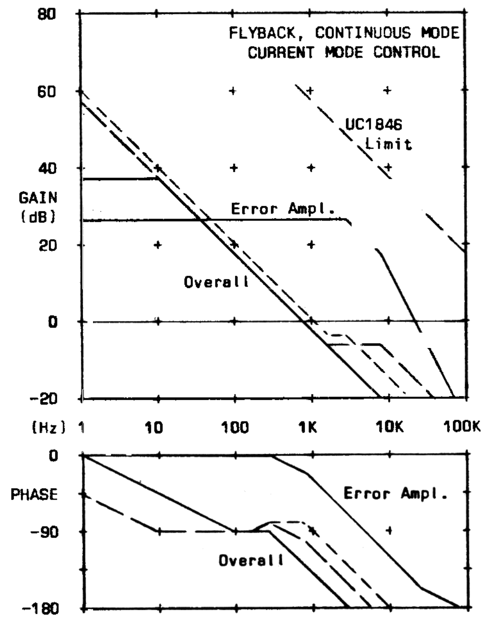
f_z (ESR) $= 1/(2\pi R_cC)$ $= 1590$ Hz at 10 mΩ, 7950 Hz at 2 mΩ

f_z (RHP) $= 2728$ Hz at 12 V and 2.4 Ω, $= 7275$ Hz at 24 V and 2.4 Ω

Low Frequency Gain from Equation (2):

$$K = \frac{\max I_L}{\max V_C} = \frac{\max I_O}{(1-D)\max V_C} = \frac{6}{(1-.5)2.5} = 4.8$$

$v_o/v_c = 57.6$ (35.2 dB) at 24 V, 24 Ω, $= 3.84$ (11.7 dB) at 12 V, 2.4 Ω



Error Amplifier Compensation:

Control I.C.: UC1846

Crossover frequency (0 dB loop gain):

f_c = 800 Hz (best achievable - RHPzero)

E/A gain needed at 800 Hz = 26.4 dB

Two poles cancel the ESR zero and right-half-plane zero. The location of these two poles is set by trail and error. Although above the crossover frequency, these poles are necessary or the gain would stay flat or even rise, causing instability at higher frequency.

f_p = 2700 Hz at 26.4 dB gain
f_p = 8000 Hz at 17.1 dB

The E/A gain is flat (26.4 dB) below the first pole at 2700 Hz.

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $$V_c = \frac{V_o(V_o+V_{in})}{KR_o\ V_{in}} = 0.156 \text{ to } 2.08 \text{ V.} \qquad \Delta V_c = 1.92 \text{ V}$$

Output voltage error with actual E/A DC gain of 20.1 (26.4 dB below 2700 Hz):

$\Delta V_o = \Delta V_c/20.1 = 1.92/20.1$ = 95 mV (1% regulation)

Implementation: Circuit of Appendix A-1

Current control factor, K = 4.8, in the UC1846 is set by the fixed gain (3X) of the current sense amplifier together with current sampling resistor R_s.

$K = I_L/V_c = 4.8 = 1/(3R_s)$. $R_s = .069\ \Omega$

UC1846 error amplifier gain limit is >80 dB with R_f >30K. 26.4 dB needed, OK

Gain required (26.4 dB) = 20.9 = R_f/R_i. Let R_f = 500K, R_i = 500K/20.9 = 24K.

Pole 1 at f_p = 2700 Hz. $C_f = 1/(2\pi f_p R_f)$ = 120 pF
Pole 2 at f_p = 8000 Hz $R_p = R_i/10$ = 2.4K. $C_p = 1/(2\pi f_p R_p)$ = 8200 pF

Slope compensation: Current downslope is 1.5A/8.33 µs, or 2.25A projected over the 12.5 µs period. This equates to 2.25x.069 = .155 volts p-p at the current sense amplifier input. Compensation ramp should be .155/2 = .078 V positive ramp. UC1846 oscillator ramp is 2 V. A 25:1 divider provides .077 V. Put 1K between current sense resistor R_s and current sense amplifier input, and 24K from timing capacitor C_t to current sense amplifier input.

BOOST CONFIGURATIONS — BASIC EQUATIONS

Boost regulator topologies have the same general characteristics as their flyback circuit counterparts. The Bode plots have the same shape, and the same type of compensation is employed. The specific values of gain and pole/zero frequencies are slightly different because of modifying factors in the various basic equations: Accordingly, only the basic equations are given for the boost circuits.

BOOST — Discontinuous Inductor Current — Duty Cycle Control:

DC Relationships:

(1) $V_o = V_{in}(1/2 + \sqrt{1/4 + D^2/J})^{\frac{1}{2}}, \quad D = V_c/V_s, \quad J = 2Lf_s/R_o$

Control to Output Gain:

(2) $\dfrac{v_o}{v_c} = \dfrac{V_{in}}{V_s\sqrt{J}}\left(\dfrac{4-V_{in}/V_o}{4-V_{in}/V_o-V_{in}^2/V_o^2}\right)^{\frac{1}{2}} H_e(s). \qquad H_e(s) = \dfrac{1+s/\omega_z}{1+s/\omega_p}$

Line to Output Gain:

(3) $\dfrac{v_o}{v_{in}} = \dfrac{V_o}{V_{in}} H_e(s), \qquad \omega_z = \dfrac{1}{R_cC}, \qquad \omega_p = \dfrac{2+1/\sqrt{1+4D^2/J}}{R_oC}$

BOOST — Discontinuous Inductor Current — Voltage Feedforward:

DC Relationships: $\quad V_s = V_{in}/K, \quad K = V_{in}D/\max V_c$

$V_o = V_{in}(1/2 + \sqrt{1/4 + (K^2/J)V_c^2/V_{in}^2})^{\frac{1}{2}}, \quad D = V_c/V_s = \dfrac{KV_c}{V_i}, \quad J = 2Lf_s/R_o$

Control to Output Gain:

(2) $\dfrac{v_o}{v_c} = \dfrac{K}{\sqrt{J}}\left(\dfrac{4-V_{in}/V_o}{4-V_{in}/V_o-V_{in}^2/V_o^2}\right)^{\frac{1}{2}} H_e(s). \qquad H_e(s) = \dfrac{1+s/\omega_z}{1+s/\omega_p}$

Line to Output Gain:

(3) $\dfrac{v_o}{v_{in}} = \dfrac{V_o}{2V_o-V_{in}} H_e(s), \qquad \omega_z = \dfrac{1}{R_cC}, \qquad \omega_p = \dfrac{2+1/\sqrt{1+4D^2/J}}{R_oC}$

BOOST — Discontinuous Inductor Current — Current Mode Control:

DC Relationships: $\quad I_p = KV_c, \quad K = \max I_p/\max V_c$

(1) $V_o = V_{in}(1/2 + \sqrt{1/4 + (K^2/J)V_c^2/V_{in}^2})^{\frac{1}{2}}, \quad D = V_c/V_s = \dfrac{KV_c}{V_i}, \quad J = 2Lf_s/R_o$

Control to Output Gain:

(2) $\dfrac{v_o}{v_c} = \dfrac{K}{\sqrt{J}}\left(\dfrac{4-V_{in}/V_o}{4-V_{in}/V_o-V_{in}^2/V_o^2}\right)^{\frac{1}{2}} H_e(s). \qquad H_e(s) = \dfrac{1+s/\omega_z}{1+s/\omega_p}$

Line to Output Gain:

(3) $\dfrac{v_o}{v_{in}} = \dfrac{V_o}{2V_o-V_{in}} H_e(s), \qquad \omega_z = \dfrac{1}{R_cC}, \qquad \omega_p = \dfrac{2+1/\sqrt{1+4D^2/J}}{R_oC}$

BOOST CONFIGURATIONS -- BASIC EQUATIONS

Boost — Continuous Inductor Current — Direct Duty Cycle Control:

$$D = V_c/V_s, \quad (1-D) = V_i/V_o, \quad \omega_o = \frac{1-D}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_c C}, \quad Q = \frac{R_o}{\omega_o L}$$

DC Relationships:

(1) $V_o = V_{in}/(1-D) = V_{in}/(1-V_c/V_s)$ (1a) $V_c = V_s \dfrac{V_o - V_{in}}{V_o}$

Control to Output Gain:

(2) $\dfrac{v_o}{v_c} = \dfrac{V_{in}}{V_s} \dfrac{V_o^2}{V_{in}^2} f_1(s)\ H_e(s).$ $H_e(s) = \dfrac{1 + s/\omega_z}{1 + (s/\omega_o)/Q + (s/\omega_o)^2},$

Line to Output Gain:

(3) $\dfrac{v_o}{v_{in}} = \dfrac{V_o}{V_{in}} H_e(s)$ RHP zero: $f_1(s) = 1 - \dfrac{sL}{R} \dfrac{V_o^2}{V_i^2}$

Boost — Continuous Inductor Current — Current Mode Control:

$$I_o = I_L(1-D), \quad I_L = KV_c, \quad \omega_p = \frac{2}{R_o C}, \quad \omega_z = \frac{1}{R_c C}, \quad D = \frac{V_o - V_{in}}{V_o}$$

DC Relationships:

(1) $V_o = \sqrt{KV_cR_oV_i}$ (1a) $V_c = V_o^2/(KR_oV_i)$

Control to Output Gain:

(2) $\dfrac{v_o}{v_c} = \dfrac{KR_o}{2} \dfrac{V_{in}}{V_o} f_1(s)\ H_e(s).$ $H_e(s) = \dfrac{1 + s/\omega_z}{1 + (s/\omega_o)/Q + (s/\omega_o)^2}$

Line to Output Gain:

(3) $\dfrac{v_o}{v_{in}} = \dfrac{V_o}{2V_{in}} H_e(s)$ RHP zero: $f_1(s) = 1 - \dfrac{sL}{R} \dfrac{V_o^2}{V_i^2}$

Voltage feedforward control does not perform effectively with continuous mode boost and flyback circuits, and this use is not recommended.

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