TPS92070 Design Calculator worksheet

- **Yellow Highlighted areas are User defined inputs, bordered areas are calculated results**
- **Assume worst case for calculations**
- **Using Cree XLamp MX-6 warm white LEDs as a reference for LED specifications**

Unit definitions:

$m\Omega := 10^{-3}\cdot\Omega$ $mW := 10^{-3}W$ $ns := 10^{-9}s$ $nC := 10^{-9}\cdot C$ $nH := 10^{-9}\cdot H$ $mJ := 1\cdot 10^{-3}J$

Input Parameters: need to allow for input voltage sag for the VACmin value to prevent ficker at minimum current. Also note that dynamic range of the device does not lend itself to Universal input range

AC INPUT: Enter the input voltage range for the specific application

$V_{ACmin} := 180V$

$V_{ACmax} := 265V$

$V_{ACnom} := 230V$

$f_{LINE} := 50Hz$

$V_{INmin} := \sqrt{2}\cdot V_{ACmin}$

$V_{INmin} = 254.558\ V$

$V_{INmax} := \sqrt{2}\cdot V_{ACmax}$

$V_{INmax} = 374.767\ V$

$V_{INnom} := \sqrt{2}\cdot V_{ACnom}$

$V_{INnom} = 325.269\ V$

The LED load: calculations for design, use maximum LED voltage for mass market design calculations

$I_{LED} := 370mA$ **Enter the desired LED current for the specific application**

$n_{LED} := 5$ **Enter the number of LEDs in the series string for the specific application**

$V_{LEDmax} := 3.8V$ $V_{LEDnom} := 3.3V$

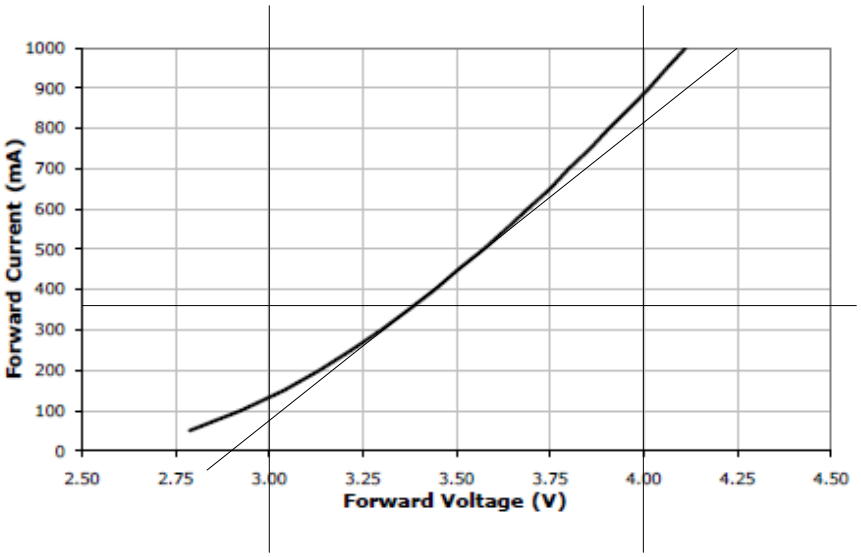
$V_{OUTmax} := V_{LEDmax}\cdot n_{LED}$ $V_{OUT} := V_{LEDnom}\cdot n_{LED}$

$V_{OUTmax} = 19\ V$ $V_{OUT} = 16.5\ V$

$P_{OUTmax} := V_{OUTmax}\cdot I_{LED}$ $P_{OUT} := V_{OUT}\cdot I_{LED}$

$P_{OUTmax} = 7.03\ W$ $P_{OUT} = 6.105\ W$

Differential resistance of LEDs, which is the change in forward voltage/change in current for the LEDs. Assume they are all similar to CREE (approximating with a straight line at I_{LED}).



$\Delta V_{LED} := 1V$ **Enter the estimated change in voltage using extrapolated straight line at desired output current**

$\Delta I_{LED} := 800mA - 75mA$

$$R_{LED} := \frac{\Delta V_{LED}}{\Delta I_{LED}}$$

$R_{LED} = 1.379\ \Omega$ **Estimated dynamic resistance per LED**

Design Expectations/ Assumptions:

$f_{SWmin} := 30kHz$ **Minimum design frequency at max power, minimum input. Do not want to operate at the 20kHz minimum frequency clamp listed on the data sheet as this may result in flicker at the frequency limit during transients**

$$T_{SWmax} := \frac{1}{f_{SWmin}}$$

$T_{SWmax} = 33.333\ \mu s$

Load Line Operating Point:

- **switching frequency at Vbulk_min set to f_{SWmin} to calculate inductance.**
- **As the bulk voltage increases, the switching frequency will increase up to a max of 146kHz (maximum max frequency clamp, actual max frequency will depend upon the final transformer design).**

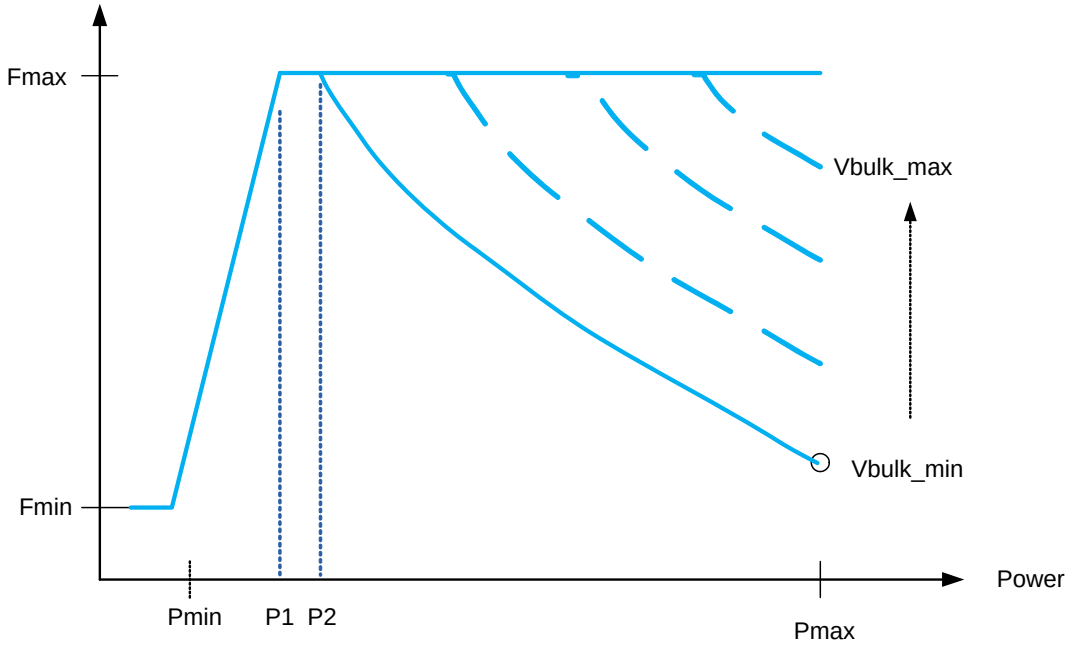
As Vin increases, frequency increases for a given Pmax

Mode 1, Transition Mode: From Pmax to P2, variable Ipeak, variable fs, with valley detect. Vpwm ranges from 0.6V at Pmax, down to 0.065V at P2; VCOMP will be from 3.7V (Pmax) to somewhere around 2.6V (P2)

Mode 2, DCM: From P2 to P1, maximum fixed frequency, variable Ipeak, with valley detect, ends when Vcomp = 2.6V, Vpwm = 0.065V throughout entire mode (hence the fixed frequency)

Mode 3, Frequency Foldback: From P1 to Pmin, fixed peak current, variable frequency, with valley detect, VCOMP is between 2.6V and 1.63V,

Mode 4, Open Control Loop: Below Pmin, fixed frequency , fixed minimum peak current, no valley detect



$\eta := 0.82$ **Anticipated full load efficiency**

$PF_{min} := 0.8$ **Required PF for residential lighting is 0.7 but circuit will have a higher PF when operated without a dimmer, thanks to valley fill PFC**

$$P_{INmax} := \frac{P_{OUTmax}}{\eta}$$

$P_{INmax} = 8.573\ W$

$$I_{IN\_RMSmax} := \frac{P_{INmax}}{V_{INmin} \cdot PF_{min}}$$

$I_{IN\_RMSmax} = 42.098\ mA$

- **Fuse rating will be dependent upon user input voltage requirements**
- **Input varistor rated for 300V placed after diff. chokes to take advantage of the choke impedance**
- **Differential mode chokes worked better than single common mode choke on the input. 7.5k resistors in parallel for damping orf input surge**
- **X2 capacitor placed after diff. mode choke, 10nF, high value capacitors may interfere with triac dimmer, testing may indicate using a lower value**
- **Varnish Differential mode inductors to reduce audible hum, but some hum still evident, need potting? swap out ceramic caps?**
- **Capacitors on either side of differential mode inductor L1 should be smallest recommended value to try to get the best PF possible.**
- **Safety Y1 capacitor 3300pF, large enough to eliminate the CM choke**

Bridge rectifier:

$I_{BRIDGEavg} := 10 \cdot I_{IN\_RMSmax}$

$V_{BRIDGEblocking} := V_{INmax}$

$V_{F\_BRIDGE} := 1.0V$

$P_{BRIDGE} := V_{F\_BRIDGE} \cdot I_{IN\_RMSmax}$

$P_{BRIDGE} = 0.042\,W$

Valley fill circuit: two stage circuit allows power to be drawn from line over larger portion of AC line cycle ...capacitors set up so they charge in series (each to half the bulk voltage for two stage), discharge in parallel...results in passive power factor correction. First capacitor must be sized for peak bulk voltage, second for half bulk voltage. Because valley fill and dimmers don't play well together, the TDD signal will turn on the Q1 valley fill swich when a dimmer is detected. In that way, only the first capacitor is in circuit and the rest of the valley fill components are not. Dimmer existence is confirmed when the time it takes for SEN to cross 1V rising threshold to 5V rising threshold is less than 100us...typical 50-60 Hz line voltage would take 300us to 1.1ms. If flickering...check to see if SEN is configured to drop below 1V...

From 150 degrees to 210 degrees on the input sine wave the capacitors will be discharging (the time period when the amplitude of the sine wave is below 1/2 peak), ...

$\Delta t_{VF} := \frac{1}{6} \cdot \frac{1}{f_{LINE}}$ **60 degrees out of 360 degree cycle the valley fill capacitors are delivering current**

$\Delta t_{VF} = 3.333\,ms$ **Required hold up time for valley fill capacitors**

$V_{BULKvf} := \frac{\sqrt{2} \cdot V_{ACmin}}{2}$

$V_{BULKvf} = 127.279\,V$ **Bulk voltage that valley fill capacitors charge and discharge in a two stage design**

$V_{BULKmin} := 0.75 \cdot V_{BULKvf}$ **Assuming I let the capacitors discharge 25%**

$V_{BULKmin} = 95.459\,V$ **Allowed minimum bulk voltage during valley fill discharge time**

$\Delta V := V_{BULKvf} - V_{BULKmin}$

$\Delta V = 31.82\,V$ **Allowed droop during valley fill discharge**

$C_{VFtotal} := \frac{2 P_{INmax} \cdot \Delta t_{VF}}{V_{BULKvf}^{2} - V_{BULKmin}^{2}}$

$C_{VFtotal} = 8.064\,\mu F$

$$C_{VF} := \frac{C_{VFtotal}}{2}$$

$C_{VF} = 4.032\,\mu F$

$C_{VF} := 4.7\mu F$ **Enter the Actual value of valley fill capacitors used**

$V_{Cvf1} := V_{INmax}$

$V_{Cvf1} = 374.767\ V$ **Capacitor on first stage rated for 400V min required**

$$V_{Cvf2} := \frac{V_{INmax}}{2}$$

$V_{Cvf2} = 187.383\ V$ **Capacitor on second stage could berated for 200V min**

$$V_{BULKmin} := \sqrt{V_{BULKvf}^{2} - \frac{2P_{INmax}\cdot\Delta t_{VF}}{2\cdot C_{VF}}}$$

$V_{BULKmin} = 100.597\ V$

Or can use a rule of thumb of 0.5uF per W for 230Vac design, 1uF per Watt for 115Vac:

$$C_{ValleyFill} := \text{if}\left(V_{ACnom} > 200V, \frac{0.5\mu F}{W}\cdot P_{INmax}, \frac{1\mu F}{W}\cdot P_{INmax}\right)$$

$C_{ValleyFill} = 4.287\,\mu F$ **same result, and easier (!)**

The VF resistor reduces input surge and smoothes out the current spike at the transition from series to parallel connection of the valley fill caps and will be subjected to huge surges, surge rated for 250W for 1ms everytime AC is switched on...larger values smooth out spike better but cost on efficiency. If resistor is not surge rated it will burn right off the board after multiple start ups; PF minimum requirement met when the resistor was replaced with a short to maximize efficiency, PF > 0.8 at nominal input. Select standard diode, such as 1N4007 1A, 1000V.

VF FET switch: must have voltage rating equal to half peak voltage and Rdson of 2 Ohms is good.

Output Capacitors: LEDs are very tolerant of voltage and current ripple, minimal output capacitance is acceptable, the loop will take care of the line frequency ripple and the switching frequency ripple is negligible (it's a don't care) for LEDs. ***Assume 1uF per 1W of nominal output power, add 20% derating for temperature*****, LEDs are very tolerant of output ripple so no output inductor used**

$$C_{OUT} := \left(\frac{1\mu F}{1W}\cdot P_{OUTmax}\right)\cdot 1.2$$

$C_{OUT} = 8.436\,\mu F$

$C_{OUT} := 10\mu F$ **Add enough margin for temperature to meet the capacitance and size requirements and Enter actual value used here**

Flyback Inductor: For ZVS switching, set Turns Ratio of transformer such that the flyback voltage is equal to the maximum bulk voltage. $t_{DEADTIME}$ is equal to 1/2 the resonance of L_P and C_{PRI}, C_{PRI} is the sum of C_{OSS} + C_{EXTDS}, C_{LPRI}, $C_{reflectedDiode}$.... but initial calculations just use C_{OSS}...actual deadtime calculated after FET sellected

$V_{FLYBACK} := V_{INmax}$ **To strive for zero voltage switching, maximize efficiency**

$V_{FLYBACK} = 374.767\ V$

$T_{SWmax} := \frac{1}{f_{SWmin}}$

$T_{SWmax} = 33.333\ \mu s$

$T_{SW} = t_{ON} + t_{DEMAG} + t_{DEADTIME}$

$V_F := 0.65V$ **Forward drop of the output diode**

$N_{PS} := \frac{V_{FLYBACK}}{V_{OUTmax} + V_F}$

$N_{PS} = 19.072$ **Calculated primary to secondary turns ratio**

$N_{PS} := 18.5$ **Enter the Actual primary to secondary turns ratio, as supplied by magnetics manufacturer**

$V_{FLYBACK} := N_{PS} \cdot (V_{OUT} + V_F)$

$V_{FLYBACK} = 317.275\ V$

$V_{DS\_PRI} := V_{INmax} + V_{FLYBACK}$

$V_{DS\_PRI} = 692.042\ V$

Primary Inductance: Balanced volt*seconds ...$t_{DEADTIME}$ estimated to be 500ns until actual deadtime (0.5 times the resonance of Lpri and Coss) is measured

$t_{ON} = T_{SW} - t_{DEADTIME} - t_{DEMAG}$

Volt Seconds IN:

$V_{BULKmin} \cdot t_{ON} = L_P \cdot I_{PRIpeak}$

Volt Seconds OUT (demagnetizing):

$$\left(V_{OUT} + V_F\right)\cdot t_{DEMAG} = \frac{L_P}{N_{PS}^{\,2}}\cdot I_{PRIpeak}\cdot N_{PS}$$

$$\left(V_{OUT} + V_F\right)\cdot t_{DEMAG}\cdot N_{PS} = L_P\cdot I_{PRIpeak}$$

Make them balance:

$$V_{BULKmin}\cdot t_{ON} = \left(V_{OUT} + V_F\right)\cdot t_{DEMAG}\cdot N_{PS}$$

$$V_{BULKmin}\cdot t_{ON} = \left(V_{OUT} + V_F\right)\cdot\left(T_{SW\_FMmin} - t_{DEADTIME} - t_{ON}\right)\cdot N_{PS}$$

$t_{DEADTIME} := 500\,ns$ **Assumption for now**

$$t_{ON} := \frac{\left(V_{OUT} + V_F\right)\cdot N_{PS}\cdot\left(T_{SWmax} - t_{DEADTIME}\right)}{V_{BULKmin} + \left(V_{OUT} + V_F\right)\cdot N_{PS}}$$

$t_{ON} = 24.929\,\mu s$

Calculate the Primary Inductance:

$$I_{PRIpeak} = \frac{V_{BULKmin}\cdot t_{ON}}{L_P}$$

$$P_{INmax} = \frac{L_P\cdot I_{PRIpeak}^{\,2}\cdot f_{SWmin}}{2}$$

$$P_{INmax} = \frac{L_P\cdot\left(\frac{V_{BULKmin}\cdot t_{ON}}{L_P}\right)^2\cdot f_{SWmin}}{2}$$

$$P_{INmax} = \frac{L_P\cdot\left(\frac{V_{BULKmin}\cdot t_{ON}}{L_P}\right)^2\cdot f_{SWmin}}{2}$$

$$L_{Pnom} := \frac{\left(V_{BULKmin}\cdot t_{ON}\right)^2\cdot f_{SWmin}}{2\cdot P_{INmax}}$$

$L_{Pnom} = 11.004\,mH$

$L_P := 13.80\,mH$ **Enter the Actual inductance from magnetics manufacturer**

Assuming the primary inductance is +/- 10%:

$L_{Pmin} := 0.9 \cdot L_P$

$L_{Pmin} = 12.42\ mH$

$L_{Pmax} := 1.1 \cdot L_P$

$L_{Pmax} = 15.18\ mH$

Maximum Peak primary current: Maximum value calculated using minimum primary inductance

$$I_{PRIpeak} := \sqrt{\frac{2 \cdot P_{INmax}}{L_{Pmin} \cdot f_{SWmin}}}$$

$I_{PRIpeak} = 214.518\ mA$

Maximum On-time:

$$t_{ON} := \frac{I_{PRIpeak} \cdot L_{Pmin}}{V_{BULKmin}}$$

$t_{ON} = 26.485\ \mu s$

Primary Current Sense (PCS) Resistor:

$V_{PWMthreshold\_typ} := 0.5V$

$V_{PCS} := V_{PWMthreshold\_typ}$

$$R_{PCS} := \frac{V_{PCS}}{I_{PRIpeak}}$$

$R_{PCS} = 2.331\ \Omega$

$R_{PCS} := 2.37\Omega$ **Enter the Actual value used for primary current sense resistor**

$V_{PCSmax} := 650mV$

$$I_{PRIpeak} := \frac{V_{PCSmax}}{R_{PCS}}$$

$I_{PRIpeak} = 0.274\ A$

$$I_{PRIrms} := \frac{I_{PRIpeak}}{\sqrt{3}} \cdot \sqrt{\frac{t_{ON}}{T_{SWmax}}}$$

$I_{PRIrms} = 0.141\ A$

$$P_{RPCS} := I_{PRIrms}^{2} R_{PCS}$$

$P_{RPCS} = 0.047\ W$

$$t_{DEMAG} := L_{Pmin} \cdot \frac{I_{PRIpeak}}{(V_{OUT} + V_F) \cdot N_{PS}}$$

$t_{DEMAG} = 10.736\ \mu s$

Primary side over-current limit: Calculate minimum threshold to make sure not within normal operating conditions

$V_{PCS\_PCL} := 670mV$

$$I_{PRI\_OCLpeak} := \frac{V_{PCS\_PCL}}{R_{PCS}}$$

$I_{PRI\_OCLpeak} = 0.283\ A$

$I_{SEC\_OCLpeak} := I_{PRI\_OCLpeak} \cdot N_{PS}$

$I_{SEC\_OCLpeak} = 5.23\ A$

Bias Winding: now that the on-time and demagnetizing times are better known

$V_{BIAS} := 12V$ **Bias voltage desired**

$V_{Fbias} := 0.7V$ **Forward voltage drop of diode on bias winding**

$$N_{PB} := \frac{V_{BULKmin} \cdot t_{ON}}{(V_{BIAS} + V_{Fbias}) \cdot t_{DEMAG}}$$

$N_{PB} = 19.54$

$N_{PB} := 23.12$ **Enter the Actual primary to bias turns ratio, as supplied by magnetics manufacturer**

$$V_{BIAS} := \frac{V_{BULKmin} \cdot t_{ON} - N_{PB} \cdot t_{DEMAG} \cdot V_{Fbias}}{N_{PB} \cdot t_{DEMAG}}$$

$V_{BIAS} = 10.034\ V$

MOSFET rating:

$$V_{DS} := V_{INmax} + V_{FLYBACK} + 0.3 \cdot V_{INmax}$$

$V_{DS} = 804.472\ V$

Use FET with good avalanche rating. A capacitor across Drain to source will slow down the rise time and avoid adding a snubber and help with EMI.

Input the MOSFET characteristics of the actual device that will be used. Example shows STD3NK80ZT4 parameters but the User MUT input the specific characteristics of the MOSFET used

$I_{PRIpeak} = 0.274\ A$ $t_f := 40 \cdot ns$ $R_{DSon} := 4.5\Omega$ $Q_g := 19 \cdot nC$

$f_{SWmax} := 146kHz$ $C_{OSS} := 57pF$ $C_{ISS} := 485 \cdot pF$

$$P_{FETcond} := I_{PRIrms}^{2} \cdot R_{DSon}$$

$P_{FETcond} = 0.09\ W$

$$V_{DSswitching} := V_{INmax} - N_{PS} \cdot (V_{OUT} + V_F)$$

$V_{DSswitching} = 57.492\ V$

$$P_{FETswitching} := f_{SWmax} \cdot \left(\frac{C_{OSS} \cdot V_{DSswitching}^{2}}{2} + \frac{V_{DSswitching} \cdot I_{PRIpeak} \cdot t_f}{2} \right)$$

$P_{FETswitching} = 59.795\ mW$

$$P_{FET} := P_{FETcond} + P_{FETswitching}$$

$P_{FET} = 0.149\ W$

Resonant ringing:

$$f_{RES} := \frac{1}{2 \cdot \pi \cdot \sqrt{L_P \cdot C_{OSS}}}$$

$f_{RES} = 0.179\ MHz$

Timing to hit first valley:

$$t_{DEADTIME} := \frac{1}{2 \cdot f_{RES}}$$

$t_{DEADTIME} = 2.786\,\mu s$

This is a more accurate estimate than the 500ns initial estimate

$$f_{SWmin} := \frac{1}{t_{ON} + t_{DEMAG} + t_{DEADTIME}}$$

$f_{SWmin} = 24.995\,kHz$

Actual minimum switching frequency

Output Diode: use a Schottky to minimize losses

$$I_{SECpeak} := I_{PRIpeak} \cdot N_{PS}$$

$I_{SECpeak} = 5.074\ A$

$$I_{SECrms} := \frac{I_{SECpeak}}{\sqrt{3}} \cdot \sqrt{\frac{t_{DEMAG}}{T_{SWmax}}}$$

$I_{SECrms} = 1.663\ A$

$V_{Fdiode} := 0.62V$

Enter forward drop of diode used

$$V_{Drating} := \left(\frac{V_{INmax}}{N_{PS}} + V_{OUT}\right) \cdot 1.3$$

$V_{Drating} = 47.785\,V$

$$P_{DIODEcond} := V_{Fdiode} \cdot I_{LED}$$

$P_{DIODEcond} = 0.229\,W$

Secondary side current during an OCL:

$$I_{SECocl\_rms} := \frac{N_{PS} \cdot I_{PRI\_OCLpeak}}{\sqrt{3}} \cdot \sqrt{\frac{t_{DEMAG}}{T_{SWmax}}}$$

$I_{SECocl\_rms} = 1.714\ A$

$$I_{SECocl\_avg} := \frac{N_{PS} \cdot I_{PRI\_OCLpeak}}{2} \cdot \frac{t_{DEMAG}}{T_{SWmax}}$$

$I_{SECocl\_avg} = 0.842\ A$

Secondary Side LED Current Sense Resistor:

$V_{CS} := 100mV$

$$R_{LEDsense} := \frac{V_{CS}}{I_{LED}}$$

$R_{LEDsense} = 0.27\ \Omega$

$R_{LEDsense} := 0.27\Omega$ **Enter the actual value of the LED current sense resistor used**

$$I_{LED} := \frac{V_{CS}}{R_{LEDsense}}$$

$I_{LED} = 0.37\ A$

$P_{RLEDsense} := I_{SECrms}^{2} \cdot R_{LEDsense}$

$P_{RLEDsense} = 0.746\ W$

$V_{LEDsense} := R_{LEDsense} \cdot I_{LED}$

$V_{LEDsense} = 0.1\ V$

Use a half Watt 1206 resistor

TPS92070 Pins:

Pin 1 BP: ABS MAX = -0.3 to 7.7V, Per pin description for bypassing internal 7V regulator that powers the gate driver, ceramic, 10V, place close to IC. BP can supply 1mA max so do not connect any other circuitry to BP. Also want the capacitor on BP low enough so BP is allowed to discharge completely when the dimmer is off, otherwise the LEDs will FLASH; data sheet says 1uF but I recommend 0.68uF to avoid flashing at turn off under all operating conditions

$C_{BP} := 0.68\mu F$

Pin 2 VDD: Current thru the internal Zener on VDD (21Vmin, 25Vmax) will initiate an OVP response so plan bias windings accordingly! UVLOon = 8V. Use a smoothing resistor to prevent peak charging due to leakage inductance spike, if this resistor is too high, such as 40 Ohms, the LEDs flicker. Connected to source of FET driven by VZ for rapid charging of VDD capacitor

$VDD := V_{BIAS}$

$C_{VDD} := 10 \cdot C_{BP}$

$C_{VDD} = 6.8\,\mu F$

$C_{VDD} := 6.8\mu F$ **Enter the actual value of the capacitor used**

$R_{VDD} := 15\Omega$ **For smoothing of spikes that would peak charge the capacitor**

$$V_{Dbias} := V_{OUT} \cdot \frac{N_{PS}}{N_{PB}} + \frac{V_{INmax}}{N_{PB}} + V_{BIAS}$$

$V_{Dbias} = 39.446\,V$ **Required minimum blocking voltage for bias diode**

Pin 3 GND: Use as direct return for noise sensitive pins, layout using star connection

Pin 4 VD: Valley Detect Input. Used to detect valley voltage of the Aux winding with a resistor divider in order to start the next switching cycle. Worst case, peak voltage must be less than 6V and a minimum of 50uA must be sourced from VD to set the valley detect circuitry.

$I_{VDmin} := 50\mu A$ **50uA for worst case BUT better efficiency if you use 30uA and should work over operating range...**

$$\frac{V_{BULKmin}}{N_{PB}} = 4.351\ V$$

$$R_{VD1} := \frac{1}{N_{PB}} \cdot \frac{V_{BULKmin}}{I_{VDmin}}$$

$R_{VD1} = 87.022\,k\Omega$

$R_{VD1} := 86.6k\Omega$ **Enter the actual value of the standard value used**

$$I_{VDmin} := \frac{V_{BULKmin}}{N_{PB} \cdot R_{VD1}}$$

$I_{VDmin} = 50.243\,\mu A$

R_{VD2}: primary criteria of this resistor is to keep VD less than its Abs Max rating if V_{OVP} triggered on VDD so part not compromised, then check that the voltage on VD is less than 6V under normal bias conditions:

$VDD_{OVPmax} := 25V$

$V_{VDmax} := 6V$

$$V_{VDmax} = \frac{V_{OVPmax} \cdot R_{VD2}}{R_{VD1} + R_{VD2}}$$

$$R_{VD2} := \frac{V_{VDmax} \cdot R_{VD1}}{VDD_{OVPmax} - V_{VDmax}}$$

$R_{VD2} = 27.347\,k\Omega$

$R_{VD2} := 27.4k\Omega$ **Enter the actual value of the standard value used**

$$V_{VD} := \frac{V_{BIAS} \cdot R_{VD2}}{R_{VD1} + R_{VD2}}$$

$V_{VD} = 2.412\ V$ **well below the 6V maximum recommended value for normal operating range**

$$V_{LEDovp} := \frac{VDD_{OVPmax} \cdot N_{PB}}{N_{PS}} - V_{Fdiode}$$

$V_{LEDovp} = 30.623\ V$

$$V_{VDovp} := \frac{VDD_{OVPmax} \cdot R_{VD2}}{R_{VD1} + R_{VD2}}$$

$V_{VDovp} = 6.009\ V$ **Verify that VD stays below 7V ABS MAX during OVP condition**

Can add a capacitor to this pin to tweak ZVS...if needed

Pin 5 ISO: Inverting input to the secondary side current sense comparator and isolation transformer buffer. This pin is driven by the Gate drive signal from the PWM. In non-isolated designs this pin would be connected to GND. When configured for isolated sensing, ISO is connected directly to the signal transformer. When the GATE signal goes high, ISO is shorted to ground, capacitor on CS will hold the voltage on CS during this time for the sample and hold function.

Pin 6 CS: LED current sense feedback and positive input terminal of the transconductance error amplifier. EVM uses isolated current sense. Corner frequency of LC averaging must be well below the minimum switching frequency of the controller, set to half the minimum frequency. Must use a high enough inductance so that the capacitor is relatively small and does not slow down the dynamics of the circuit. Using a higher inductance results in better performance particularly at low currents

Secondary side coupling capacitor selected first, standard value, much less than 1uF

$C_{CSsec} := 0.22\mu F$

Corner frequency of the LC circuit set to 1/2 the minimum switching frequency

$$f_{LC} := \frac{f_{SWmin}}{2}$$

$f_{LC} = 12.498\,kHz$

$$\frac{1}{2\cdot\pi\cdot\sqrt{L_{CS}\cdot C_{CSsec}}} = f_{LC}$$

$$L_{LC} := \frac{1}{4\cdot C_{CSsec}\cdot f_{LC}^{2}\cdot\pi^{2}}$$

$L_{LC} = 737.161\,\mu H$

$L_{CS} := 450\mu H$ **Available value: must be as high as possible for adequate opertion at minimum dimming**

$$f_{LCactual} := \frac{1}{2\cdot\pi\cdot\sqrt{L_{CS}\cdot C_{CSsec}}}$$

$f_{LCactual} = 15.996\,kHz$

Primary side capacitor sized for half secondary side for sample and hold circuit

$$C_{CSpri} := \frac{C_{CSsec}}{2}$$

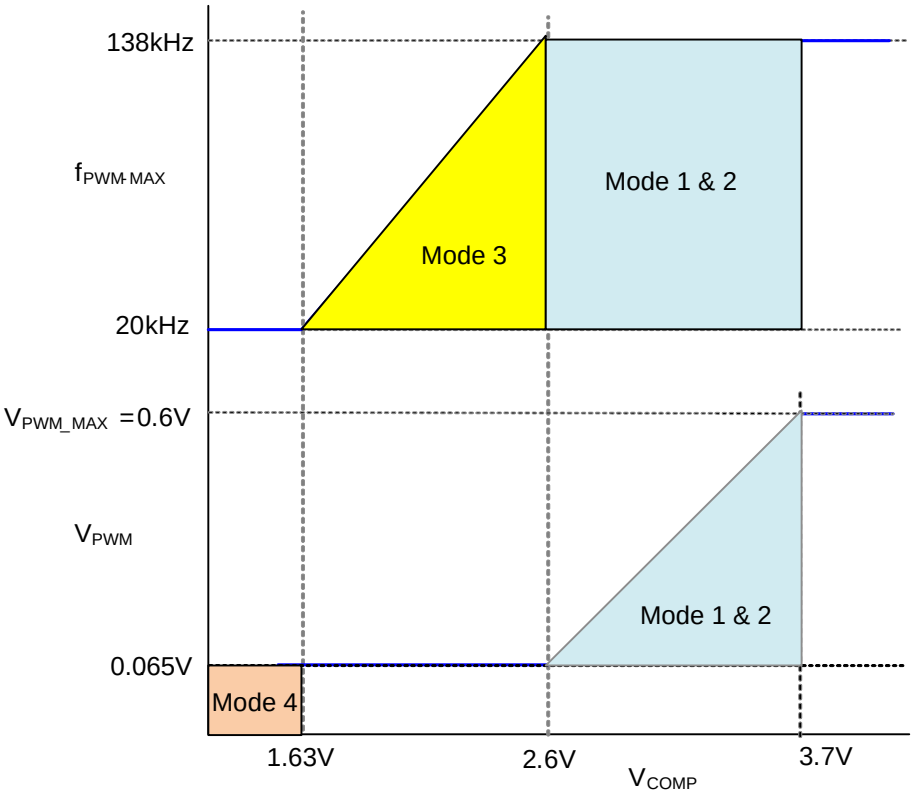
$C_{CSpri} = 0.11\,\mu F$

$C_{CSpri} := 0.1\mu F$

$$\frac{1}{2\cdot\pi\cdot\sqrt{L_{CS}\cdot C_{CSpri}}} = 23.725\,kHz$$

Pin 7 COMP: Average current mode control loop compensation output, needs only a dominant pole. Reccomendation is 10nF to 1uF, the higher the value will result in higher output line frequency ripple

$C_{COMP} := 33nF$



Pin 8 LP: sets pole for DTC low pass filter. A capacitor to ground will set the response time of the dimming level detection so want value to be big enough to minimize line frequency ripple but not too big to adversely effect the response time. ABS MAX is 7.7V.

$C_{LP} := 0.22\mu F$ **Recommendation is 220nF < C_{LP} < 1uF.**

the LP voltage will be converted to 0.2V to 0.4V when between 1V (33% triac conduction) to 1.98V (66% conduction) which is internally set

Pin 9 MIN: sets the minimun LED current during dimming,

$$I_{LEDmin} := \frac{I_{LED}}{25}$$ **Set for a 25:1 current range**

$I_{LEDmin} = 14.815\,mA$

$V_{CS\_min} := R_{LEDsense} \cdot I_{LEDmin}$

$V_{CS\_min} = 4\,mV$

$$R_{MIN} := \frac{225V \cdot \Omega}{V_{CS\_min}}$$

$R_{MIN} = 56.25\,k\Omega$

$R_{MIN} := 56.2k\Omega$ **Enter the actual value of the standard value used**

$$I_{LEDmin} := \frac{250V \cdot \Omega}{R_{LEDsense} \cdot R_{MIN}}$$

$I_{LEDmin} = 16.476\,mA$ **minimum LED current is only achieved with dimmers that can actually dim this low**

Pin 10 SEN: Dimmer sense input, used in conjunction with DTC which adds a weak bleeder when the SEN pin determines the rectified line voltage falls to 50V to discharge SEN capacitor, then a stronger bleeder kicks in at 10V to load the triac. Two 1MΩ resistor in series for top resistor divider.

$R_{SEN1} := 2 \cdot 1.00M\Omega$

$V_{ACweakbleeder} := 50V$ **May need to adjust this for a higher threshold depending upon dimmer performance, some dimmers have enough ripple that would prevent SEN from falling below 1V. Had to adjust this value to kick in at 70V instead of 50V to accommodate all of the dimmers tested.**

$V_{SEN\_Hmin} := 4.75V$

$$\frac{V_{ACweakbleeder} \cdot R_{SEN2}}{R_{SEN1} + R_{SEN2}} = V_{SEN\_Hmin}$$

$$R_{SEN2} := \frac{R_{SEN1} \cdot V_{SEN\_Hmin}}{V_{ACweakbleeder} - V_{SEN\_Hmin}}$$

$R_{SEN2} = 209.945\,k\Omega$

$R_{SEN2} := 162k\Omega$ **One dimmer had enough leakage that SEN did not go below 1V and flickering resulted so threshold was changed to 70V to initiate discharging the SEN capacitors sooner**

$V_{SEN\_Hmax} := 5.25V$

$$V_{ACweakbleeder} := V_{SEN\_Hmax} \cdot \frac{R_{SEN2} + R_{SEN1}}{R_{SEN2}}$$

$V_{ACweakbleeder} = 70.065\ V$

Pin 11 VZ: Zener voltage clamp for start up from bulk voltage, and provides drive for DTC FET which is used to rapidly charge the VDD capacitor, need I_{VZ} at least 10µA worst case to start up and 10mA for DTC. A 5.1V zener is needed on VZ to prevent the driver from failing input surge testing. This is because the VZ pin is too weak to hold down the gate of the DTC FET during surge testing.

$V_{VZ} := 13V$

$I_{VZ} := 10\mu A$

$I_{DTC} := 10mA$

$I_{BASE} := \frac{I_{DTC}}{100}$

$R_{VZ} := \frac{V_{INmin} - V_{VZ}}{I_{BASE} + I_{VZ}}$

$R_{VZ} = 2.196\,M\Omega$

$R_{VZ} := 2M\Omega$

Pin 12 DTC: Dimmer trigger circuit input. Connected to the source of NFET cascode device and is used to load the triac dimmer, a 205 Ohm series resistor added to limit the current

Pin 13 PGND: Power ground of IC, star connect to GND

Pin 14 PCS: Primary current sense (refer to current sense resistor section). Despite having an internal 200ns blanking time to avoid false tripping of the comparator due to capacitive charge spikes, an additional blanking time is needed to prevent flickering on designs that require deep dimming. If the on-time is about the same as the internal blanking time, the part will switch off as soon as the internal blanking time is over which would be at deep dimming and result in flickering. Set blanking time for approximately 1.5us to start. Too low and will flicker at deep dimming, too long and output current regulation will be too high and line regulation will not be as tight as it should be

$t_{LEB} := 1.5\mu s$

$C_{LEB} := 3.3nF$ **maximum recmmended value**

$R_{LEB} := \frac{t_{LEB}}{C_{LEB}}$

$R_{LEB} = 454.545\ \Omega$

$R_{LEB} := 511\Omega$

Pin 15 TDD: Triac dimmer detect, drives the bypass FET on the passive valley fill circuit when dimming is detected. Connect directly to Gate of VF switch

Pin 16 GATE: connect directly to the gate of the primary side switch