SM72442

Application Note 2124 Power Circuit Design For SolarMagic SM3320

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Power Circuit Design For SolarMagic™ SM3320

National Semiconductor
Application Note 2124
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Overview of SolarMagic MPPT with Panel-Mode Capability

National Semiconductor's SolarMagic technology, the state-of-the-art maximum power point tracking (MPPT) chipset, improves energy harvest of each individual Photovoltaic (PV) panel under real world conditions. To further optimize the SolarMagic performance, National Semiconductor developed the second generation chipset, anchored by the MPPT chip SM72442, capable of intelligent maximum power tracking (MPPT) as well as direct power Panel-Mode (PM). *Figure 1* shows a typical architecture of a PV system employing a SolarMagic distributed MPPT/PM solution to enhance the system performance. In additional to employing a DC/DC converter for MPPT by each PV module, a direct Panel-Mode switch is introduced to be able to bypass the DC/DC converter in appropriate operating conditions. With the exception of the MPPT/PM enhancements, almost all merits of the first generation MPPT chipset are retained. Besides, it offers the following additional advantages.

- It replaces the interleaved Buck and Boost switching modes and provides an almost lossless energy harvest solution when the maximum power point voltage of the host PV panel is nearly equal to the DC/DC converter's output voltage. Instead of incurring power processing losses, the MPPT/PM controller will shutdown the switching of the DC/DC converter, and turn on the PM switch to directly extract power from the PV panel, thereby achieving almost lossless energy harvest.
- It offers a backup solution to achieve DC/DC converter fault protection. When the DC/DC converter fails, though very rare, to process power, the MPPT/PM controller will turn-on the PM switch, allowing the host PV panel to be continually harvested rather than being blocked out of service.

Shown in *Figure 1*, several MPPT/PM enhanced modules are connected in series by their outputs, forming a string circuit. Multiple strings are parallel connected via blocking diodes to establish an MPPT/PM enhanced PV array, feeding power to the dc-ac power inverter which may be tied to the utility grid.

The inverter operates by regulating its input dc voltage such that power intake from the PV array will be transferred to the grid instead of being stored in the dc link shunt capacitors. The regulated inverter input dc voltage, often referred to as the dc link voltage, can be considered constant, thus imposing a design constraint for SolarMagic converters.

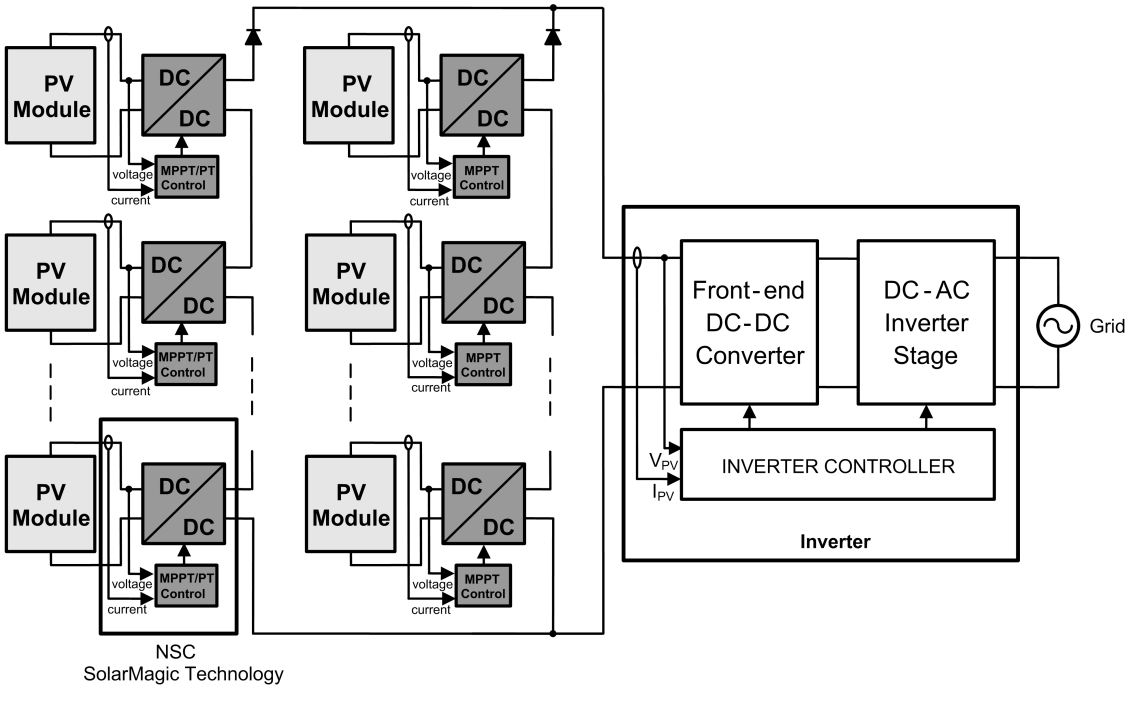

FIGURE 1. SolarMagic MPPT/PM Enhanced PV System Architecture

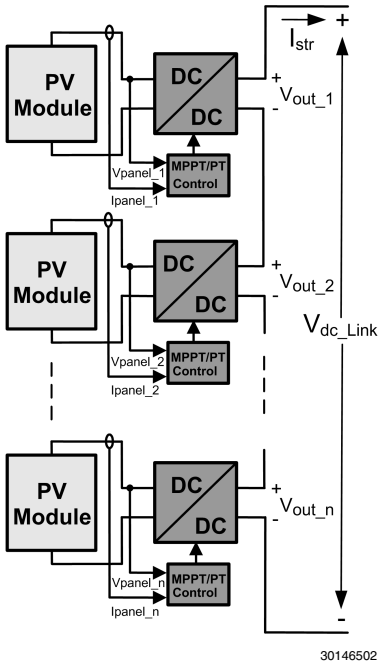

FIGURE 2. A String of MPPT/PM Enhanced PV Modules

Specifically, each converter's output voltage is a portion of the dc link voltage. Refer to *Figure 2*, which shows a single string tied to the inverter. Assuming the k-th panel in the string of "n" modules produces a power of Pk, where k = 1, 2, …n, then the total power harvested from the string is determined by,

$$P_{str} = \sum_{k=1}^{n} P_k \quad (1)$$

Because the converters in the string are series connected, they all have the same output current, the string current, I_{str}, which is given by

$$I_{str} = \frac{P_{str}}{V_{dc\_Link}} \quad (2)$$

Therefore, the output voltage of th k-th converter is governed by

$$Vout_k = \frac{P_k}{P_{str}} \bullet V_{dc\_Link} \quad (3)$$

On the other hand, each PV panel, as a power source, is desired to operate at its maximum power point, at which the panel terminal voltage is the maximum power point voltage Vmpp. This requires that each SolarMagic DC/DC converter shown in *Figure 1* should be controlled such that it can establish its input voltage to track the panel's Vmpp. This imposes another design constraint for the SolarMagic converter.

For the k-th module, the converter's input voltage should be

$$Vin_k = Vmpp_k \quad (4)$$

Equation 2 and *Equation 3* indicate the voltage conditions that the SolarMagic converter should be operated with.

In a string, when a converter loses its power due to heavy shading over the host PV panel or failure in either the panel or the DC/DC converter, it may block the string current. The solution is to employ an output bypass diode, as shown in *Figure 3*. During normal operation the output bypass diode is reverse biased, and while in converter shutdown mode the diode becomes forward biased continues the string current to keep the string in service.

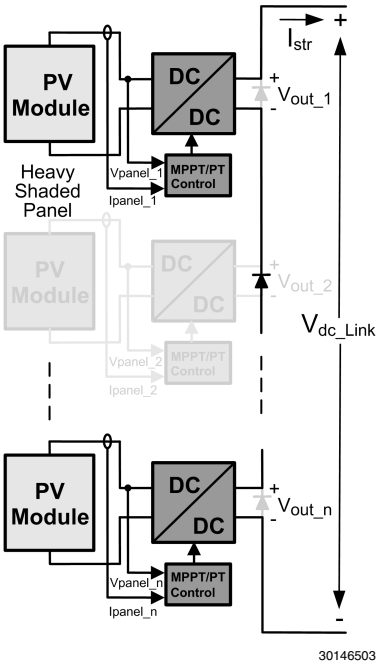

FIGURE 3. Output Bypass Diode Continues the String Current

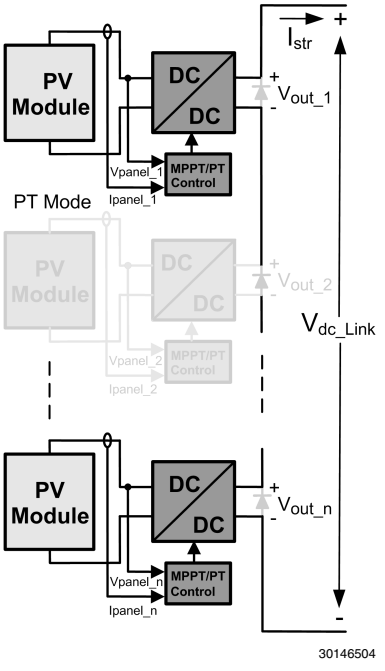

FIGURE 4. Panel Mode Offering Almost Lossless Energy Harvest

Figure 4 illustrates a scenario when the second PV module in the string operates in panel mode. More modules or the entire string may operate in panel mode when the panel mode conditions are valid. In panel mode, the DC/DC converter is shutdown to eliminate the switch-mode power conversion losses. The power produced by the host PV panel is almost losslessly harvested via the PM switch. Note that the PM switch may also be engaged as a fault protection mechanism to continue the power production by the host PV panel. These fault conditions may be over-current, over-temperature, or converter stage failure.

Power Converter Topology Selection

It is clear that the SolarMagic converter is required to establish the link between the two voltages defined by *Equation 2* and *Equation 3*. In reality, for a given PV system, these two voltages will vary with sun light irradiation conditions perceived by each PV module or other factors. The converter should be flexible to cope with these variations, namely able to operate in all of the following conditions: (i) Vin < Vout; (ii) Vin = Vout; (iii) and Vin>Vout. In other words, the converter should be able to boost up or buck down the input voltage. This leads to the selection of a four switch Buck and Boost converter topology with PM switch. The PM switch can establish an almost lossless direct link to the string.

Figure 5 shows a Buck-and-Boost converter topology with PM switch. It consists of the following components:

(i) Power Inductor L1

(ii) Buck (BK) switch leg including Q1 and Q2

(iii) Boost (BST) switch leg including Q3 and Q4

(iv) Input and Output filter capacitors Cin and Cout

(v) Output bypass diode D1

(vi) PM switch implemented with common-gate and common-source MOSFETs Q5A and Q5B

Theoretically Q2 and Q4, the two synchronous rectifiers, can be replaced with rectifier diodes without affecting the operating function. The circuit seems simpler, but efficiency-wise the diode will cause more conduction losses than the synchronous rectifier, making the use of a diode prohibitive in the converter legs.

The output bypass diode D1 is employed to continue the string current when its host PV model losses power such as in heavy shading conditions. During normal energy harvest, D1 will remain reverse biased.

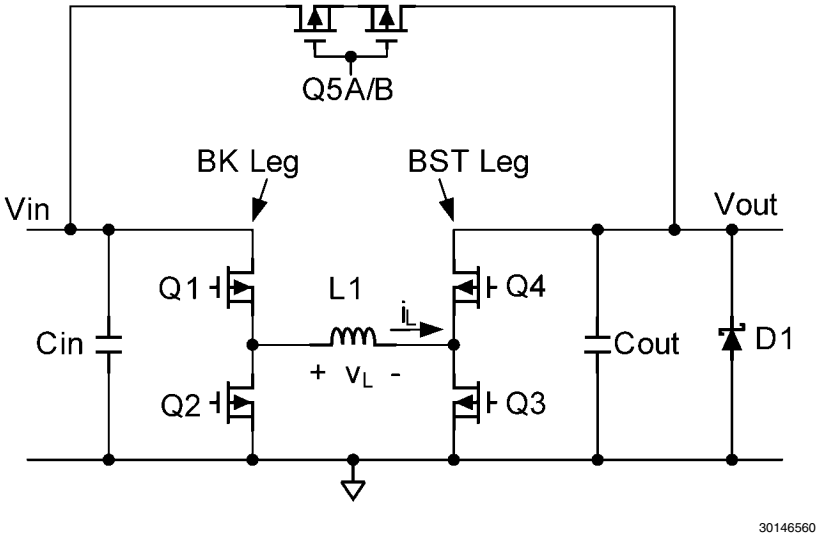

FIGURE 5. Buck-and-Boost Converter Topology with Panel Mode Switch

Operating Principle and Power Converter Design Equations

Based on real time assessment of the operating conditions, the SolarMagic MPPT/PM controller will dynamically determine an optimal mode among the three, so as to operate the converter to track the maximum power point of the PV panel. When the optimal operating condition falls into a narrow window that Vin and Vout are within about ±2% of each other, the panel mode is engaged to take the advantage of the almost lossless energy harvest feature. In panel mode as shown in *Figure 6*, Q5A/B remains ON while the DC/DC converter shuts down, establishing a direct link between the PV panel output and the string. Note that the panel mode replaces the interleaved Buck and Boost modes in the first generation SolarMagic SM1230 solution with the SM72441 MPPT control IC.

When the panel mode is not the optimal operating condition, the MPPT/PM controller will turn-off PM switches and engage the DC/DC converter for maximum power tracking. In a conventional Buck-and-Boost converter, switching of the diagonal switches is synchronized. Namely Q1 and Q3 are turned on and off at the same time. So are Q2 and Q4. In SolarMagic applications, the switching sequence of the four switches in *Figure 5* is different from the conventional Buck-and-Boost converter. The SolarMagic converter has three operating modes, which are the buck-only mode (BK); the boost-only mode (BST); and the buck-boost-interleaved mode (BB). Based on real time assessment of the operating conditions, the SolarMagic MPPT/PM controller will dynamically determine an optimal mode to operate the converter in order to track the maximum power point of the PV panel.

Generally, when the PV panel's Vmpp is lower than about 98% of Vout defined in *Equation 2*, the controller will run the converter in the BK mode. *Figure 7*a shows the equivalent circuit of BK mode, where only Q1 and Q2 are switching, while Q3 remains OFF and Q4 stays ON.

When the PV panel's Vmpp is greater than about 102% of the output voltage defined in *Equation 2*, the controller will run the converter in the BST mode. *Figure 7*b shows the equivalent circuit of BST mode. Only Q3 and Q4 are switching, while Q2 remains OFF and Q1 stays ON.

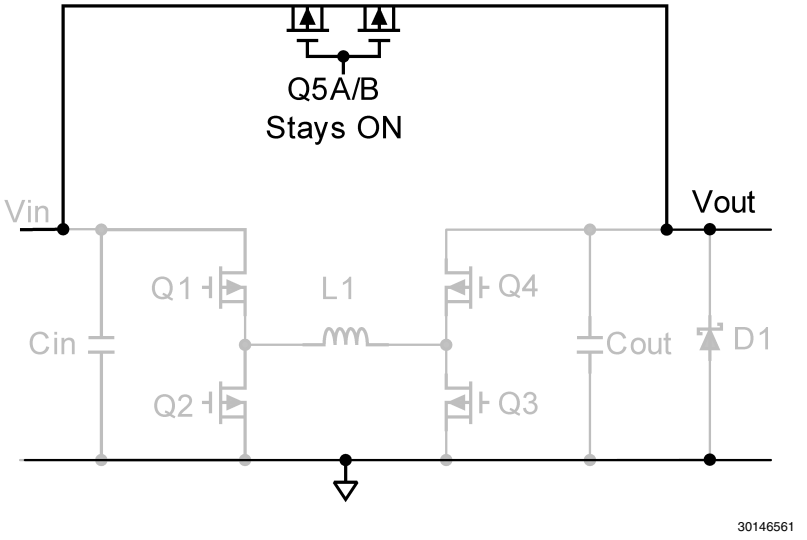

FIGURE 6. Panel Mode

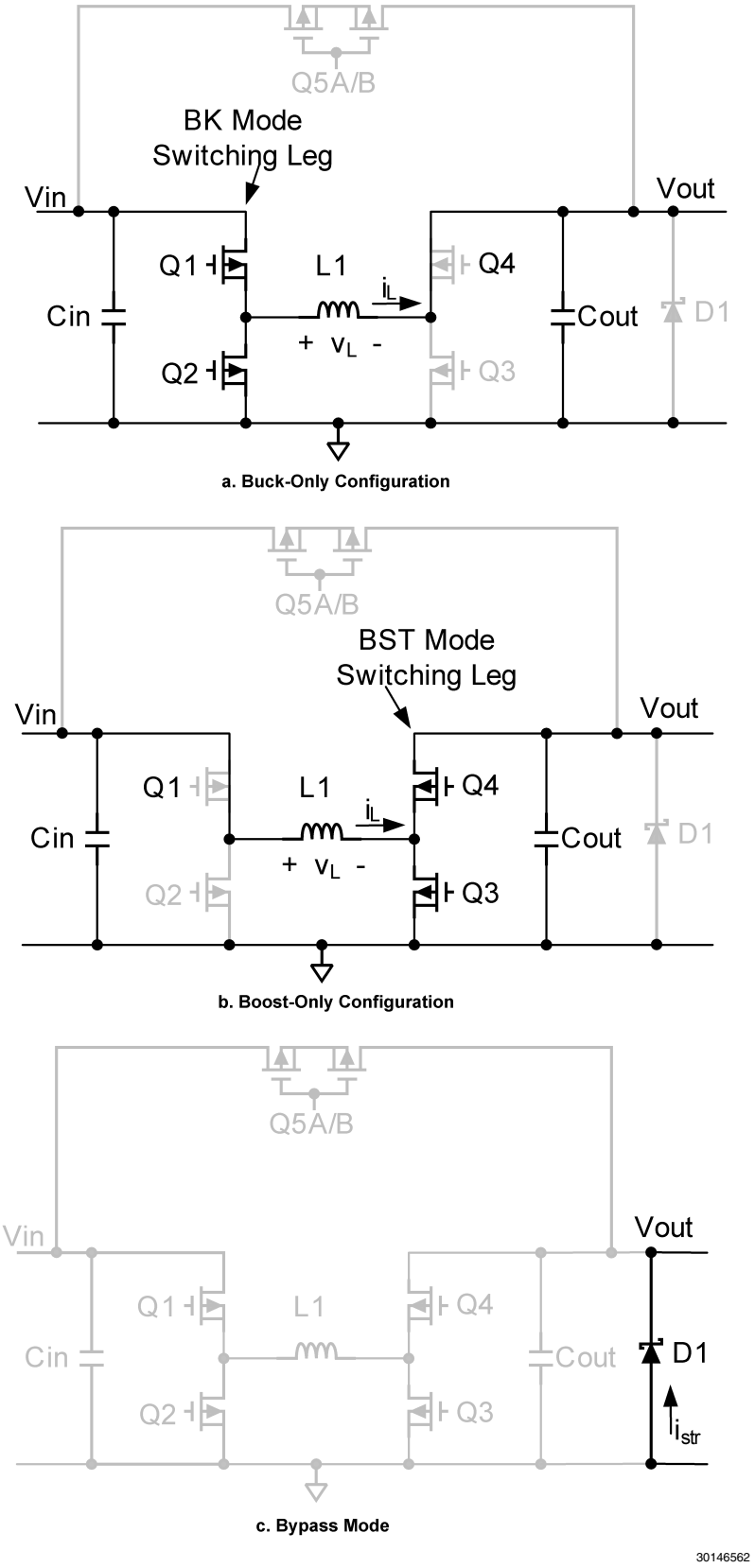

FIGURE 7. Buck-Only, Boost-Only and Output Bypass Configurations

For convenience in discussion, the following assumptions are made:

(i) The inductor L1 is an ideal inductor. Its inductance is constant. Its equivalent resistance is negligible.

(ii) The input and output capacitors are ideal capacitors. Their capacitances are constants. Their equivalent resistances are negligible.

(iii) The inductor and capacitors form an ideal LC filter, such that the input current ripples and output voltage ripples are negligible.

(iv) Q1 through Q4 are ideal switches. They can be switched ON and OFF instantaneously, and their conduction resistance Rds (on) is negligible.

(v) The gate drive dead times between Q1 and Q2, and between Q3 and Q4, are negligible.

(vi) Other power losses in the converter are negligible.

1. BK Mode

Figure 8 shows key waveforms of the converter of *Figure 5* when it operates in BK mode (equivalent to *Figure 7*a). Q1 and Q2 are switched complementarily. The voltage across the inductor, v_L, is (Vin-Vout) when Q1 is ON, and (-Vout) when Q1 is OFF. For steady state, the inductor's volt-second product must be balanced each switching cycle, namely,

$$(Vin - Vout) \times D + (-Vout) \times (1 - D) = 0 \quad (5)$$

Where D is the duty cycle of the Q1.

Substituting the PV panel voltage Vmpp from *Equation 3* into *Equation 4*, one will obtain the converter duty cycle in BK mode, which is

$$D_{BK} = \frac{Vout}{Vmpp} \quad (6)$$

Note: *Equation 5* indicates the duty cycle required to establish the power link in BK mode between the PV panel maximum voltage (Vmpp) and the shared system dc link voltage Vout as defined in *Equation 2*.

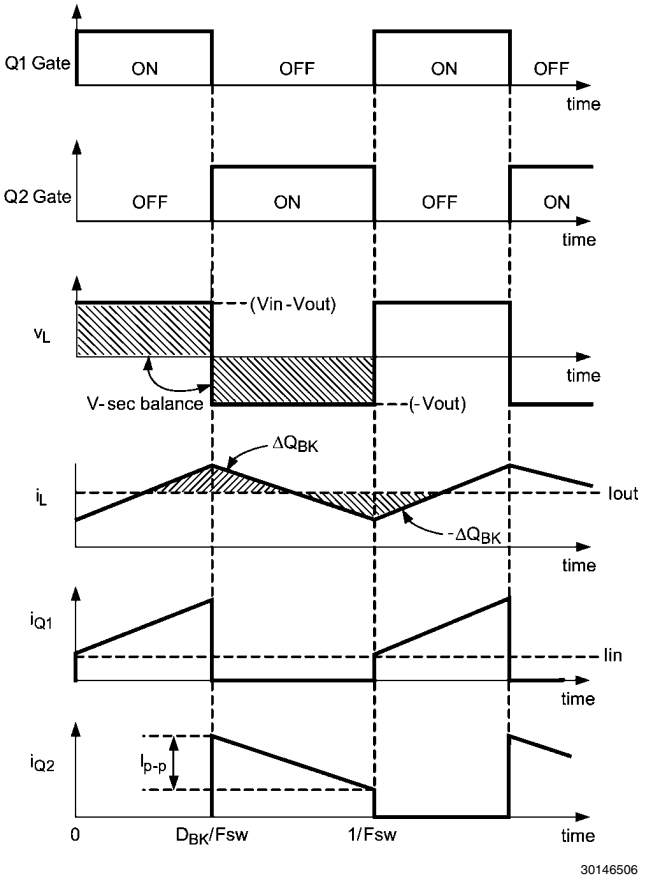

FIGURE 8. Buck-Only Key Waveforms

2. BST Mode

Figure 9 shows key waveforms of the converter of *Figure 5* when it operates in BST mode (equivalent to *Figure 7*b). In BST mode, Q3 and Q4 are switched complementarily. The voltage across the inductor, v_L, is Vin when Q3 is ON, and (Vin-Vout) when Q3 is OFF. For steady state, the inductor's volt-second product must be balanced each switching cycle, namely,

$$\text{Vin} \times D + (\text{Vin} - \text{Vout}) \times (1 - D) = 0 \tag{7}$$

Where D is the duty cycle of the Q3.

Substituting the PV panel voltage Vmpp from *Equation 3* into *Equation 6*, one will obtain the converter duty cycle in BST mode, which is

$$D_{BST} = \frac{\text{Vout} - \text{Vmpp}}{\text{Vout}} \tag{8}$$

Note: *Equation 7* indicates the duty cycle required to establish the power link in BST mode between the PV panel maximum voltage (Vmpp) and the shared system dc link voltage Vout as defined in *Equation 2*.

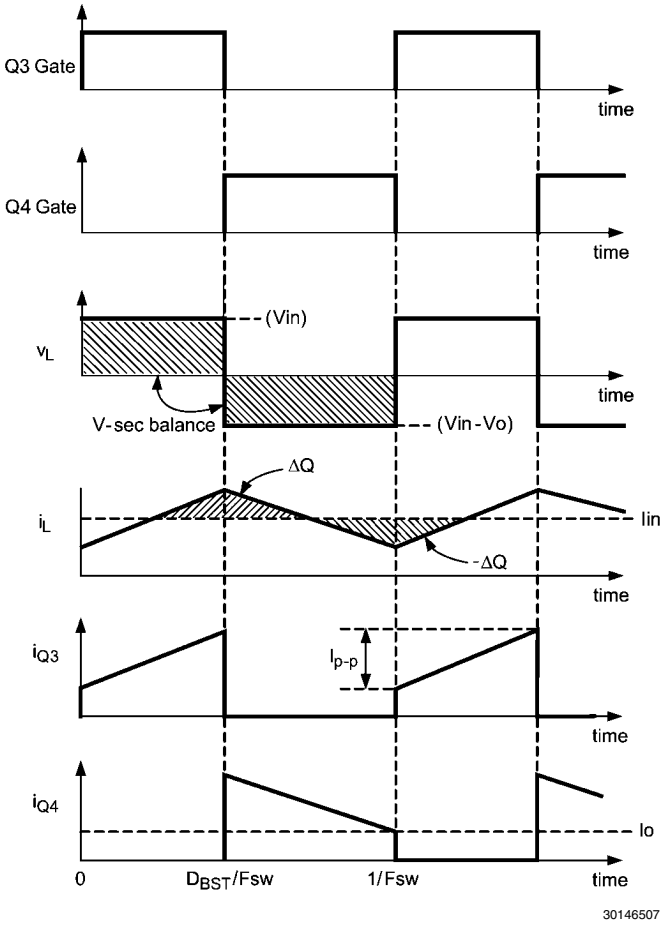

FIGURE 9. Boost-Only Key Waveforms

3. Converter Power Circuit Design Equations

Assuming the converter is operating at the panel maximum power point, Pmpp, and the converter internal losses are negligible. The following can be obtained.

$$\begin{cases} Iin = \dfrac{Pmpp}{Vmpp} = Impp \\ Iout = \dfrac{Pmpp}{Vout} \end{cases} \tag{9}$$

3.1 Inductor Current

Now let us first look at the inductor current. In BK mode (refer to *Figure 7*a and *Figure 8*), when Q1 is on, (Vin-Vout) is applied across the inductor L1, thereby its current will rise linearly. When Q2 is on, (-Vout) is applied across L1, thereby the current will decrease linearly. This leads to a saw-tooth current waveform as shown in *Figure 8*.

Similarly, for BST mode (refer to *Figure 7*b and *Figure 9*), when Q3 is on, (Vin) is applied across the inductor L1, thereby its current will rise linearly. When Q4 is on, (Vin-Vout) is applied across L1, thereby the current will decrease linearly. This leads to a saw-tooth current waveform as shown in *Figure 9*.

Obviously the inductor ripple current is determined by:

$$I_{p-p} = \begin{cases} \dfrac{Vout}{L1} \bullet \dfrac{1 - D_{BK}}{Fsw} & (BK\_Mode) \\ \dfrac{Vmpp}{L1} \bullet \dfrac{D_{BST}}{Fsw} & (BST\_Mode) \end{cases} \tag{10}$$

Since the averaged current through the inductor is Iout in BK mode, and Iin in BST mode, the peak inductor current is given by

$$I_{pk} = \begin{cases} Io + \dfrac{Vout}{2 \bullet L1} \bullet \dfrac{1 - D_{BK}}{Fsw} & (BK\_Mode) \\ Iin + \dfrac{Vmpp}{2 \bullet L1} \bullet \dfrac{D_{BST}}{Fsw} & (BST\_Mode) \end{cases} \tag{11}$$

3.2 Capacitor Ripple Voltage

The area of the shaded triangles shown in the i_L curves in *Figure 8* and *Figure 9* are equal to the total electric charge exchanged in and out of the input or output capacitors, respectively, in one switching cycle. The net charge exchange in the capacitor within a switching cycle is thus determined by

$$\begin{cases} \Delta Q_{BK} = \dfrac{1}{8} \bullet \dfrac{I_{p-p}}{Fsw} = \dfrac{(1 - D_{BST}) \bullet Vout}{8 \bullet Fsw^2 \bullet L1} & (BK\_Mode) \\ \Delta Q_{BST} = \dfrac{1}{8} \bullet \dfrac{I_{p-p}}{Fsw} = \dfrac{D_{BST} \bullet Vmpp}{8 \bullet Fsw^2 \bullet L1} & (BST\_Mode) \end{cases} \tag{12}$$

Therefore, the input and output ripple voltages can be estimated by

$$\begin{cases} \Delta vout_{pk-pk} = \dfrac{\Delta Q_{BK}}{Cout} = \dfrac{(Vmpp - Vout) \bullet Vout}{8 \bullet Fsw^2 \bullet L1 \bullet Cout \bullet Vmpp} & (BK\_Mode) \\ \Delta vin_{pk-pk} = \dfrac{\Delta Q_{BST}}{Cin} = \dfrac{Vout - Vmpp}{8 \bullet Fsw^2 \bullet L1 \bullet Cin} & (BSTMode) \end{cases} \tag{13}$$

3.3 MOSFET Currents

The peak current through each MOSFET is determined by *Equation 10*. Now let us find out the rms current of each MOSFET.

Referring to the waveforms in *Figure 8* and *Figure 9*, the rms current through Q1 can be approximated as

$$I_{rms\_Q1} = \begin{cases} Iout \bullet \sqrt{D_{BK}} & (BK\_Mode) \\ Impp & (BST\_Mode) \end{cases} \quad (14)$$

Substituting *Equation 5* and *Equation 8* into *Equation 13*, one can obtain

$$I_{rms\_Q1} = \begin{cases} \dfrac{Pmpp}{\sqrt{Vout \bullet Vmpp}} & (BK\_Mode) \\ Impp & (BST\_Mode) \end{cases} \quad (15)$$

Similarly, the rms current through Q2 is given by

$$I_{rms\_Q2} = \begin{cases} \dfrac{Pmpp}{Vout} \bullet \sqrt{1 - \dfrac{Vout}{Vmpp}} & (BK\_Mode) \\ 0 & (BST\_Mode) \end{cases} \quad (16)$$

The rms current through Q3 is given by

$$I_{rms\_Q3} = \begin{cases} \dfrac{Pmpp}{Vout} & (BK\_Mode) \\ \dfrac{Pmpp}{Vmpp} \bullet \sqrt{\dfrac{Vout - Vmpp}{Vout}} & (BST\_Mode) \end{cases} \quad (17)$$

And the rms current through Q4 is given by

$$I_{rms\_Q4} = \begin{cases} 0 & (BK\_Mode) \\ \dfrac{Pmpp}{\sqrt{Vout \bullet Vmpp}} & (BST\_Mode) \end{cases} \quad (18)$$

The worst case values defined in through *Equation 17* define the extreme requirements the power components need to meet.

Power Converter Component Selection Procedure

Step 1: PV Panel Characteristics

To select the components for the power circuit of the converter shown in *Figure 5*, we first need to know the targeted PV panel's electrical characteristics, including the following:

- **P_{max}:** PV panel maximum power level
- **Voc_{min}, Voc_{max}:** Minimum and Maximum PV panel open circuit voltages
  Applicable absolute maximum Voc is limited either by SolarMagic driver IC's 100V maximum rating, or by application specified limit, whichever is lower.
- **$Vmpp_{min}$, $Vmpp_{max}$:** Minimum and Maximum MPP voltage. May sometimes be approximated by,
  $Vmpp_{max} \cong 0.78 \times Voc_{max}$;
  $Vmpp_{min} \cong 0.78 \times Voc_{min}$.
- **Isc_{max}:** PV panel maximum short circuit current.
- **$Impp_{min}$, $Impp_{max}$:** Minimum and Maximum PV panel MPP current. Obviously,
  $Impp_{min} = P_{max} / Vmpp_{max}$;
  $Impp_{max} = P_{max} / Vmpp_{min}$

These parameters define the power circuit's input specifications.

Step 2: Other Converter Specifications

The following additional parameters need to be determined, too, before selecting the components.

- **$Vout_{max}$:** Maximum output voltage.

Absolute maximum output voltage is limited either by SolarMagic driver IC's 100V maximum rating, or by application specified limit, whichever is lower.

- **$Vout_{min}$:** Minimum buck down voltage at full power, which may be determined by the following, whichever is smaller.
  $Vout_{min} = P_{max} / Iout_{max}$, as limited by the maximum output current limit,
  $Vout_{min}$ = Vdc_Link_min/n as limited by Inverter dc link voltage, where n is the number of PV modules to be installed in a string, and Vdc_lin_min is the minimum inverter dc link voltage for maximum power operation.
- **ΔVin_{p-p}:** Maximum peak-to-peak input ripple voltages
  Generally less than 5% of input dc voltage.
- **$\Delta Vout_{p-p}$:** Maximum peak-to-peak output ripple voltage.
  Generally less than 5% of the output voltage.
- **Fsw:** Switching frequency controlled by SolarMagic MPPT controller. The nominal Fsw is 200 kHz, with ±10% tolerance.
  Fsw_{min} = 180 kHz
  Fsw_{max} = 220 kHz

Step 3: Decide the Full Power BK and BST Duty Cycles

Since the power circuit components to be selected below need be able to support the worst operating conditions, which can be reflected in the worst case converter duty cycles , we need to determine (i) the minimum BK duty cycle that relates to the maximum voltage step down ratio from the input to the output; and (ii) the maximum BST duty cycle that corresponds to the maximum voltage step up ratio from the input to the output, both at maximum power. According to *Equation 5* and *Equation 7*, we can easily find that these worst case duty cycles are given by:

$$\begin{cases} D_{BK\_min} = \dfrac{Vout_{min}}{Vmpp_{max}} & (BK\_Mode) \\ D_{BST\_max} = \dfrac{Vout_{max} - Vmpp_{min}}{Vout_{max}} & (BST\_Mode) \end{cases} \tag{19}$$

Step 4: Select the Inductor L1, Input Capacitor Cin and Output Capacitance Cout.

In BK mode the inductor L1 teams up with Cout to fulfill an output L-C filter, and in BST mode it works with Cin to fulfill an input L-C filter. Because both the inductor and capacitors affect the filter performance, selections of L1, Cin and Cout are correlated. Selection trade-offs between the values of inductor and capacitors are normally required.

According to *Equation 9*, one can obtain the maximum inductor ripple current, as given by

$$I_{p-p\_max} = \begin{cases} \dfrac{Vout_{min}}{L1} \bullet \dfrac{1 - D_{BK\_min}}{Fsw_{min}} & (BK\_Mode) \\ & \text{whichever is greater.} \\ \dfrac{Vmpp_{min}}{L1} \bullet \dfrac{D_{BST\_max}}{Fsw_{min}} & (BST\_Mode) \end{cases} \tag{20}$$

A good design practice is to limit the inductor ripple current to below 30% of the maximum DC current, or the peak-to-peak ripple be 60% of the maximum DC current. Applying this constraint to *Equation 19*, the minimum inductance should satisfy the following:

$$\begin{cases} L1 \geq \dfrac{Vout_{min}^2}{0.6 \bullet P_{max}} \bullet \dfrac{1 - D_{BK\_min}}{Fsw_{min}} & (BK\_Mode) \\ \text{And} & \text{whichever is greater.} \\ L1 \geq \dfrac{Vmpp^2}{0.6 \bullet P_{max}} \bullet \dfrac{D_{BST\_max}}{Fsw_{min}} & (BST\_Mode) \end{cases} \tag{21}$$

In addition to the inductance value requirement, L1 should stay away from saturation at the peak current defined by *Equation 10*. Substituting the worst case values, the peak current that L1 needs to handle without being saturated is given by

$$I_{pk} = \begin{cases} \dfrac{P_{max}}{Vout_{min}} + \dfrac{Vout_{min}}{2 \bullet L1} \bullet \dfrac{1 - D_{BK\,min}}{Fsw_{min}} & (BK\_Mode) \\ & \text{whichever is greater.} \\ \dfrac{P_{max}}{Vmpp_{min}} + \dfrac{Vmpp_{min}}{2 \bullet L1} \bullet \dfrac{D_{BST\,max}}{Fsw_{min}} & (BST\_Mode) \end{cases} \tag{22}$$

The inductor windings are recommended to use multiple strand wires in order to reduce power losses.

Substituting the input and output ripple specification limits to *Equation 12*, and applying the worst case parameters obtained previously, we can obtain the minimum filter capacitance required to meet the ripple limits, as follows

$$\begin{cases} C_{out} \geq \dfrac{(Vmpp_{max} - Vout_{min}) \bullet Vout_{min}}{8 \bullet Fsw_{min}^{2} \bullet L1 \bullet Vmpp_{max} \bullet \Delta vout_{p\text{-}p}} \\ \\ C_{in} \geq \dfrac{Vout_{max} - Vmpp_{min}}{8 \bullet Fsw_{min}^{2} \bullet L1 \bullet \Delta vin_{p\text{-}p}} \end{cases} \tag{23}$$

Obviously, the capacitors' voltage rating should satisfy the following,

$$\begin{cases} V\_rating\_of\_C_{out} \geq Vout_{max} \\ \\ V\_rating\_of\_C_{in} \geq Voc_{max} \end{cases} \tag{24}$$

Seen from *Equation 22* that a greater valued L1 can reduce the need of capacitance of Cin and Cout, and vice versa. Trade-offs among the overall cost, size and availability are recommended in selecting L1, Cin and Cout.

Ceramic capacitors of X7R type are recommended for Cin and Cout. In addition, Cin and Cout can be a combination of multiple smaller valued capacitors connected in parallel instead of a single large valued one. Normally this approach can reduce the overall cost owing to component availability, unit price, and procurement lead time.

Step 5. Determine the Power MOSFET Switches

Power MOSFETs are generally selected according to voltage rating, rms current requirement, and peak current. It is obvious that the voltage rating requirements of the four MOSFETs are determined by

$$\begin{cases} V\_rating\_of\_Q1 \geq Voc_{max} \\ V\_rating\_of\_Q2 \geq Voc_{max} \\ V\_rating\_of\_Q3 \geq Vout_{max} \\ V\_rating\_of\_Q4 \geq Vout_{max} \end{cases} \tag{25}$$

The peak current of the MOSFETs are all determined by *Equation 21*.

The RMS current of the four MOSFETs are determined, respectively, by substituting the worst case values into *Equation 14* through *Equation 17*, which yields the following:

$$I_{rms\_Q1} = \begin{cases} \dfrac{P_{max}}{\sqrt{Vout_{min} \bullet Vmpp_{max}}} & (BK\_Mode) \\ \\ \dfrac{P_{max}}{Vmpp_{min}} & (BST\_Mode) \end{cases} \quad \text{whichever is greater.} \tag{26}$$

$$I_{rms\_Q2} = \frac{P_{max}}{Vout_{min}} \bullet \sqrt{1 - \frac{Vout_{min}}{Vmpp_{max}}} \tag{27}$$

$$I_{rms\_Q3} = \begin{cases} \dfrac{P_{max}}{Vout_{min}} & (BK\_Mode) \\ \dfrac{P_{max}}{Vmpp_{min}} \bullet \sqrt{\dfrac{Vout_{max} - Vmpp_{min}}{Vout_{max}}} & (BST\_Mode) \end{cases} \quad \text{whichever is greater.} \tag{28}$$

$$I_{rms\_Q4} = \frac{P_{max}}{\sqrt{Vout_{max} \bullet Vmpp_{min}}} \tag{29}$$

In addition, a MOSFET's Rds(on) and gate charge are two other factors that need to be considered to reduce the overall power losses in the MSOFET. However, a lower Rds(on) MOSFET will generally have greater gate charge, therefore it may reduce conduction losses at the cost of increased switching losses. Besides, a lower Rds(on) MOSFET usually costs more than a higher Rds(on) MOSFETs at the same voltage and current ratings and package. Trade-offs among overall efficiency and cost are recommended in selecting the MOSFETs.

Step 6. Determine the Output Bypass Diode Obviously the output bypass diode must support a reverse voltage greater than the maximum output voltage. When it is in conduction mode, it should continue the maximum string current. Therefore, the ratings of the output bypass diode should meet the following requirements,

$$\begin{cases} V\_rating\_of\_D1 > Vout_{max} \\ I\_rating\_of\_D1 > \dfrac{P_{max}}{Vout_{min}} \end{cases} \tag{30}$$

A Schottky diode is recommended for the sake of minimal conduction losses in the diode when it is conducting. The conduction losses will turn into a thermal burden, thus a Schottky diode will help reduce the cooling requirement, and consequently the overall cost of the converter.

Step 7. Determine the PM Switch Selection

Step 7 is only required when utilizing the second generation MPPT controller SM72442 and it's panel mode function. When the converter is in panel mode, Q5A/B conducts the panel maximum power point current Impp. On the other hand, since the panel mode switch is also engaged in converter fault conditions, the PM switch should be able to conduct the maximum PV panel short circuit current Isc. Therefore, PM switches current rating should satisfy

$$I_{D\_Q5A} = I_{D\_Q5B} \geq I_{sc\_max} \tag{31}$$

When the converter is in panel mode, the maximum voltage across the PM switches is given by:

$$\begin{cases} V\_rating\_of\_Q5A = V\_rating\_of\_Q5B > Voc_{max} \\ \qquad\qquad\qquad\qquad\qquad\qquad \text{whichever is greater} \\ V\_rating\_of\_Q5A = V\_rating\_of\_Q5B > Vout_{max} \end{cases} \tag{32}$$

In order to minimize the conduction losses in Q5A/B, an ultra low Rds(on) FET meeting the rating requirements given in *Equation 30* and *Equation 31* should be selected.

Summary of Power Circuit Selection Guide

Table 1 summarizes key selection criteria of the SolarMagic Power Converter

TABLE 1.

Component	Value	Rating	Notes
L1	$\begin{cases} L1 \geq \dfrac{Vout_{min}^2}{0.6 \bullet P_{max}} \bullet \dfrac{1 - D_{BK\_min}}{Fsw_{min}} & (BK\_Mode) \\ \text{And} \\ L1 \geq \dfrac{Vmpp^2}{0.6 \bullet P_{max}} \bullet \dfrac{D_{BST\_max}}{Fsw_{min}} & (BST\_Mode) \end{cases}$ whichever is greater.	$I_{pk} = \begin{cases} \dfrac{P_{max}}{Vout_{min}} + \dfrac{Vout_{min}}{2 \bullet L1} \bullet \dfrac{1 - D_{BK\,min}}{Fsw_{min}} & (BK\_Mode) \\ \dfrac{P_{max}}{Vmpp_{min}} + \dfrac{Vmpp_{min}}{2 \bullet L1} \bullet \dfrac{D_{BST\,max}}{Fsw_{min}} & (BST\_Mode) \end{cases}$ whichever is greater.	Multi-strand windings in parallel to minimize power losses in winding.
Cin	$C_{in} \geq \dfrac{Vout_{max} - Vmpp_{min}}{8 \bullet Fsw_{min}^2 \bullet L1 \bullet \Delta vin_{p\text{-}p}}$	$V\_rating\_of\_C_{in} \geq Voc_{max}$	Recommending multiple ceramic capacitors.
Cout	$C_{out} \geq \dfrac{(Vmpp_{max} - Vout_{min}) \bullet Vout_{min}}{8 \bullet Fsw_{min}^2 \bullet L1 \bullet Vmpp_{max} \bullet \Delta vout_{p\text{-}p}}$	$V\_rating\_of\_C_{out} \geq Vout_{max}$	Recommending multiple ceramic capacitors.
Q1		$I_{rms\_Q1} = \begin{cases} \dfrac{P_{max}}{\sqrt{Vout_{min} \bullet Vmpp_{max}}} & (BK\_\ Mode) \\ \dfrac{P_{max}}{Vmpp_{min}} & (BST\_\ Mode) \end{cases}$ whichever is greater. $I_{pk} = \begin{cases} \dfrac{P_{max}}{Vout_{min}} + \dfrac{Vout_{min}}{2 \bullet L1} \bullet \dfrac{1 - D_{BK\,min}}{Fsw_{min}} & (BK\_Mode) \\ \dfrac{P_{max}}{Vmpp_{min}} + \dfrac{Vmpp_{min}}{2 \bullet L1} \bullet \dfrac{D_{BST\,max}}{Fsw_{min}} & (BST\_Mode) \end{cases}$ whichever is greater. $V\_rating\_of\_Q1 \geq Voc_{max}$	Trade-off between low Rds(on) and low gate charge MOSFETs needed to minimize overall power dissipation.

Component	Value	Rating	Notes
Q2		$$I_{rms\_Q2} = \frac{P_{max}}{Vout_{min}} \bullet \sqrt{1 - \frac{Vout_{min}}{Vmpp_{max}}}$$ $$I_{pk} = \begin{cases} \frac{P_{max}}{Vout_{min}} + \frac{Vout_{min}}{2 \bullet L1} \bullet \frac{1 - D_{BK_{min}}}{Fsw_{min}} & \text{(BK\_Mode)} \\ \frac{P_{max}}{Vmpp_{min}} + \frac{Vmpp_{min}}{2 \bullet L1} \bullet \frac{D_{BST_{max}}}{Fsw_{min}} & \text{(BST\_Mode)} \end{cases}$$ whichever is greater. $$V\_rating\_of\_Q2 \geq Voc_{max}$$	Trade-off between low Rds(on) and low gate charge MOSFETs needed to minimize overall power dissipation.
Q3		$$I_{rms\_Q3} = \begin{cases} \frac{P_{max}}{Vout_{min}} & \text{(BK\_ Mode)} \\ \frac{P_{max}}{Vmpp_{min}} \bullet \sqrt{\frac{Vout_{max} - Vmpp_{min}}{Vout_{max}}} & \text{(BST\_ Mode)} \end{cases}$$ whichever is greater. $$I_{pk} = \begin{cases} \frac{P_{max}}{Vout_{min}} + \frac{Vout_{min}}{2 \bullet L1} \bullet \frac{1 - D_{BK_{min}}}{Fsw_{min}} & \text{(BK\_Mode)} \\ \frac{P_{max}}{Vmpp_{min}} + \frac{Vmpp_{min}}{2 \bullet L1} \bullet \frac{D_{BST_{max}}}{Fsw_{min}} & \text{(BST\_Mode)} \end{cases}$$ whichever is greater. $$V\_rating\_of\_Q3 \geq Vout_{max}$$	Trade-off between low Rds(on) and low gate charge MOSFETs needed to minimize overall power dissipation.

Component	Value	Rating	Notes
Q4		$I_{rms\_Q4} = \frac{P_{max}}{\sqrt{Vout_{max} \bullet Vmpp_{min}}}$ $I_{pk} = \begin{cases} \frac{P_{max}}{Vout_{min}} + \frac{Vout_{min}}{2 \bullet L1} \bullet \frac{1 - D_{BK_{min}}}{Fsw_{min}} & \text{(BK\_Mode)} \\ \frac{P_{max}}{Vmpp_{min}} + \frac{Vmpp_{min}}{2 \bullet L1} \bullet \frac{D_{BST_{max}}}{Fsw_{min}} & \text{(BST\_Mode)} \end{cases}$ whichever is greater. $V\_rating\_of\_Q4 \geq Vout_{max}$	Trade-off between low Rds(on) and low gate charge MOSFETs needed to minimize overall power dissipation.
D1		$V\_rating\_of\_D1 > Vout_{max}$ $I\_rating\_of\_D1 > \frac{P_{max}}{Vout_{min}}$	Ultra-Low forward voltage drop Schottky diode preferred.
Q5A, Q5B		$\begin{cases} V\_rating\_of\_Q5A = V\_rating\_of\_Q5B > Voc_{max} \\ V\_rating\_of\_Q5A = V\_rating\_of\_Q5B > Vout_{max} \end{cases}$ whichever is greater $I_{D\_Q5A} = I_{D\_Q5B} \geq Isc_{max}$	Ultra-Low Rds(on) MOSFET preferred.

Notes

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