Design Review: A 300W, 300KHz Current-Mode Half-Bridge Converter with Multiple Outputs Using Coupled Inductors

by Roger Adair

TOPIC 6

Design Review: A 300W, 300KHz Current-Mode Half-bridge Power Supply with Multiple Outputs using Coupled Inductors

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Introduction

This paper gives a practical example of the design of an off-line switching power supply. The half-bridge topology is used with current mode control. Until recently this was considered an unstable combination, but a simple compensation circuit is now available and is described in this paper. This power supply has two outputs and uses a coupled inductor. Using a coupled inductor with a current mode controlled buck type topology is especially helpful, as will be explained later.

Specifications

Topology: Half Bridge

Mode: Current Mode

Output: 5V ± 1%, 10 to 50A, ripple v = 100mV pp max
15V ± 5%, 1A to 4A, ripple v = 200mv pp max

Frequency: 300KHz (600KHz oscillator)

Efficiency: 75%

Input: 110/220VAC

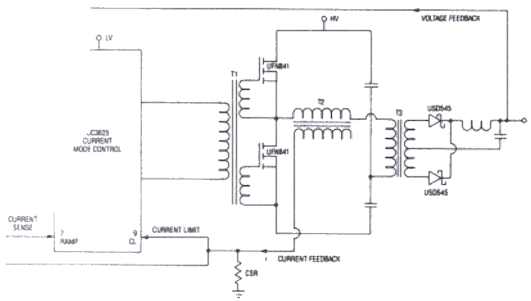

Figure 1. Simplified Schematic Showing Voltage Feedback and Current Mode Pat

Topology — Half Bridge with Current Mode Control

Advantages of Half Bridge:

1. Voltage rating of switching devices is one-half that required by Flyback or Forward converter.
2. Output filter inductor helps capacitor (compared to flyback)
3. More efficient use of transformer core and copper.
4. Leakage inductance energy is returned to the input capacitor instead of being dissipated in resistive snubbers.

Advantages of Current Mode:

1. Removes one pole of half bridge's 2 poles.
   a. Easier to compensate.
   b. Better large signal performance from error amplifier.
2. Gives input voltage feed forward. (Good output regulation for input line changes.)

The Stability Problem of the Half Bridge Topology Using Current Mode Control (Refer to Figure 3)

Assume that Q2 closes with a longer pulse width than Q1. Current mode control keeps the peak current equal, so the amount of charge transferred from C2 is more when Q2 is closed. As a result the voltage at node 2 will decrease. The next time Q2 closes the voltage across the primary will be less so the current ramp will have a slower slope. The peak current will be kept the same, so the pulse width will be wider. This means that the node 2 voltage decreases even further, and eventually reaches zero. It is this stability problem that has prevented the widespread use of the half-bridge topology with current mode control. Fortunately there is a simple solution to this problem, using an auxiliary transformer winding made of small diameter wire with the same number of turns as the primary winding, and two small high voltage diodes. The credit belongs to an unknown engineer who attended one of our seminars in 1984.

Operation of the Correction Circuit

Assume that node 2 is low by 1 volt, at 49.5V. When Q1 closes, the primary voltage is V_{CC} – V node 2 = 100V – 49.5V = 50.5V. The auxiliary winding also has 50.5V across it, by transformer action, with the polarity as shown. Diode D1 will hold node 3 at approx. 0 volts. The other end of the aux. winding, node 2, will try to go to +50 volts. However, as node 2 voltage approaches 50 volts (from its original value of 49V) the voltage across the primary will also approach 50 volts.

If Q2 closes when node 2 is low, no corrective action takes place. Corrective action takes place when the other half of the cycle occurs, ie, when Q1 closes again. If node 2 is high, corrective action occurs when Q2 is closed.

PWM Controller

The PWM controller used is the UC3825, a high speed 1MHz chip with voltage or current mode capability, dual high current 1.5A totem pole outputs, 50ns propagation for shutdown during fault conditions, and other desirable features. It is somewhat similar to the UC3525A and UC3526A, with the addition of much faster speed and current mode capability.

Control and Gate Drive Circuits (See Figure 2)

The MOSFET gate drive circuit consists of the dual totem pole outputs of the UC3825 driving a small toroidal transformer with two secondaries having opposite polarity outputs. There are several advantages to this type of drive; first, no coupling capacitors are needed because of the balanced drive, and second, during off time both ends of the primary are grounded, preventing transients from turning on the MOSFETs.

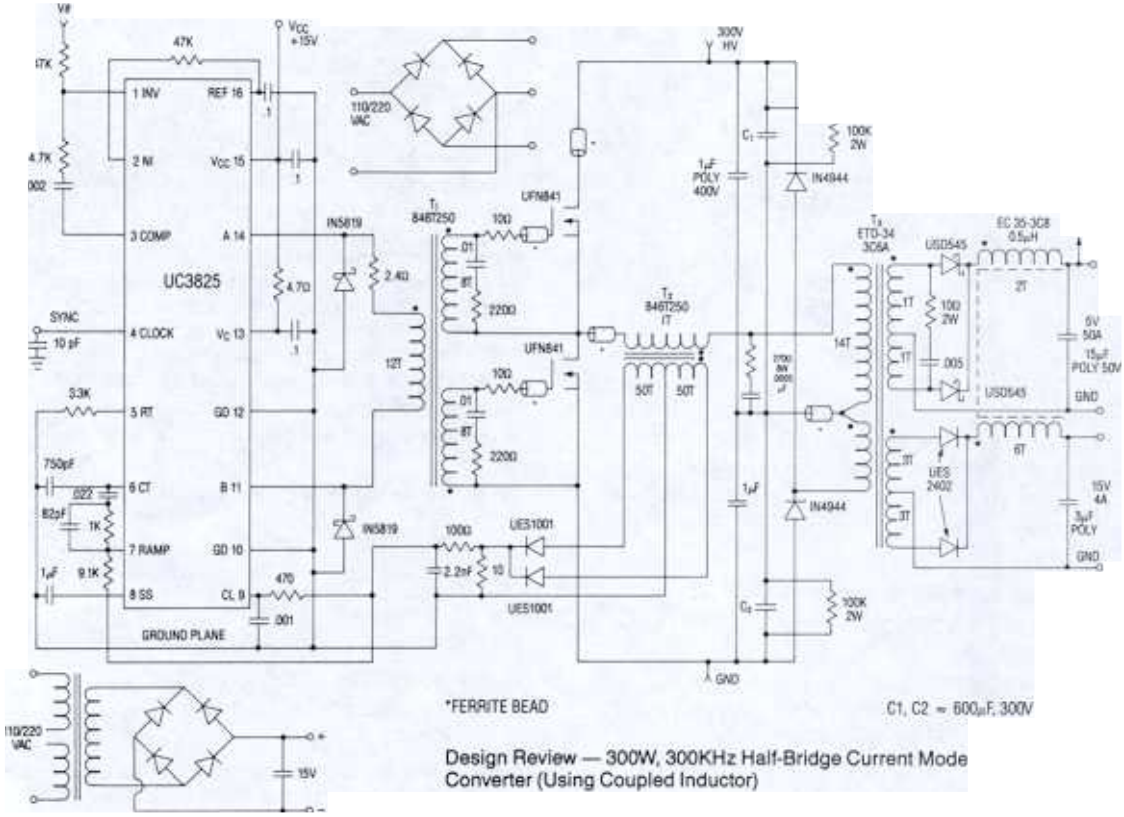

Figure 2.

T1 uses a Ferroxcube toroid, the 846T250-3C8, which has an A_L = 1650 mH/1000T. For 12 turns, $L_P = A_L \times N^2$ = (12/1000)² × 1650 mh = 230μH. Magnetizing current = i_M = di = edt/L = 15V × 1.5μs/230μH = 100 ma. This current passes through the A and B outputs of the UC3825, and creates power dissipation which needs to be minimized while keeping a low value of leakage inductance. The leakage inductance needs to be low in order to get fast risetimes and low delay time.

The ability of the core to handle the required energy without saturating is important. The circuit energy is

$1/2\ L_M I_M^2 = 1/2 \times 230\mu H\ (100ma)^2 = 1.2\mu J.$
The core can store

$$W = \frac{B^2 Ae\ le \times 10^{-6}}{2u_e} = \frac{2500^2 \times .259 \times 5.42 \times 10^{-6}}{2 \times 2700} = 16\mu J$$

(For explanation of magnetic terms refer to Section M in back of this manual). Mylar tape can be used to insulate between the primary and secondary windings.

The UC3825 outputs A and B see an inductive load, eg, the leakage inductance of the transformer. The energy stored in this inductance can drive the outputs negative during turn-off, which can impair the functioning of the chip. Schottky diodes from ground to each output will assure proper operation.

The inductance at the transformer secondaries in conjunction with the MOSFET gate capacitance will cause ringing at the gate, which could turn the MOSFET on during off-time. Resistive damping (with a small series dc blocking capacitor to reduce power dissipation) is used at each gate.

When discussing PWM controllers and gate drive circuits, especially at higher frequencies, remember that the design must start with a good ground plane, located as close to the PWM chip terminals as possible, and all components should have leads as short as possible. Supply voltages and reference voltages should be by-passed at the PWM chip terminals, and the single point ground concept should be used, especially for PWM chip signal ground, chip output ground and gate drive ground.

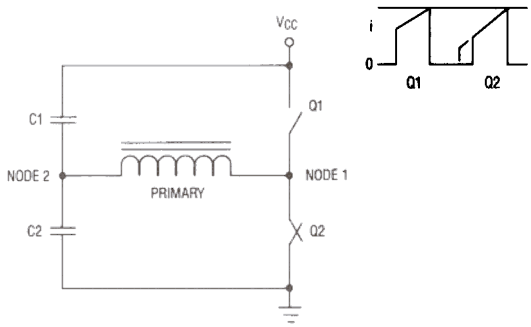

Figure 3.

Power Stage

This part of the design selects the power MOSFETs and calculates the amount of heat sinking needed.

$$I_{pri} = \frac{P_O}{V_{in} \times \text{Eff.} \times \text{D.F.}} = \frac{300W}{100V \times 0.75 \times 0.9} = 4.45A,$$

(where D.F. is the Duty Factor)

I_{pri} is time shared by the two MOSFETs

I_{pri} = 4.45A plus 10% safety margin = 4.9A

$V_{PRI\ (max)}$ = 385V

From the TO-220 MOSFET selection guide in the catalog, the UFN841 is rated at 450V, and 5.0A continuous at 100°C case. Since each of the MOSFETs will carry the 4.9A for less than half of a cycle, the current rating is OK.

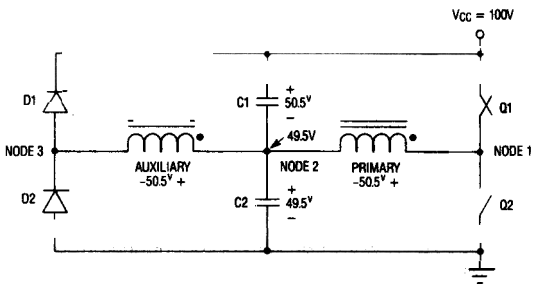

Figure 4.

The junction temperature rise due to dissipation in $R_{DS\ (ON)}$ during ON time should be decided (55°C) and the amount of heat sinking needed should be decided, 55°C. The fact that the $R_{DS\ (ON)}$ increases with temperature has to be factored into the calculations. From the data sheet curve that factor is 1.5 at 80°C.

$P_D = I^2 R_{DS\ (ON)} \times \text{D.F.} = 4.9^2 \times (0.80 \times 1.5) \times 0.45 =$ 12.9W average

where $R_{DS\ (ON)}$ is at T_j of 80°C (55°C rise)

$$R\Theta_{JA} = \frac{\Delta T_j}{P_D} = \frac{55°C}{12.9W} = 4.3°C/W$$

Two heatsinks 2" x 2.3" piggybacked will have a thermal resistance of 3°C/W. The TO-220 will add 1°C/W for a total of 4°C/W, just under the value required.

Power Transformer Design

First the approximate value of flux is determined. It is expected that at 300KHz it will be core loss limited. The allowable temperature rise of the transformer is decided, 40°C. The core and copper loss are made equal as a first approximation. It is planned to use the Ferroxcube ETD series of cores.

Temperature rise due to core loss = $\frac{40°C}{2} = 20°C$

$R\Theta$ of ETD-34 (smallest ETD) = 19°C/W

$$P = \frac{20°}{19°C/W} = 1.05W$$

$$\frac{P}{Vol} = \frac{1.05W}{7.64cm^2} = 140\ mw/cm^2$$

For 3C6A core loss curve at 140mw/cm²

B_{max} (at 300KHz) = 600GAUSS

$\Delta B = 2B_{max} = 2 \times 600G = 1200G$ pk to pk
= 0.12 Tesla

Now the core size can be selected, using the area product method. (Refer to Section M5 for a similar method.)

$$\text{Area product } AP = A_w A_e = \frac{11.1\ Pin\ 1.143}{K \Delta B\ F}\ cm^4$$

$$= \frac{11.1 \times 300W / 0.75^{1.143}}{(1 \times 0.3 \times 0.41) \times 0.12T \times 300KHz} = 1.03cm^4$$

For ETD-34, $AP = A_e A_W = 0.971cm^2 \times 1.22cm^2$
$= 1.18cm^4$

Minimum number of primary turns to support the primary voltage at the frequency selected.

$$N_{pri} = \frac{V_{pri\ (min)} \times 10^4}{2F \Delta B\ Ae} =$$

$$\frac{100V \times 10^4}{2 \times 300K \times 0.12T \times 0.971cm^2} = 14.2 \text{ turns minimum}$$

Turns ratio: Primary to 5 volt secondary

$$N = \frac{N_p}{N_s} = \frac{k\ [V_{in\ (min)} - V_{(on)}]\ D.F.}{V_O + V_F}$$

where k is allowance for inaccuracies, IR drops and delays.

$$= \frac{0.9\ (100-3.2)\ 0.9}{5 + 0.55} = 14.1$$

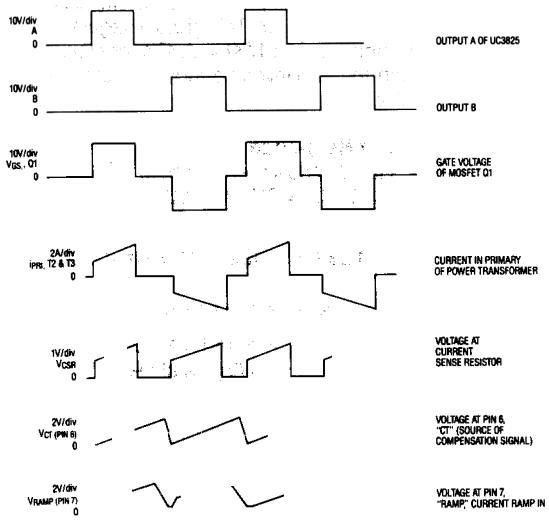

Figure 5.

Since 5V and 15V are required, the secondary turns ratio needed is approximately 3 to 1 (Approx. because of rectifier drops). The primary will have 14 turns, and the 5V secondary will have 1 turn (C.T.), in order to minimize copper volume and loss and window area needed. The 15V secondary will have 3 turns (C.T.) and an output of 15.5 volts.

Primary (See Sections M5 and M2)

$I_p\,(max) = I_{in}\,(max)/K_t = \dfrac{P_{in}\,(max)}{V_{in}\,(min) \times K_t} = \dfrac{300/.75}{100 \times 1} = 4.0A$

$J\,max = 450\,(AP)^{-0.125} = 450 \times 1.18^{-0.125}\,450 \times 0.98 = 440A/cm^2$

$A_{xp} = I_p(max) / J\,max = 4.0/440 = .009\,cm^2 = \#17AWG$

Depth of penetration at 300KHz = .013 cm, diameter of #17 is 0.115 cm

Use 20 × #32 in parallel. (Twisted.) See Section M2 for eddy current loss curves. Wind in two banks, one bank on each side of the secondary windings. This is termed interleaving. It reduces leakage inductance by a factor of 3.

5V Secondary

$I_S(max) = I_O(max) / 1.414 = 50A / 1.414 = 35A$

$Ax\,(sec) = I_S(max) / J\,max = 35 / 440 = 0.079cm^2$

Use copper strap 10 mils × 0.8″ = .008 sq in = $0.052cm^2$

Area OK since strap is better than wires.

Check eddy current loss factor; Dpen = 7.5/f (1/2) = 7.5 (300K) 1/2 = .013cm = 5 mils. Strap is 10 mils thick. Primary is interleaved around secondary so depth is 5 mils in from each side for a total of 10 mils.

15V Secondary

$I_S(max) = I_\Theta(max) / 1.414 = 4A / 1.414 = 2.82A$

$Ax = I_S(max) / J\,max = 2.82 / 440 = .0064cm^2$

Use copper foil 3 mils thick × 0.3 inches wide.

Losses and Temperature Rise of Transformer

$P_w = 2\,I_P^2 N_P l_t R = 2 \times 4^2 \times 14 \times 6.0 \times .00028 =$ 0.66 watts (pri & sec)

For 3C6A, loss = 1.05W

$Pt = Pw + 0.66 + 1.05 = 1.71W$

For ETD-34, $R\Theta = 19°C/W$

$\Delta T = P_T \times R\Theta = 1.71W \times 19°C/W = 32.5°C$ rise (less than 40°C is OK)

Current Sense and Slope Compensation

Known circuit values:

- Power transformer turns ratio = 14
- Current sense transformer turns ratio = 50
- Maximum primary current = 4.0A
- Voltage threshold at current limit pin of UC3825, 1.0V
- T_{ON} of UC3825 at 600KHz = 1/600K – 0.1μs deadtime = 1.57μs

For current sense circuit:

$I_{SEC} = \dfrac{I_{pri}}{N} = \dfrac{4.0A}{50} = 0.080A$

Using margin of 20%

$R_{CSR} = \dfrac{V_{th}}{1.2\,I_{sec}} = \dfrac{1.0V}{0.08 \times 1.2} = 10\ ohms$

Slope compensation, from current slope of 5V output inductor, to ramp input (Pin 7) of UC3825, and from C_T (Pin 6)

$di/dt\,(sec) = V_{sec}/L = 5.7V/0.5\mu H = 11.4A/\mu s$

$di/dt\,(pri) = \dfrac{11.4A/\mu s}{14} = 0.81A/\mu s$

V_{slope} at $CSR = \dfrac{di/dt\,(pri)}{50} \times R_{CRS} \dfrac{0.81 \times 10}{50} = 0.16V/\mu s$

V_{osc} slope at pin 6 = $1.8V/1.57\mu s = 1.15V/\mu s$

$R_{comp} = \dfrac{R_{in} \times V_{osc.\,slope}}{V_{slope} \times k} = \dfrac{R_{in} \times 1.15}{0.16 \times .75} = R_{in} \times 9.6$

where k = ratio of slope compensation introduced, to inductor slope, value usually between 0.5 and 1.0.

Current Sense Transformer

The transformer should not saturate. Circuit energy is 1/2 Li²

For the 846T250 core, primary inductance of 1 turn, L_{pri} = $A_L\,N_P{}^2/N^2 = 1650mh \times 1^2/1000^2 = 1.65\mu H$,
$W = 1/2\,L\,i^2 = 1/2 \times 1.65\mu H \times 13.2\mu J$

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Maximum core energy storage:

$$W = \frac{B^2 A_e l_e \times 10^{-8}(cm)}{2u_e} = \frac{2500^2 \times .259 \times 5.42 \times 10^{-8}}{2 \times 2700} = 16\mu J$$

Coupled Filter Inductor Design

If both inductor coils are wound on a common core, then several benefits are obtained, eg, good dynamic cross-regulation, current limiting to prevent core saturation, and low cost and smaller size. Two design constraints need to be observed. First, use the same turns ratio for the inductor windings as the secondary windings of the transformer. Second, use a winding arrangement that gives approximately 2% or more leakage inductance. (These two points will minimize circulating ripple currents and make matching rectifier V_f's unnecessary.

Coupled inductors are especially useful when current mode control is being used. Separate inductor-capacitor filters for each output each have a tendency to series resonate at their own frequencies, since current mode makes the output look like a high impedance. This adds large gain and phase shifts at these different frequencies, all usually within the loop closing frequency, and thus causing unaccustomed problems. Coupled inductors minimize this effect.

Other factors should be considered when using coupled inductors, such as ripple current, leakage inductance and wiring inductance. Refer to Section M7 for a more complete discussion.

Closing the Loop

The oscillator frequency is 600KHz. Theory suggest that we close the loop at 0db at a frequency no higher than f_{odb} = $fsw/2\pi D$ = 600KHz/2π0.9 = 106KHz, where D = maximum duty factor.

For current mode operation of a buck type converter the inductor does not appear in the forward signal path. Instead there is a pole consisting of the output filter capacitor and the effective output load resistance. This resistance changes as the load current changes: $R_O = V_O / I_O$.

The output filter capacitor and its ESR constitute a zero in the forward path. For electrolytic capacitors, whose capacitance is usually much larger than necessary in order to get a low enough ESR to meet the ripple voltage spec, the frequency of this zero is fairly low, and in many cases, it is used to get enough phase margin to close the loop. In the design discussed here, polypropylene film capacitors are used; their zero is above a megahertz and thus does not enter into loop closure.

The approach taken here is to reduce the gain of the error amplifier with a slope of −20db/decade through 0db to a negative gain equal to the (positive) gain of the control to output response at 106KHz. The error amplifier is then flattened out at the lowest output pole frequency by adding a zero in the EA compensation network. Refer to Figure 6.

In designing the network around the error amplifier, we wish to use low values of resistance for low noise pickup, but not so low as to load down the output of the EA. For this case 4.7K is used in the feedback path, in series with 0.002uf, and 47K in series with the input. This gives a negative gain of 10x = −20db, and a zero at 17KHz. A 47K resistor is also put in series with the non-inverting input to help negate input current offset.

Control to Output Response

The main output is 5V at 50A max., 5A min.
R_O = 5V/50A = 0.1Ω, R_O = 5V/5A = 1Ω

The output filter capacitor is 15μF.

$R_p = 1/2\pi R_O C = 1/2\pi\, 0.1 \times 15\mu$ = 110KHz at 50A, 11KHz at 5A

k = Max I_L/max V_C = 50A/1.0V = 50A/V

$V_O / V_C = KR_O = 50 \times 0.1 = 5$ (14db) at 50A
$= 50 \times 1 = 50$ (34db) at 5A

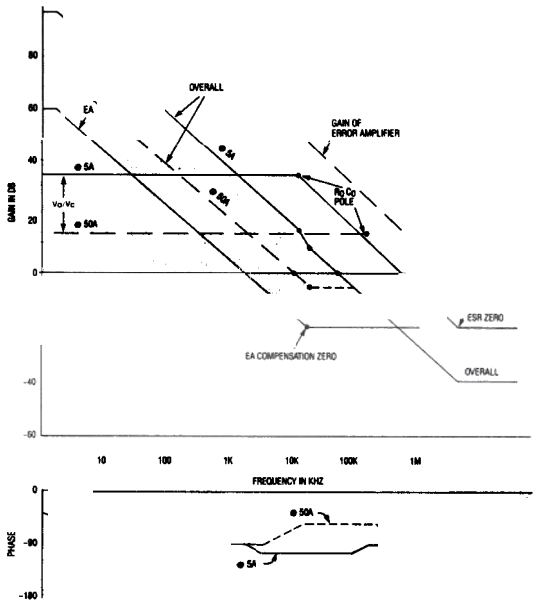

Figure 6.

Bibliography

Current mode control, SEM 400 Topic 1, and Application Note U-97

MOSFET Gate Drive, Addenda, Section D2 or Application Note U-98

Transformers, Addenda, Section M5

Inductors, Addenda, Section M6

Coupled Inductors, Addenda, Section M7

Feedback Loop, Addenda, Section C1

Snubbing, Application Note U-85

Eddy Current Losses, Addenda, Section M-2

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