Phase Management Raises Interleaved PFC Efficiency

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Whether implemented with discrete components or integrated within the PFC controller, phase management can improve light-load efficiency of power supplies to meet 80 PLUS efficiency requirements.

As the demand for higher power densities and more efficient power supplies increases, so does the popularity of interleaving power converters. It has been proven that interleaving power factor corrected preregulators can reduce the overall magnetic and electro-magnetic interference (EMI) filter volume, as well as reduce overall system conduction losses. For this reason, it has become a more popular topology for offline power converters requiring power factor correction (PFC).

However, interleaving does not come free. It increases the complexity of the design, as well as a number of diodes and FETs required. These added semiconductor devices increase switching losses, decreasing the converter's light-load efficiency and making it harder for the design to pass 80 PLUS requirements at light loads (For more on 80 PLUS initiatives,

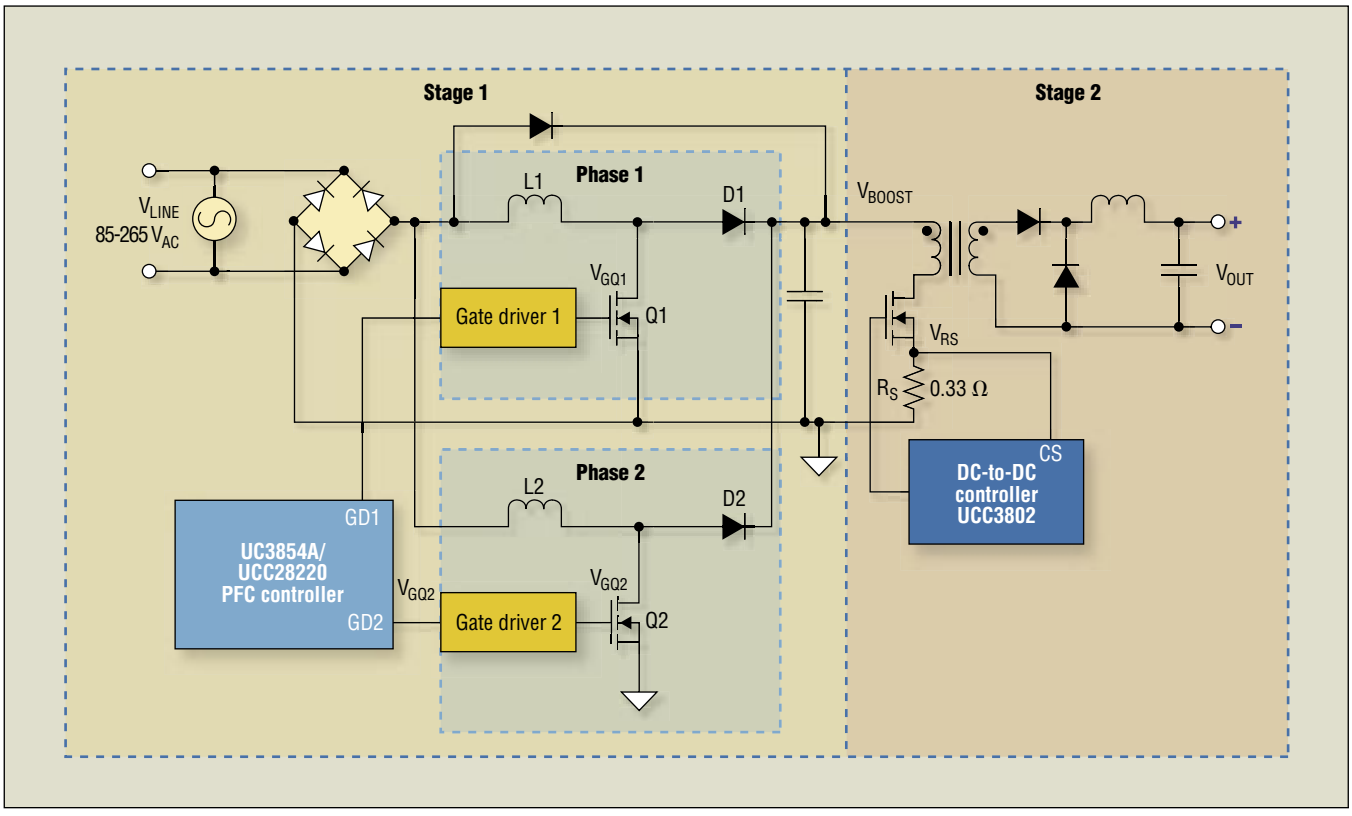

Fig. 1. *An ATX power supply with a two-phase, interleaved PFC pre-regulator exhibits lower conduction losses than a similar supply with single-phase PFC.*

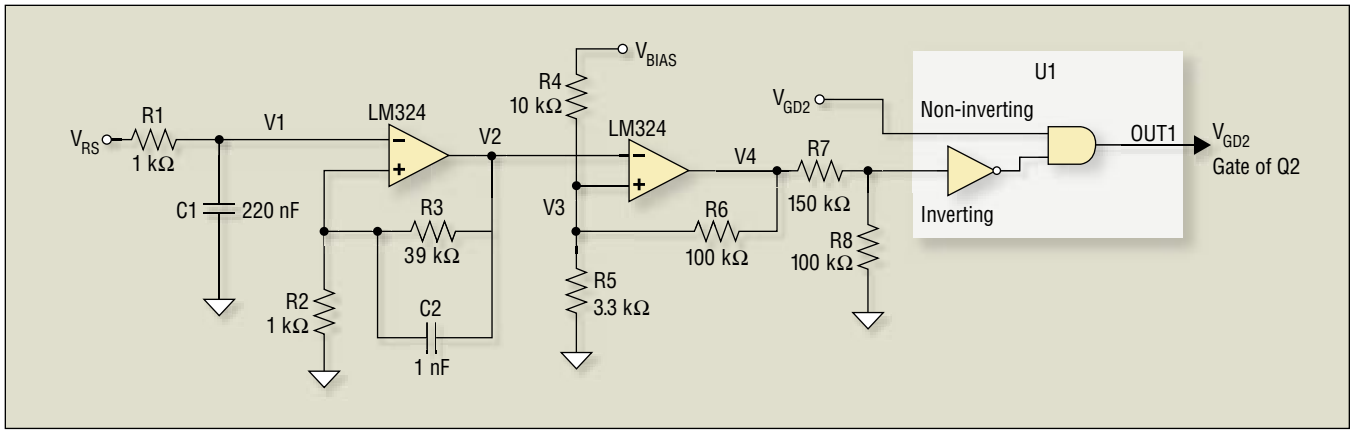

Fig. 2. *This circuit, which replaces the gate driver 2 block in Fig. 1, uses the current-sense signal developed across the forward converter's current-sense resistor (V_{RS}) to activate and deactivate phase two of the interleaved PFC pre-regulator.*

see www.80plus.org/). In these designs, it is advantageous to let just one of the phases run at light load to regulate the power and to turnoff any additional phases. With this approach, 80 PLUS requirements can be met easily. Phase-management circuitry can be implemented with discrete circuitry or integrated within a PFC controller to turn on and off phases based on overall system loading.

80 PLUS Specifications

In 2008, 80 PLUS specifications will require offline power-converter designs to have a power factor of greater than 0.9. These power systems will require PFC. Generally, an offline power converter with PFC is a two-stage system. Typically, stage one is a PFC boost pre-regulator and stage two is some type of stepdown converter. Adding the PFC pre-regulator to the system introduces additional losses, making it more difficult for the design to meet the 80 PLUS efficiency requirements from 20% to 100% load.

To help improve system efficiency, the single-stage PFC boost pre-regulator stage can be replaced with an interleaved PFC boost pre-regulator stage (**Fig. 1**). Interleaving increases system efficiency by reducing conduction losses. This is made visible by evaluating the simplified conduction loss equations for the single-phase PFC (P_{SINGLE}), and the conduction losses for an interleave PFC pre-regulator ($P_{INTERLEAVED}$). From these equations, you can see that the conduction losses of the interleaved pre-regulator could be as low as one-half that of a single-phase pre-regulator. In these equations for conduction losses, R represents the effective wiring and switch impedance of the power converter.

$$P_{SINGLE} = I^2R \qquad \text{Eq. 1}$$

$$P_{INTERLEAVED} = \left(\frac{I}{2}\right)^2 R + \left(\frac{I}{2}\right)^2 R = \frac{I^2}{2}R \qquad \text{Eq. 2}$$

Even though interleaving PFC pre-regulators can improve efficiency where conduction losses dominate over switching losses, interleaving pre-regulators can decrease light-load system efficiency. When the converter is operating at lighter loads where switching losses ($P_{SWITCHING}$) dominate, one of these converters should be shut down to improve light-load efficiency.

Eq. 3 describes the two-phase interleaved boost diodes and boost FETs switching losses, where V_{DS} and I_{DS} are the FET drain-to-source switching voltage and FET drain current, respectively. Variables t_R and t_F are the FET's drain-to-source rise and fall times. C_{OSS} is the FET's parasitic drain-to-source capacitance, Q_G is the FET's gate charge, and V_G is the gate-drive voltage applied to the FET's gate drive to activate it. Variable f_S represents the converter's switching frequency. Variable I_{RR} represents the boost diodes reverse-recovery current.

$$P_{SWITCHING} = 2\left(I_{DS}V_{DS}(t_R + t_F)f_S + \frac{C_{OSS} \times (V_{DS})^2 f_S}{2} + \frac{V_G}{2}Q_G f_S + I_{RR}V_{BOOST}f_S \right). \qquad \text{Eq. 3}$$

In these two-stage, off-line power converters, the front end (stage one) provides PFC. Generally, stage two is a forward converter that steps down the PFC boost voltage to a lower, more usable voltage. Since the PFC front end regulates the input of the forward converter, the average current-sense signal developed across the stepdown converter's current sense signal (R_S) can be used to monitor the average input power of the forward converter. This average current-sense signal can be then used to trigger phase-management circuitry.

The circuitry presented in **Fig. 2** can be added to the system presented in **Fig. 1**, providing phase management to activate and deactivate PFC boost phases based on system loading. This circuitry replaces gate driver 2 block in **Fig. 1**. This circuitry works by using the current-sense signal developed across the forward converter's current-sense resistor (V_{RS}) to activate and deactivate phase two of the interleaved PFC pre-regulator (stage one).

In **Fig. 2**, resistor R1 and C1 form a low-pass filter with a low-frequency pole at 723 Hz. This filter is used to develop a dc voltage (V1) that represents the average voltage across the stepdown converter's current-sense resistor. Generally, since

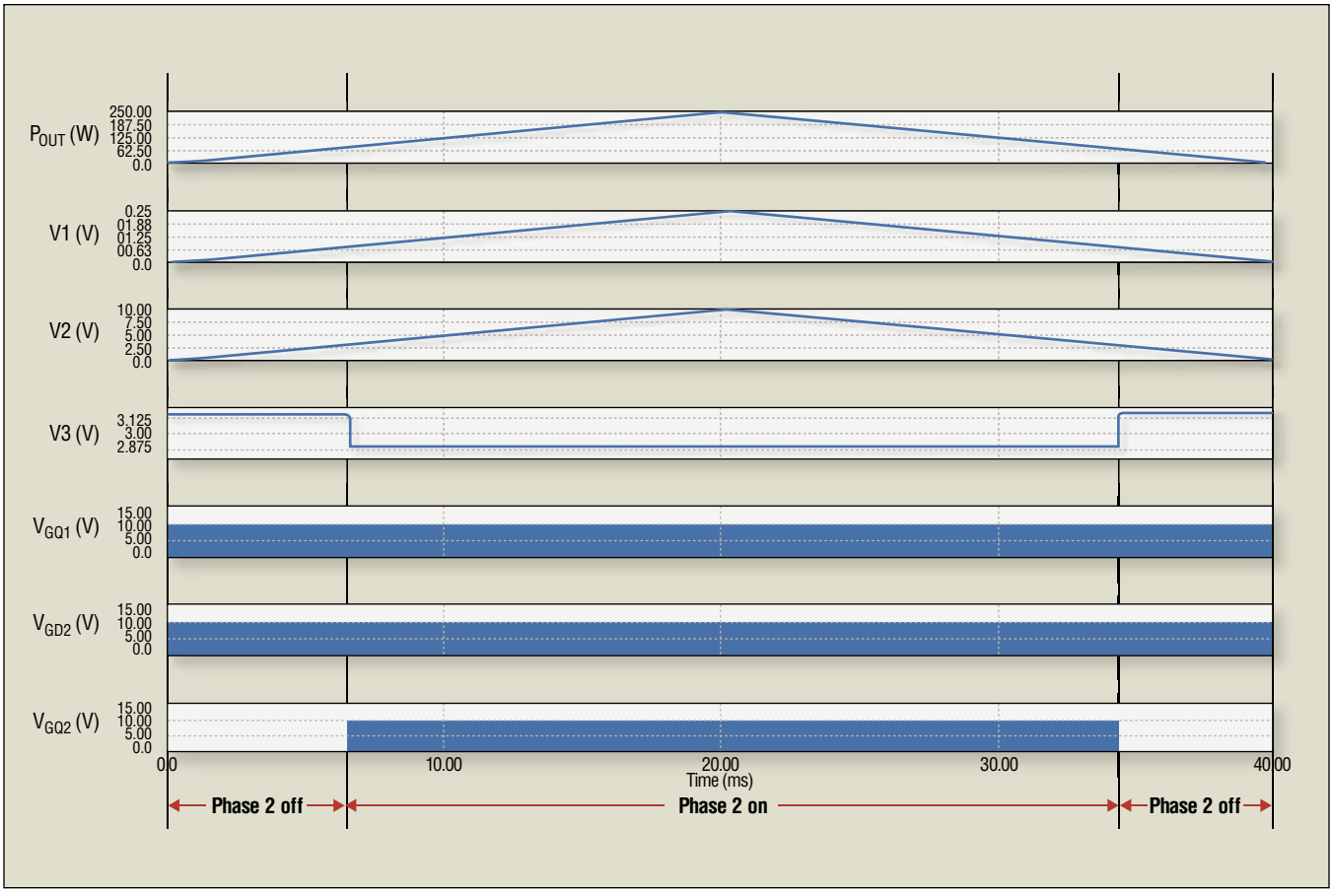

Fig. 3. *Spice simulation of the phase-management circuitry in Fig. 2 confirms that comparator A2 triggers at the desired output-power levels (32% and 29% of rated power), but because of delays introduced by the low-pass filter R1-C1, phase two in Fig. 2 turns on and off at slightly different power levels (33% and 28% of rated power).*

the average current-sense signal is less than 0.25 V, the noninverting amplifier configuration of electrical components A1, R3 and R2 is used to amplify the average current-sense signal (V1) to a more manageable voltage (V2) that can be easily monitored.

Amplifier A2 and electrical components R4, R5 and R6 form a hysteretic comparator that enables and disables phase two, based on the amplified average current-sense signal. Resistor R7 and R8 form a voltage divider to attenuate the output of amplifier A2. This helps to protect the gate driver IC U1. Gate driver U1 is a FET gate driver with an inverting and noninverting input that drives FET Q2. It can be activated and deactivated based on the output of the hysteretic comparator (V4).

When the hysteretic comparator's output is high, the boost PFC pre-regulator runs in single-phase operation, and FET Q2 is always off. When the hysteretic comparator output (V4) is low, the gate-drive control signal from the PFC control (GD2) is passed through to the FETs gate drive. The interleaved PFC pre-regulator runs both phases.

Phase-management circuitry in **Fig. 2** works in applications similar to the power converter in **Fig. 1** by properly selecting resistor R3 and R5, based on the appropriate power levels. This is done by disconnecting the GD2 trace from the PFC controller to the gate driver 2 of **Fig. 1**. The circuit of **Fig. 2** would be put in with the V_{RS} trace connected to the V_{RS} signal at R_S, and the GD2 output at the PFC connected to GD2 input of **Fig. 2** and the Out1 signal of **Fig. 2** connected to the input of the gate driver 2 of **Fig. 1**. The following example shows how to select these two resistors based on a 250-W power supply that has a regulated PFC boost voltage (V_{BOOST}) of 390 V. The current-sense resistor of the forward converter (R_S) in this example is 0.33 Ω. The circuit turns the second boost phase off when the supply is operating at less than 29% of the converters rated output power. The second boost phase turns on when the converter is operating at greater than 32% of the supply's rated output power. The bias voltage (V_{BIAS}) was set to 12 V.

Resistor R3 determines the current-sense amplifier gain and is selected so that V2 will operate from a 0-V to 10-V range. For the circuitry to turn phase two on and off, the efficiency (η) of the second power stage needs to be considered. In this example, the efficiency of the second stage was 86%, and R3 needs to be 39 kΩ, based on load and the forward converter's efficiency.

$$V1 = \frac{P_{OUT} R_S}{V_{BOOST} \times \eta} = \frac{250\ W \times 0.33\Omega}{390\ V \times 0.86} \approx 0.25\ V \qquad \text{Eq. 4}$$

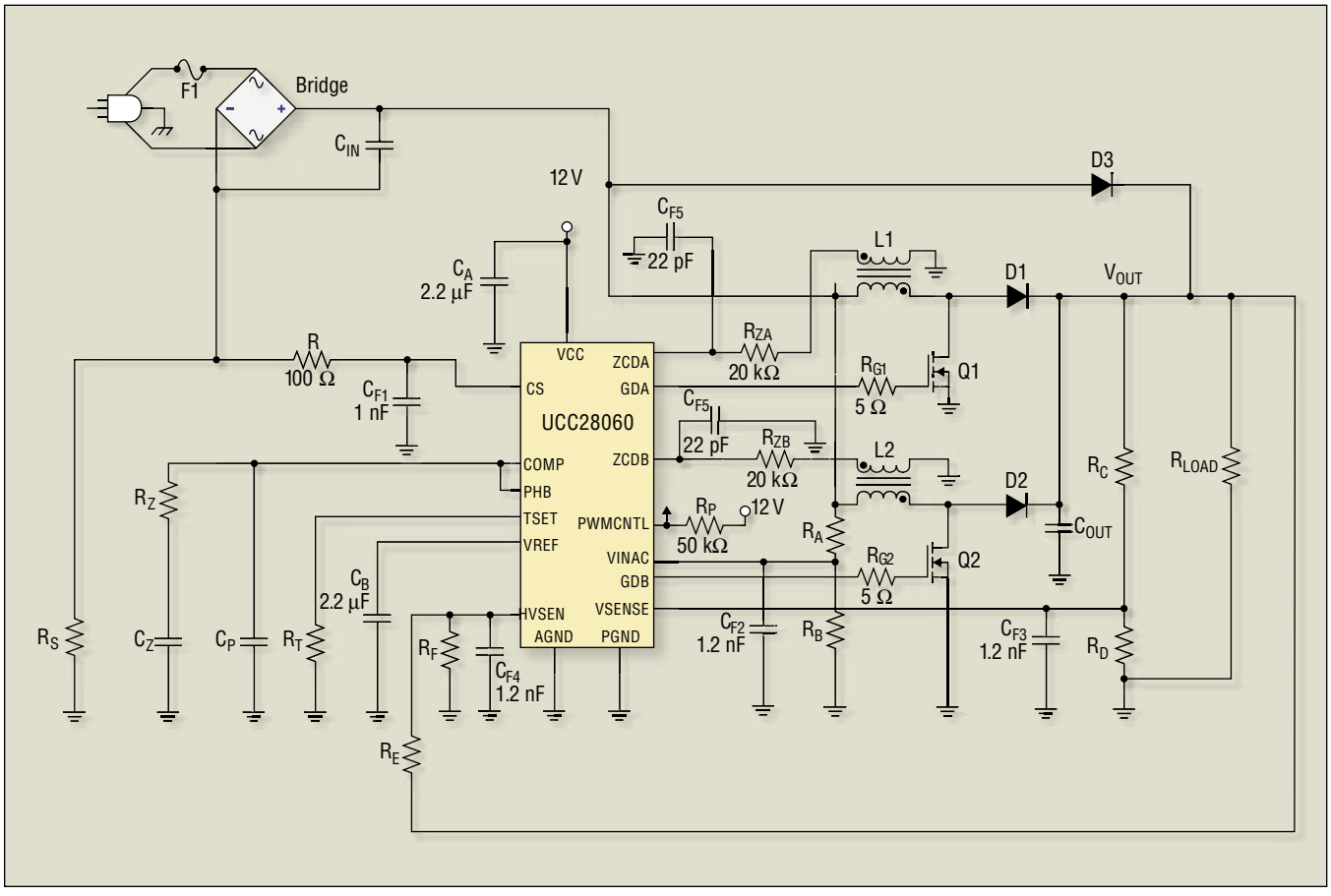

Fig. 4. *TI's UCC28060 interleaved transition-mode controller, which integrates the phase-management circuitry, is used to implement a 300-W interleaved PFC pre-regulator prototype.*

$$R2\left(\frac{V2}{V1}-1\right)=R3=1\ k\Omega\left(\frac{10\ V}{25\ V}-1\right)=39\ k\Omega \qquad \text{Eq. 5}$$

Resistor R5 sets the approximate power level where phase two is disabled. In this example, resistor R5 was selected to turn the phase off at a power level of approximately 30% of the full load power (%Load).

$$V3=\frac{P_{OUT}R_S}{V_{BOOST}}\frac{R3}{R1}\frac{\%Load}{100}=$$

$$\frac{250\ W\times 0.39\ \Omega}{390\ V}\times\frac{39\ k\Omega}{1\ k\Omega}\times\frac{30}{100}=2.925\ V \qquad \text{Eq. 6}$$

$$R5=\frac{R4\times V2}{(V_{BIAS}-V3)}=\frac{10\ k\Omega\times 2.925\ V}{12\ V-2.925\ V}=3.2\ k\Omega \qquad \text{Eq. 7}$$

A standard value resistor of 3.3 k Ω was chosen for R5.

$$R5=3.3\ k\Omega \qquad \text{Eq. 8}$$

Resistor R6 sets up the converter's hysteresis and may need to be adjusted for the individual application. In this example, the converter had roughly 288 mV of hysteresis. The second boost phase (phase two) turns on when the converter is operating at 32% of its rated output power. Phase two turns off when the converter is operating below 29% of the supply's rated output power.

$$Hyst=V_{BIAS}\left(\frac{\frac{R5\times R6}{R5+R6}}{R4+\frac{R5\times R6}{R5+R6}}-\frac{R5}{R5+\frac{R4\times R6}{R4+R6}}\right)=$$

$$12\ V(0.242-0.266)=-28\ mV \qquad \text{Eq. 9}$$

To evaluate how well the circuitry worked, a simplified SPICE model was constructed and evaluated. The output power (P_{OUT}) was varied from 0 W to 250W and back down to 0 W over a 40-ms period. The output power (P_{OUT}) and the voltages at node V2, V3 and the gate of FETs Q1 (V_{GQ1}) and Q2 (V_{GQ2}) were monitored. Refer to **Fig. 3** for waveforms.

This evaluation confirms that phase two turns on when the converter is loaded with greater than 32% of its maximum output power, and two turns off when the converter is loaded with less than 29% of the system's maximum output power. However, due to the delays caused by the low-pass filter of R1 and C1, phase two turns on at 82 W and turns off at 70 W. These values correspond to roughly 33% and 28% of the supply's rated output power. The delay is apparent in the offset of the peak of the P_{OUT} and V2 waveforms. The maximum time delay caused by the filter is less than 1.1 ms and has a minor effect on the simulated system.

An Integrated Approach

An alternative to implementing phase-management

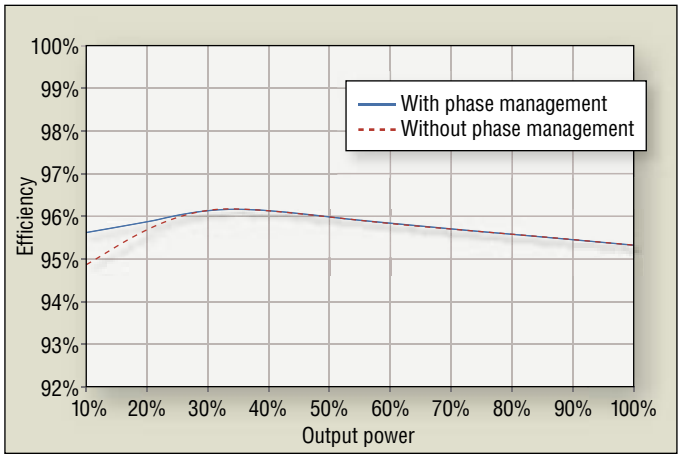

Fig. 5. *At 115-V RMS input, switching to single-phase operation at light loads improves the efficiency of the PFC pre-regulator by nearly 1%.*

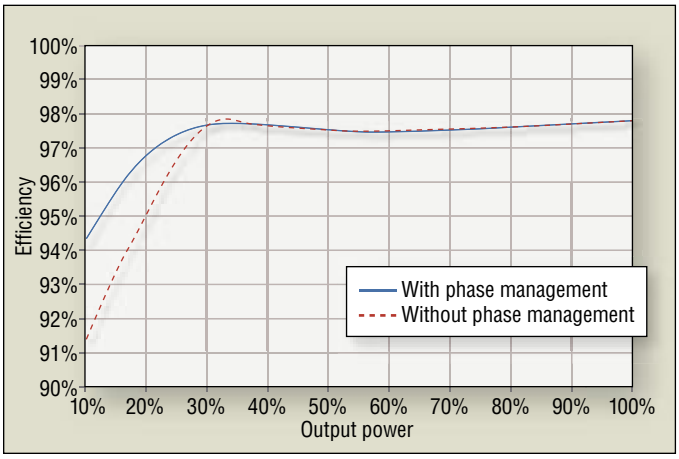

Fig. 6. *At an input of 230-V RMS, switching to single-phase operation increases light-load efficiency of the PFC pre-regulator by about 3%.*

circuitry with discrete components is to integrate this functionality within the PFC controller. To illustrate this approach, a 300-W interleaved transition-mode PFC pre-regulator prototype was constructed (**Fig. 4**) using TI's UCC28060, an interleaved transition-mode controller with built-in phase-management circuitry.

In this design, both interleaved converter phases operate when the converter is loaded with more than 30% of the power converter's maximum output power.

Figs. 5 and **6** show the PFC pre-regulator prototype's efficiency with and without phase management at input voltages of 115 Vac and 230 Vac, respectively. These graphs show that phase management improved the light-load efficiency of the prototype by 1% to 3% based on line and loading. This efficiency improvement at light loads by phase management could be the difference between passing and failing the 80 PLUS light-load efficiency specification. **PETech**