Boost back during End of Charge

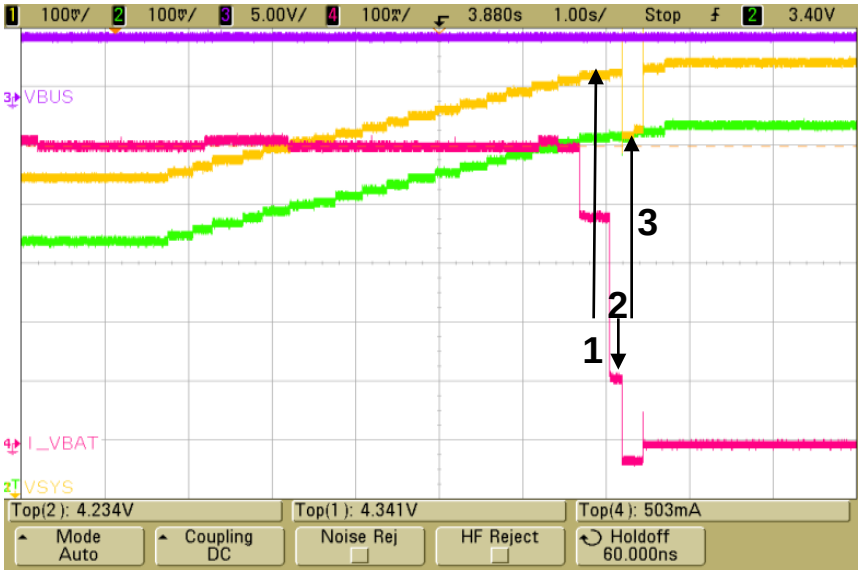
TWL6032

IPG - MIC Applications

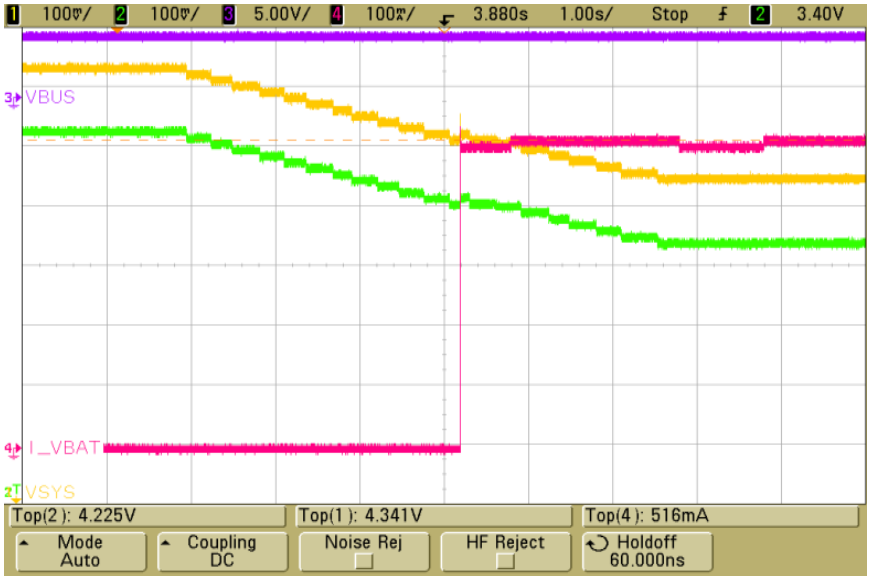
May 31, 2013

Background regarding end of charge detection

1. When approaching end of charge, VSYS is in tracking mode VSYS=VBAT+DLIN
2. At VBAT=VOREG (CV loop is active) and charge current is below ITERM the end of charge is detected. After this detection, it is needed to check if the end of charge happened with a battery connected or due to a battery unplug.
3. Around 1mA is sinked from the battery for 256ms, if VBAT collapses below 2V then it's a battery removal case otherwise it's a battery connected case.



VBAT=4.0V / VBUS=5V
VBAT increased over 4.2V to enter in CV loop

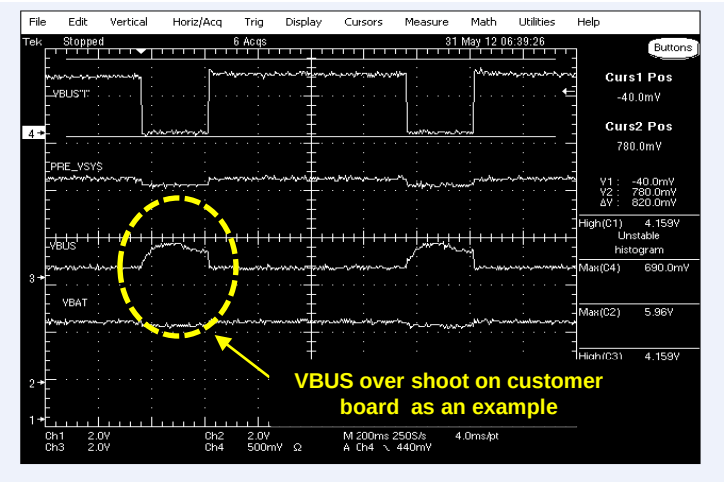


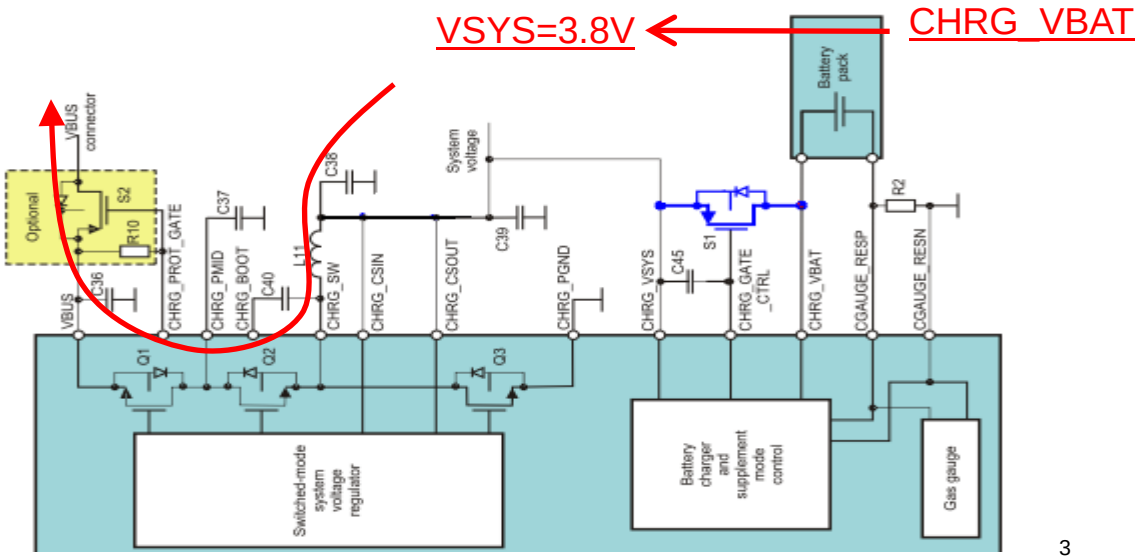
VBAT=4.2V / VBUS=5V
VBAT decreased to restart the charge and re-enter in CC loop

I_VBAT / VSYS / VBAT / VBUS

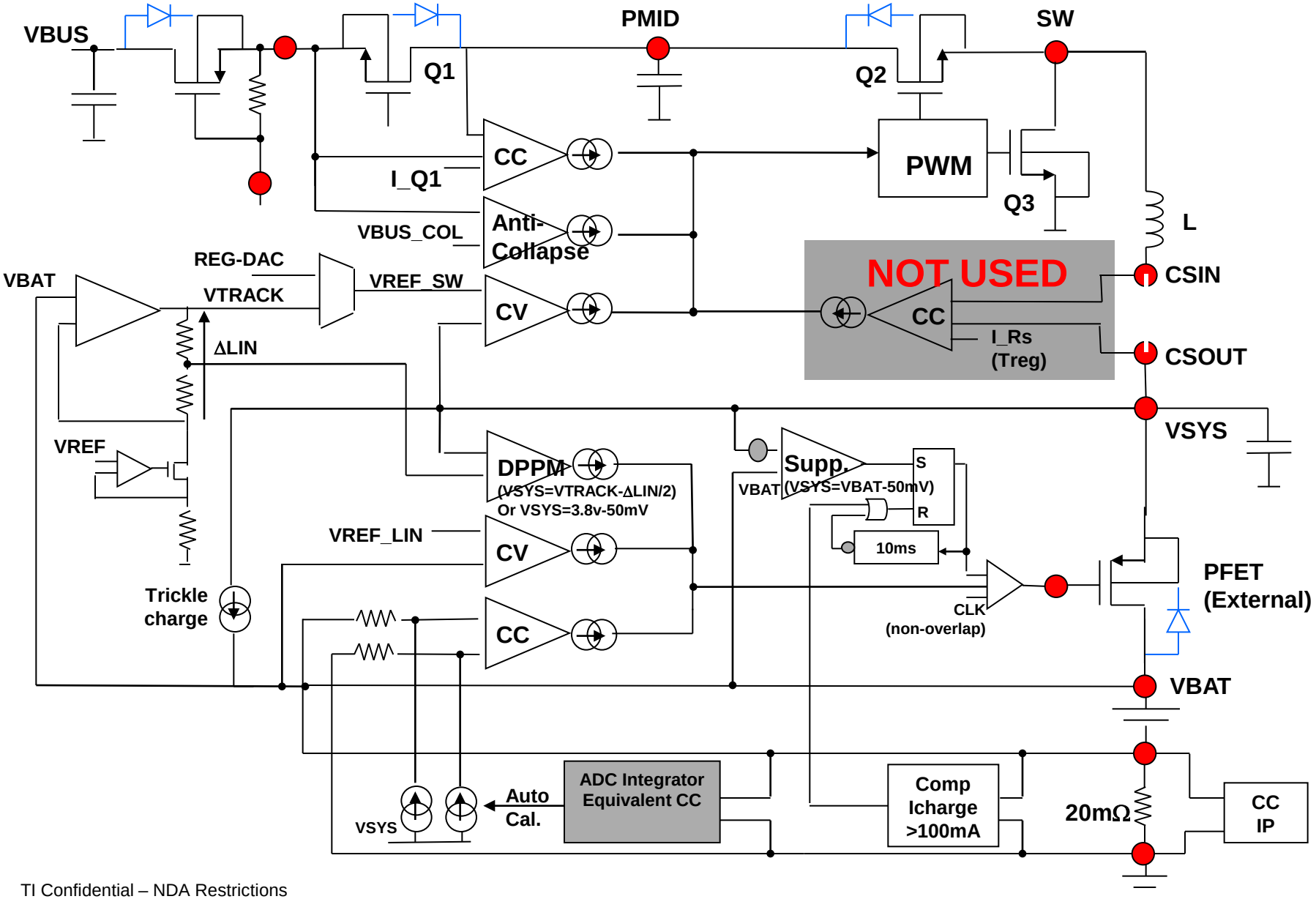
Negative current at end of charge detection

- During the battery detection mechanism (256ms), VSYS target is to 3.8V while VBAT is at VOREG so actually VSYS is over 3.8V, consequently the error amp is at minimum. PWM is always low & high side FET is always off so the boot is never recharged.
- The Low side FET needs to be turn on periodically to maintain the boot-cap voltage. In this the charger is acting as a boost any LS pulse is injecting current from battery to SW and then to VBUS through the parasitic diode of the HS FET.
- In summary in this mode there is negative current because VBAT is over VSYS target which makes the charger acting as a boost injecting current to VBUS.
- If the adaptor can not accept any negative current then it can lead to VBUS Over shoot.





Battery Charging with Power Path



How to avoid negative current?

- During CV mode software should monitor EOC interrupt continuously.
- At EOC, force VSYS > VOREG + DLIN and disable the tracking bit by writing CHARGERUSB_VSYSREG register.
- After 1 second enable the tracking again by writing CHARGERUSB_VSYSREG[7].

Why forcing VSYSREG without tracking fix the issue?

- If VSYSREG is forced without tracking at a value over VOREG + DLIN then at end of charge during the 256ms 1mA sink detection, VSYS is not forced at 3.8V.
- There is no negative current to VBUS.
- Load on VSYS is supplied from VBUS and not from the Battery.