Objective: To use LM5045 as a class-D amplifier to drive a full-bridge load as part of a transmitter for sonar applications. In this case, a sinusoidal signal is directly input to pin COMP to be PWM modulated. No external feedback is employed in this stage.

Problem: It seems that the ramp generation is heavily affected when pin SLOPE feeds into pin RAMP. This problem has been verified both in simulation and experimental bench.

Action: contact TI engineering for technical support ASAP.

i) Simulation Results:

The model used for simulation was obtained from www.ti.com. The application example shown in Figure 1 has been taken as basis for the simulation bench, which is depicted in Figure 2. As pin COMP requires a current-mode input, a V/I-converter was used to convert the sinusoidal signal, as highlighted in red. The supply voltage was altered for 70V-DC value.
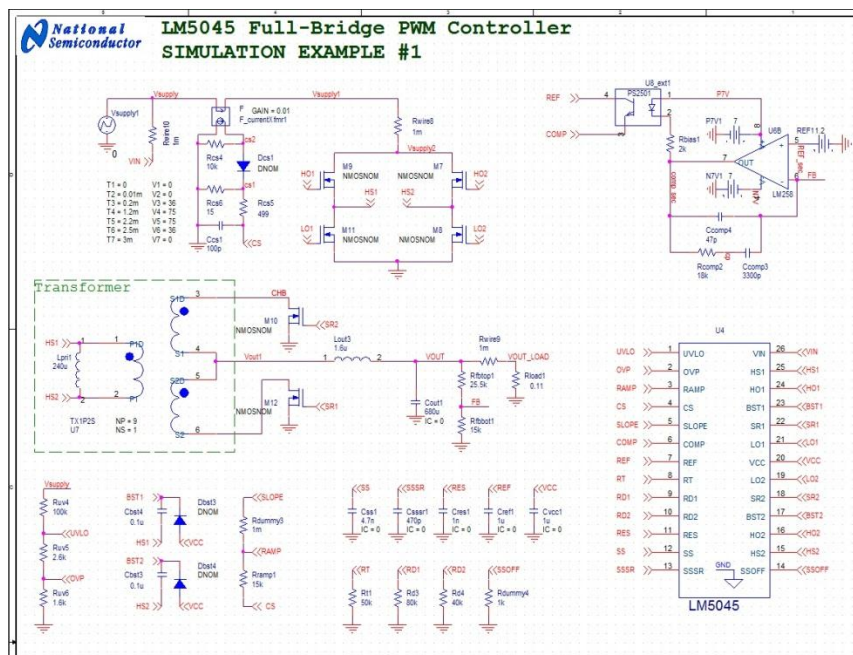
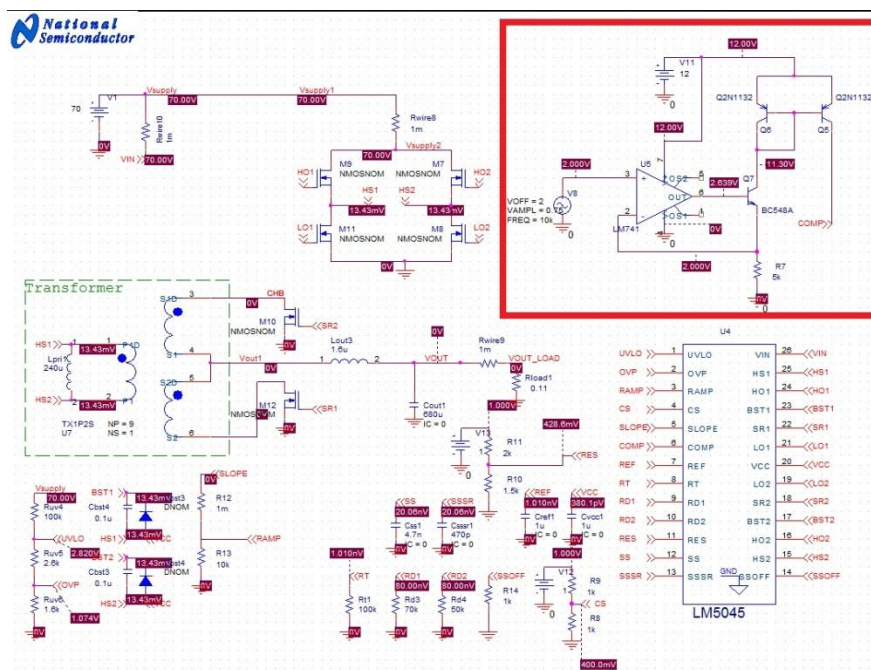

Figure 1. Original simulation bench

Figure 2. Modified simulation bench

We then expected to obtain a ramp and sinusoidal waveforms at the PWM-comparator input, according to the diagram in Figure 3 and marked in red. However, simulation data show that the ramp is deformed by the sinusoidal signal, as indicated in Figure 4.
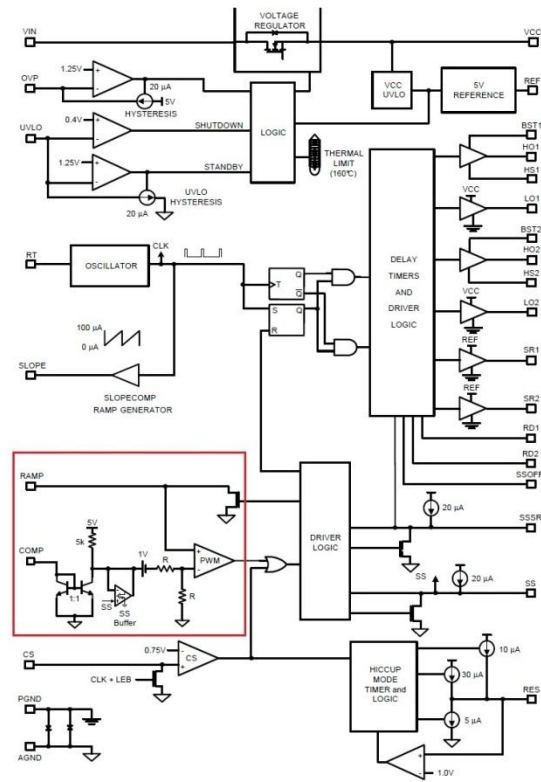

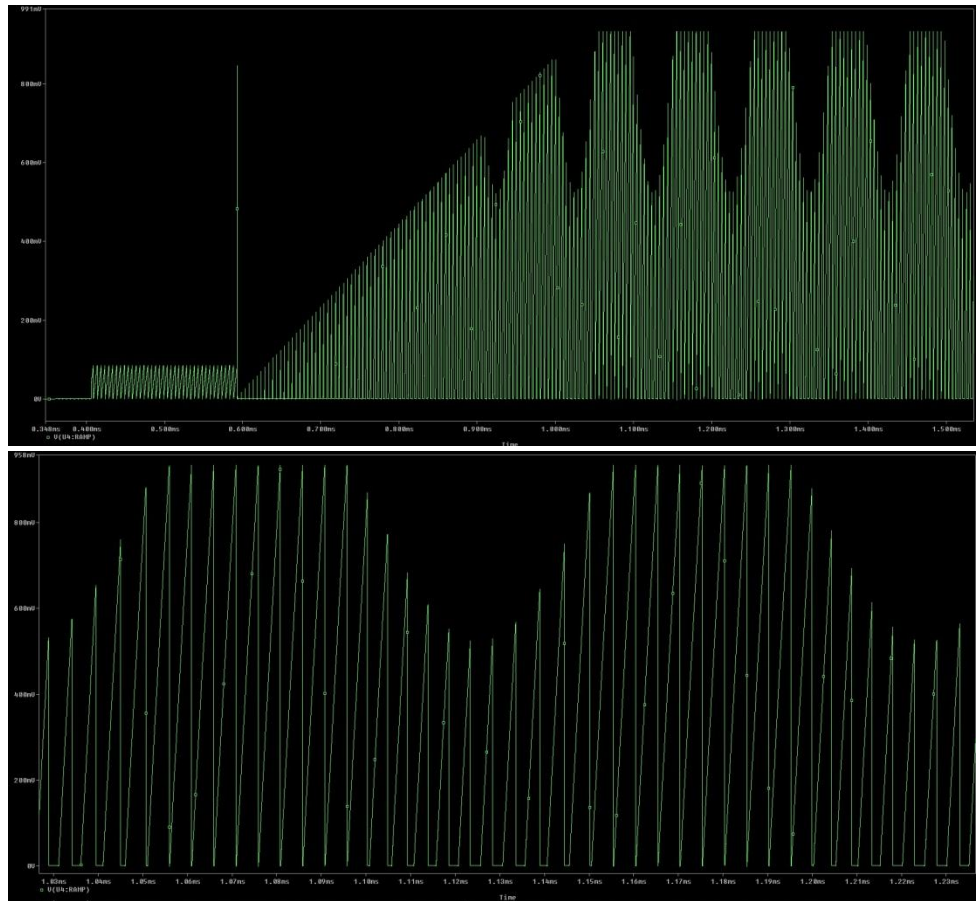Figure 3. LM5045 simplified block diagram

Figure 4 (a) Ramp deformed by sinusoidal applied to pin COMP and (b) magnification

With pin SLOPE loaded with a resistor and <u>not connected</u> to pin RAMP, the ramp would look fine (Figure 5)
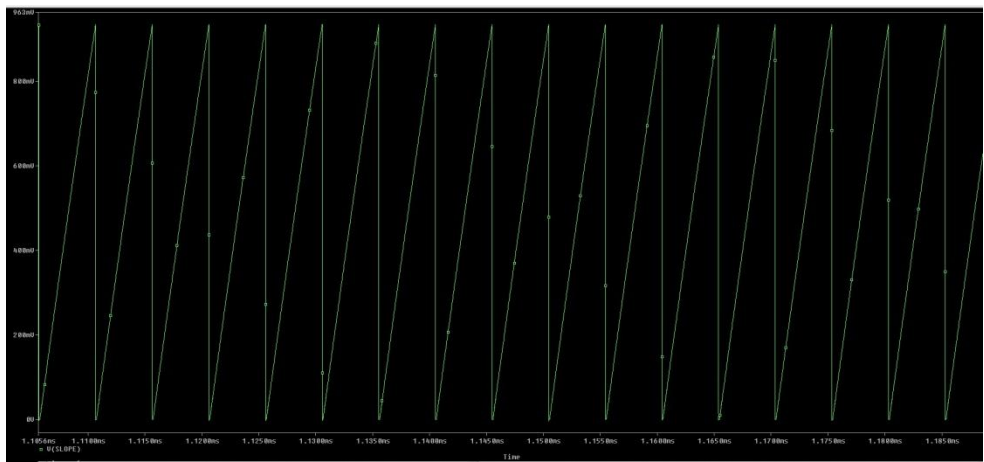

Figure 5. Output of pin SLOPE loaded with a resistor and not connected to pin RAMP

Parameters have been checked and voltage values needed for correct operation look fine, as displayed in Figure 6.
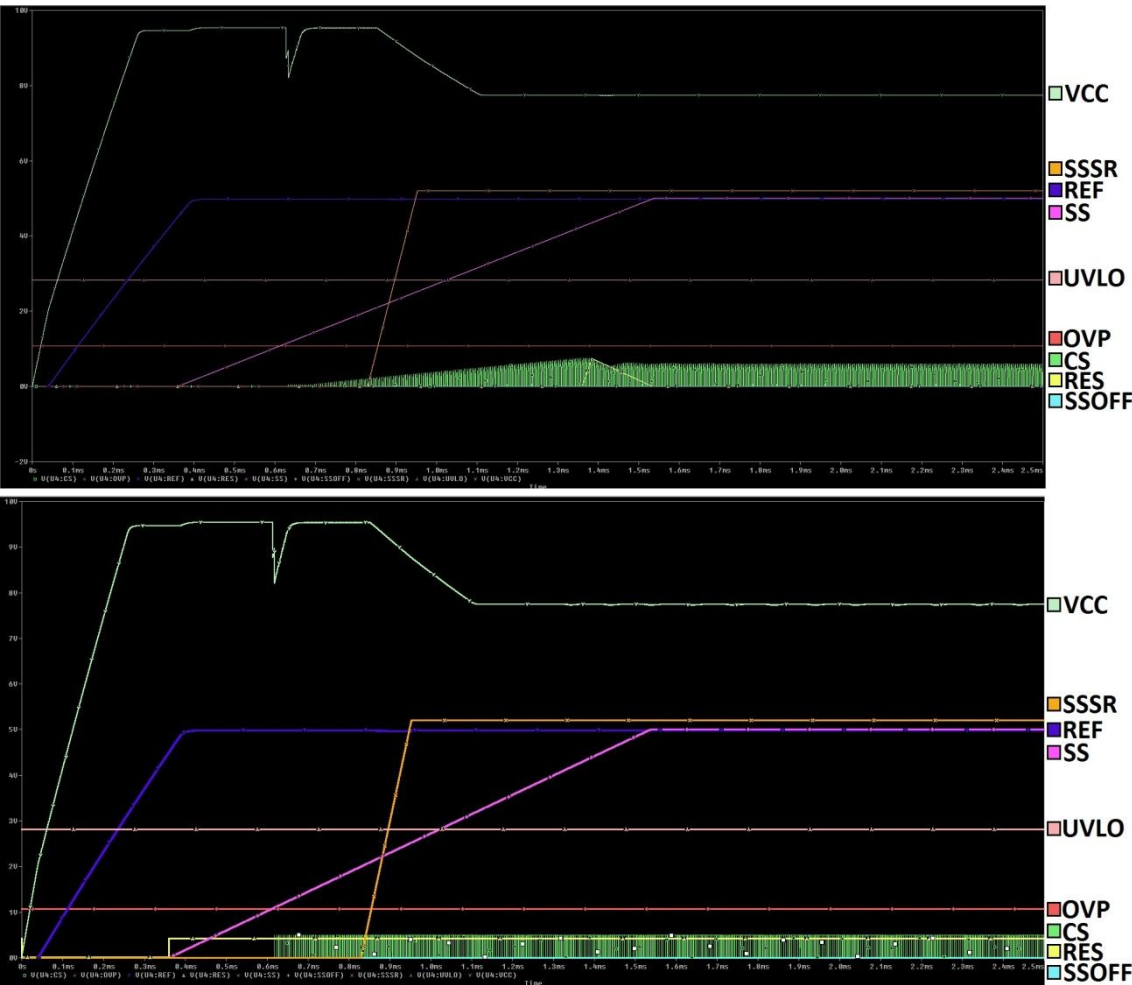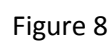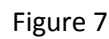

Figure 6. Control voltage waveforms

ii) Experimental Results:

On protoborad, by connecting a resistor from SLOPE to GND, we´ve got the ramp waveform. However, when pin SLOPE is tied to pin RAMP (Figure 7), the ramp waveform is completely killed, such as a grounding connection imposed by the MOSFET marked in red in Figure 8.

Figure 7

Figure 8

Initially, pins SLOPE, RAMP and CS were configured as in Figure 9(a), with corresponding waveform in Figure 9(b) and voltages listed.

SLOPE RAMP CS

Figure 9 (a)

UVLO=2.61 V

OVP= 1.03 V

REF= 4.98 V

RT= 2.00 V

RES= 0.00 V

SS= 4.94 V

SSSR= 5.48 V

VCC= 7.81 V

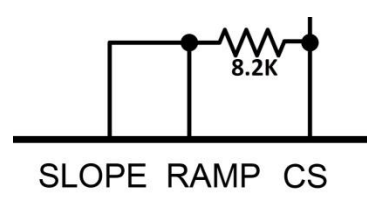SSOFF= 0.00 V

Figure 9 (b)

Now, with RAMP and SLOPE tied up (Figure 10a), the ramp waveform looks as grounded (Figure 10b)
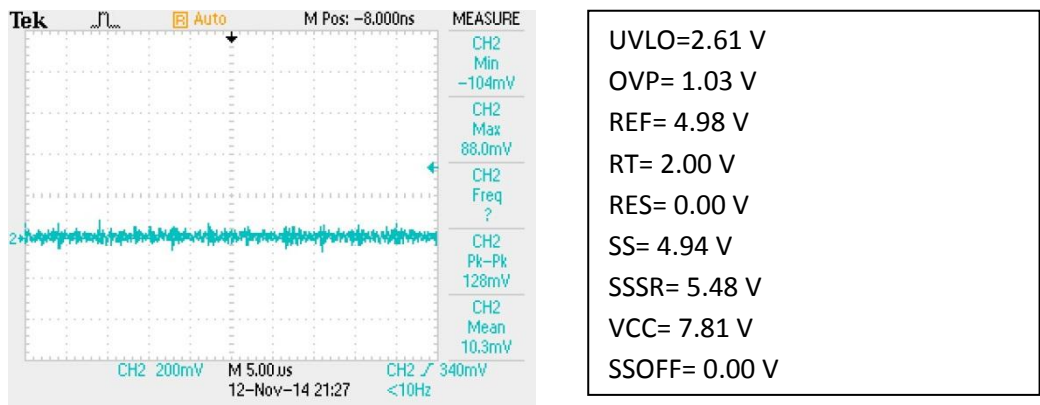

Figure 10 (a)

UVLO=2.61 V
OVP= 1.03 V
REF= 4.98 V
RT= 2.00 V
RES= 0.00 V
SS= 4.94 V
SSSR= 5.48 V
VCC= 7.81 V
SSOFF= 0.00 V

Figure 10 (b)