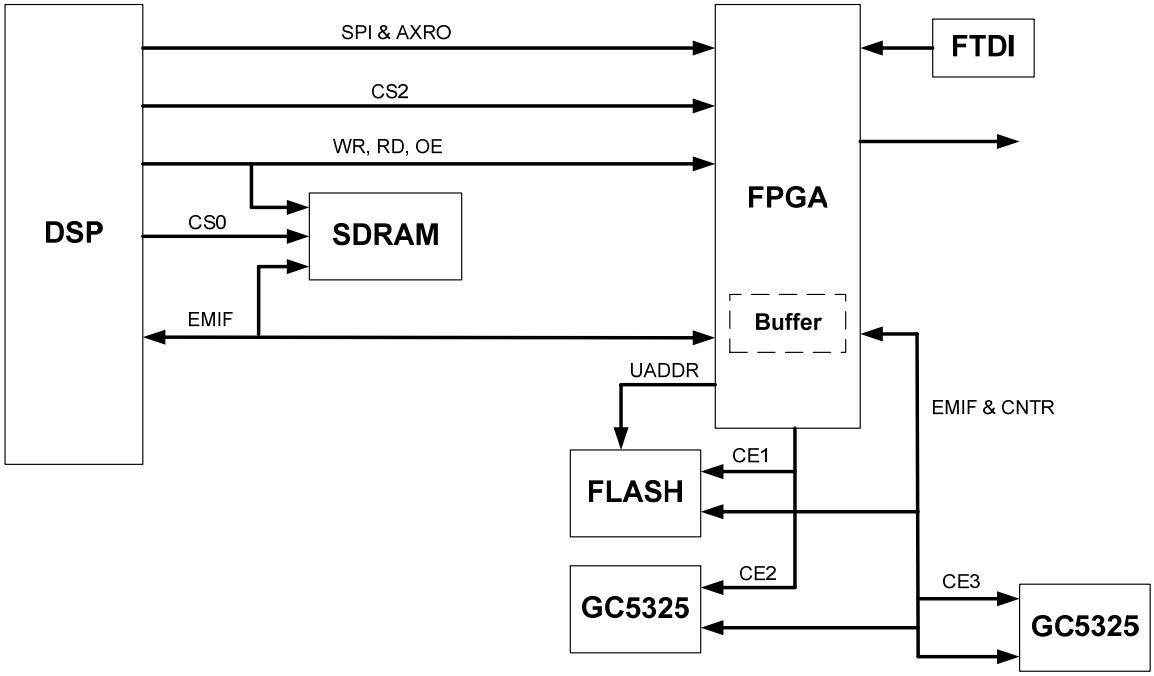
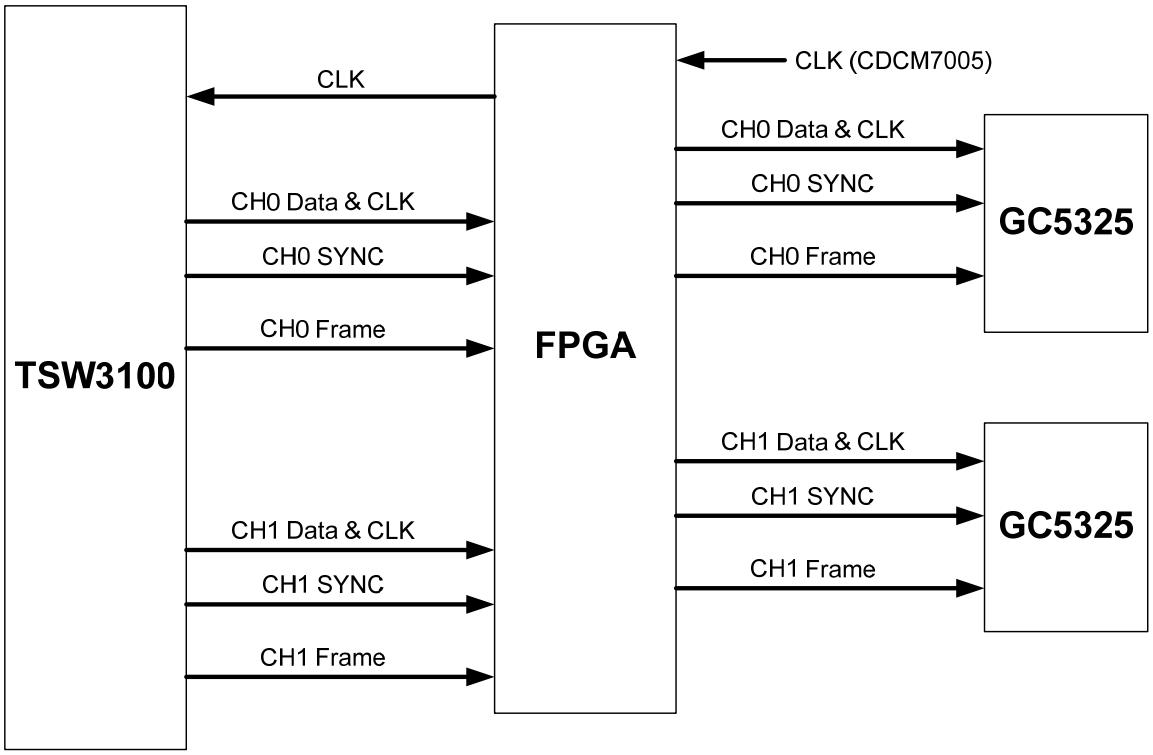
GC5325 FPGA Description



FPGA Interface Block Diagram



FPGA Baseband Block Diagram

GC5325 chip select decode table. This function is performed by the FPGA.

Dual GC5325 REV A & B Decode

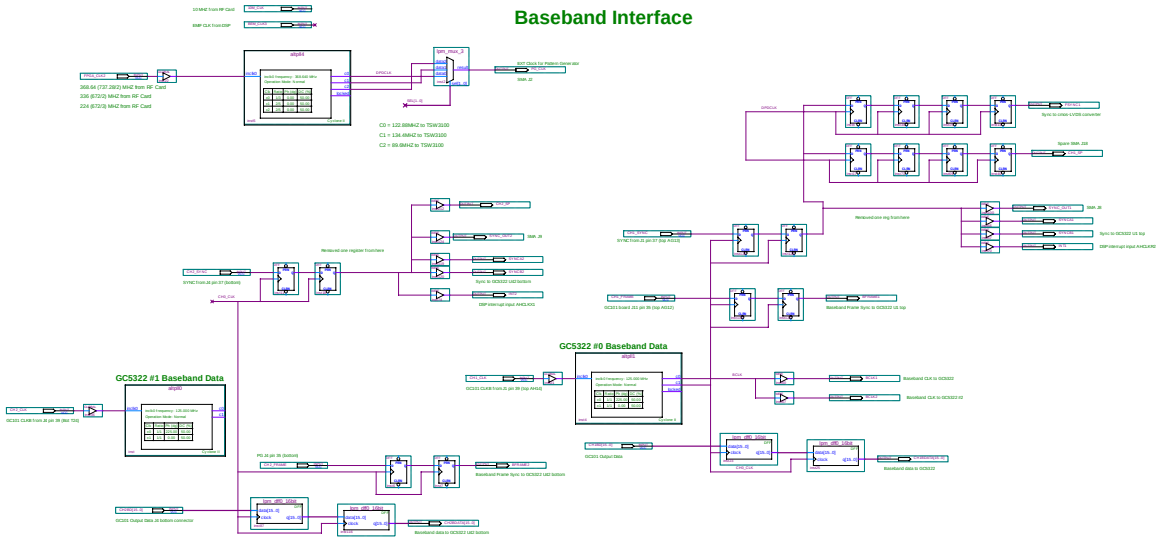
Address Decode					CE Outputs			
HD20	HD21	HD22	HD23	CS2	GC5325 #1 CE	GC5325 #2 CE	FPGA CE	FLASH CE
0	0	0	1	0	0	1	1	1
1	0	0	1	0	1	0	1	1
1	1	1	1	0	1	1	0	1
0	1	1	1	0	1	1	1	1
X	X	X	0	0	1	1	1	0

FPGA Internal Register Mapping

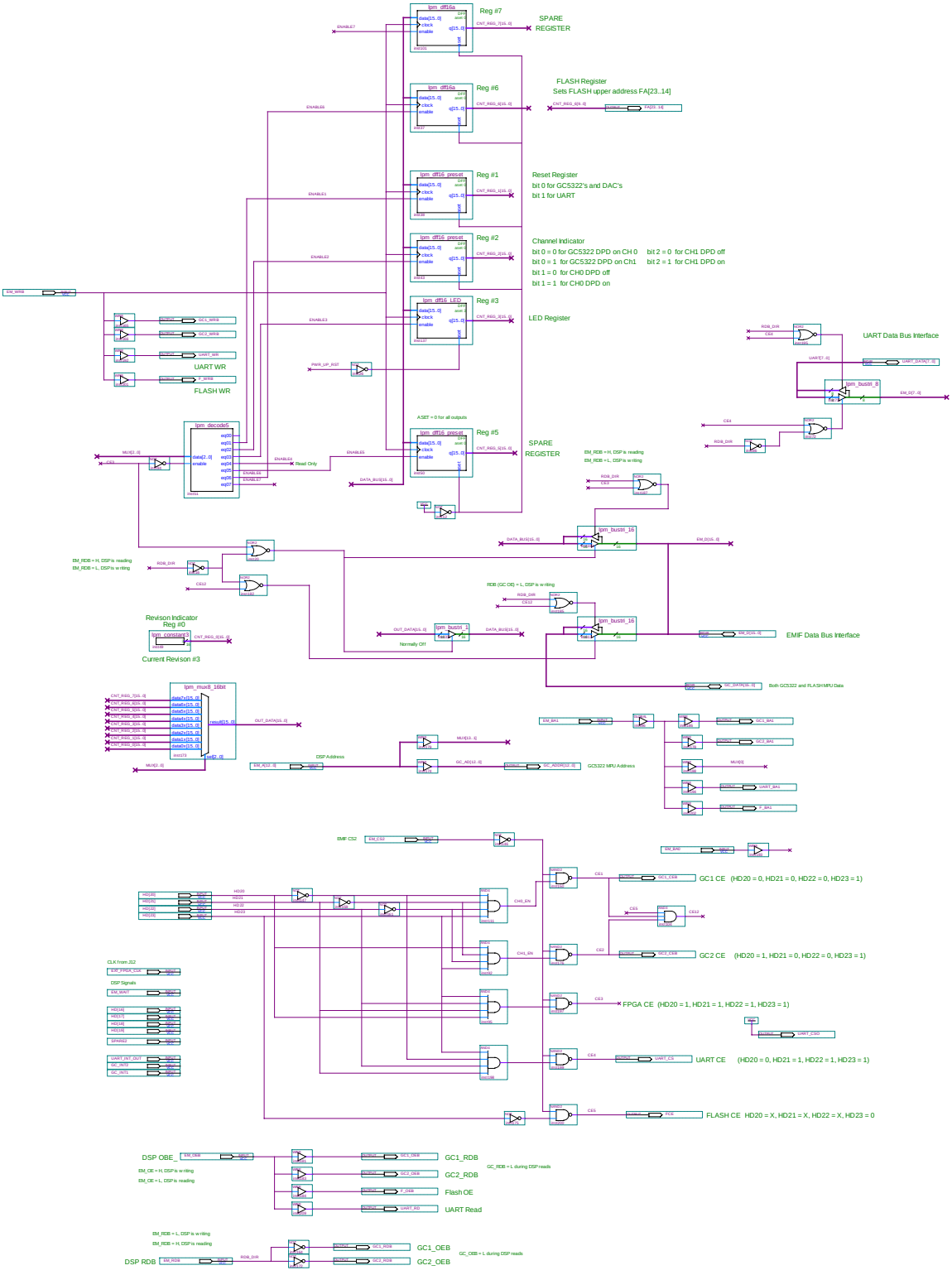
Register Name	Description	Address	R/W	Default	bits
Firmware Revision	Current firmware revision. Lower 4 bits	0x00	Read only		16
Reset	bit 0 - GC5325 and DAC reset (active low)	0x01	R/W	0	16
	bit 1 - UART reset (active high)	0x01	R/W	0	
Channel Indicator	bit 0 - Set to "0" to indicate DPD active on Ch 0. set to "1" for DPD active on Ch 1	0x02	R/W	0	16
	bit 1 – Selects RF Attenuator SPI control. Set to "0" for SPI control of CH0 attenuator. Set to “1” for FPGA control of CH0 attenuator.	0x02	R/W	0	
	bit 2 – Selects RF Attenuator SPI control. Set to "0" for SPI control of CH1 attenuator. Set to “1” for FPGA control of CH1 attenuator.	0x02	R/W	0	
LED Control	Set to "1" to turn on LED's	0x03	R/W		16
	bit 0 - Controls LED D1 (Firmware rev lsb)	0x03			
	bit 1 - Controls LED D2 (Firmware rev)	0x03			
	bit 2 - Controls LED D3 (Firmware rev)	0x03			
	bit 3 - Controls LED D4 (Firmare rev msb)	0x03			
	bit 4 - Controls LED D7 (GC config good)	0x03			
	bit 5 - Controls LED D8 (DSP tick timer)	0x03			
Dip Switch setting	bit 0 - SW5 switch 1	0x04	Read only		16
	bit 1 - SW5 switch 2	0x04			
	bit 2 - SW5 switch 3	0x04			
	bit 3 - SW5 switch 4	0x04			
Spare		0x05	R/W		16
Flash Address	bit 0 - FA[14]	0x06	R/W	0	16
	bit 1 - FA[15]	0x06			

	bit 2 - FA[16]	0x06			
	bit 3 - FA[17]	0x06			
	bit 4 - FA[18]	0x06			
	bit 5 - FA[19]	0x06			
	bit 6 - FA[20]	0x06			
	bit 7 - FA[21]	0x06			
	bit 8 - FA[22]	0x06			
	bit 9 - FA[23]	0x06			
Spare		0x07	R/W		16

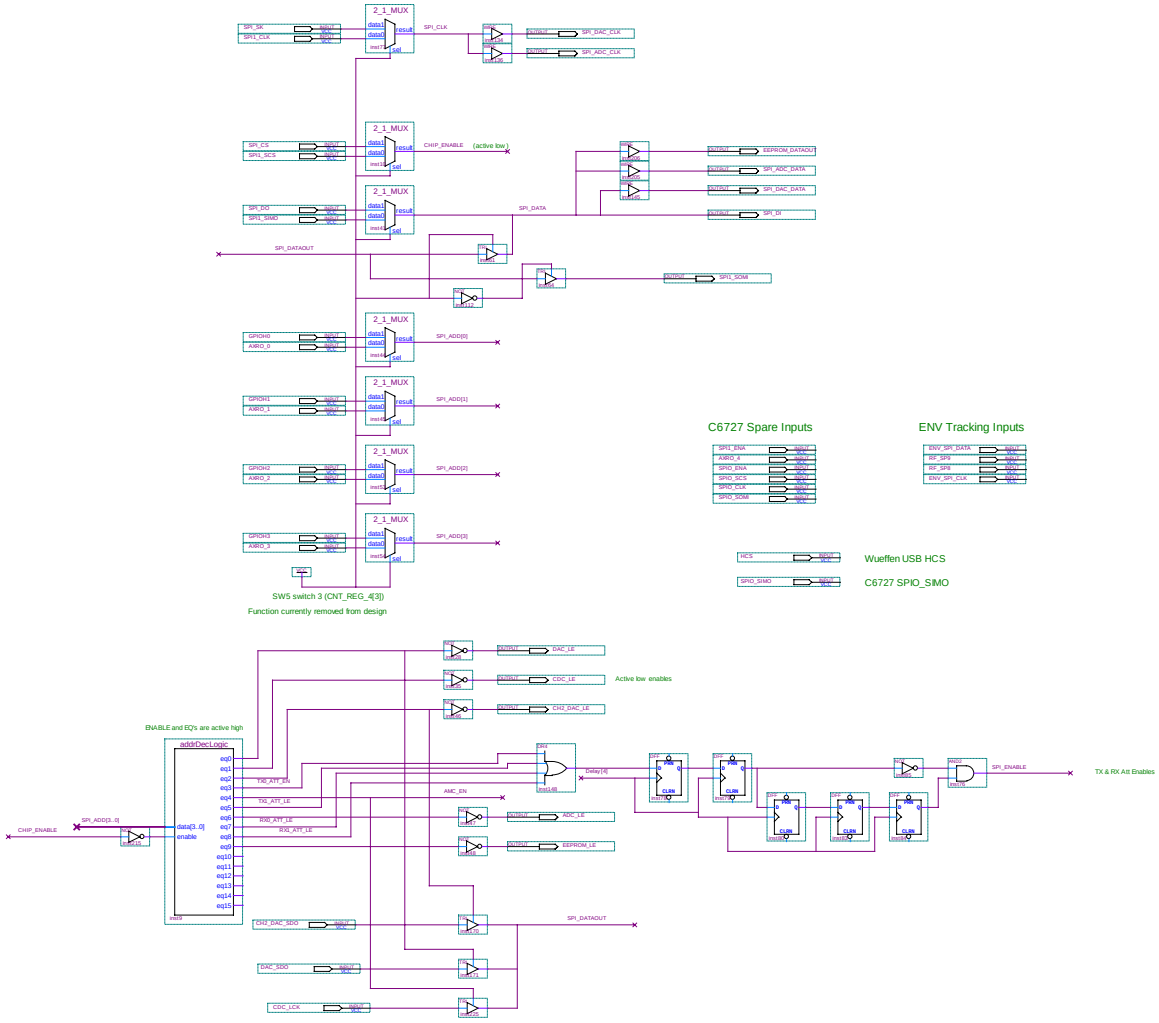
FPGA Firmware (Generated by Altera Quartus version 6.1)



DSP Interface and Internal Registers



FTDI/C6727 USB Interface to RF Board



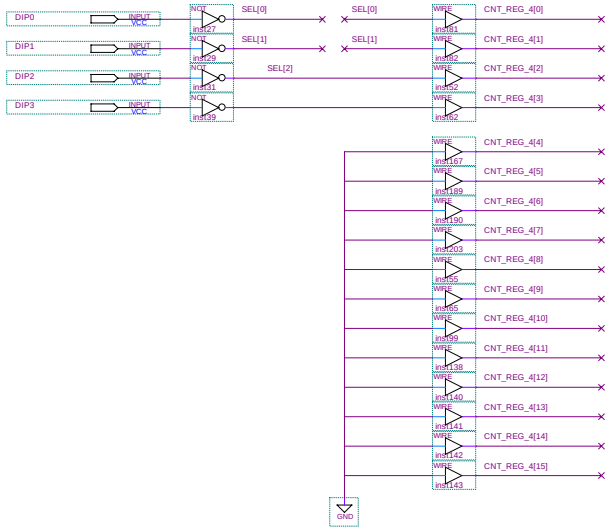
LED, DIP Switches and Test Points

(Dip Switch Open is a High level Input)

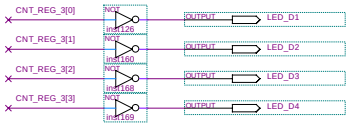
Dip Switches

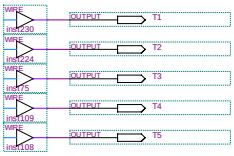
SW5

Reg #4



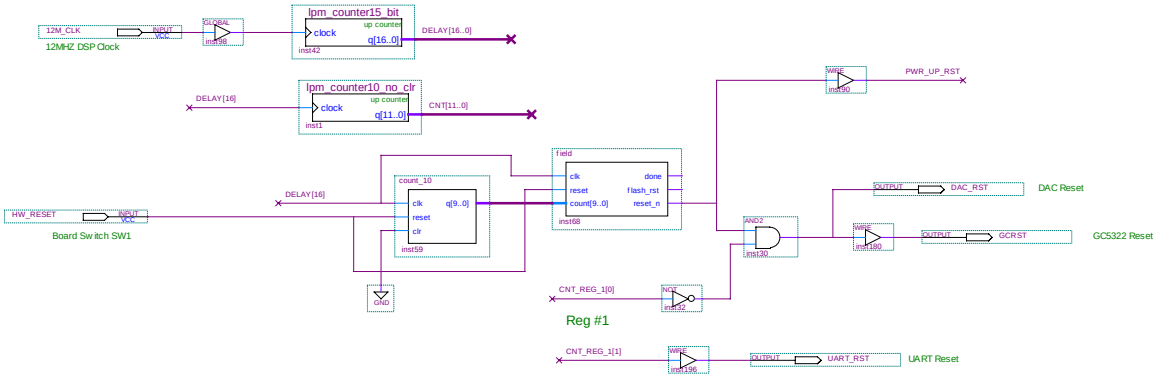
Reg #3 LED's



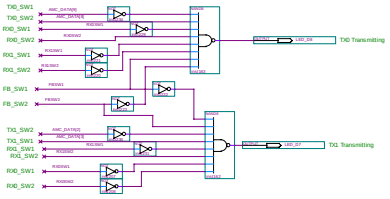


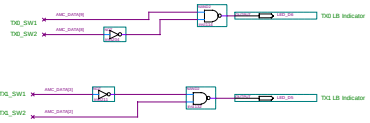
SW7

Board Reset Control

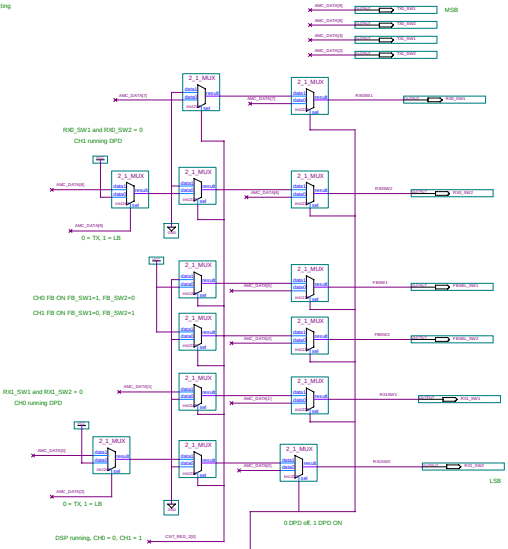


TX LED Decode





TX & RX Switch Control



TX & RX Attenuator Control