Texas Instruments

GC5330 / GC6016 Overview

April 2011

GC532x vs GC5330 - Key Product Specifications

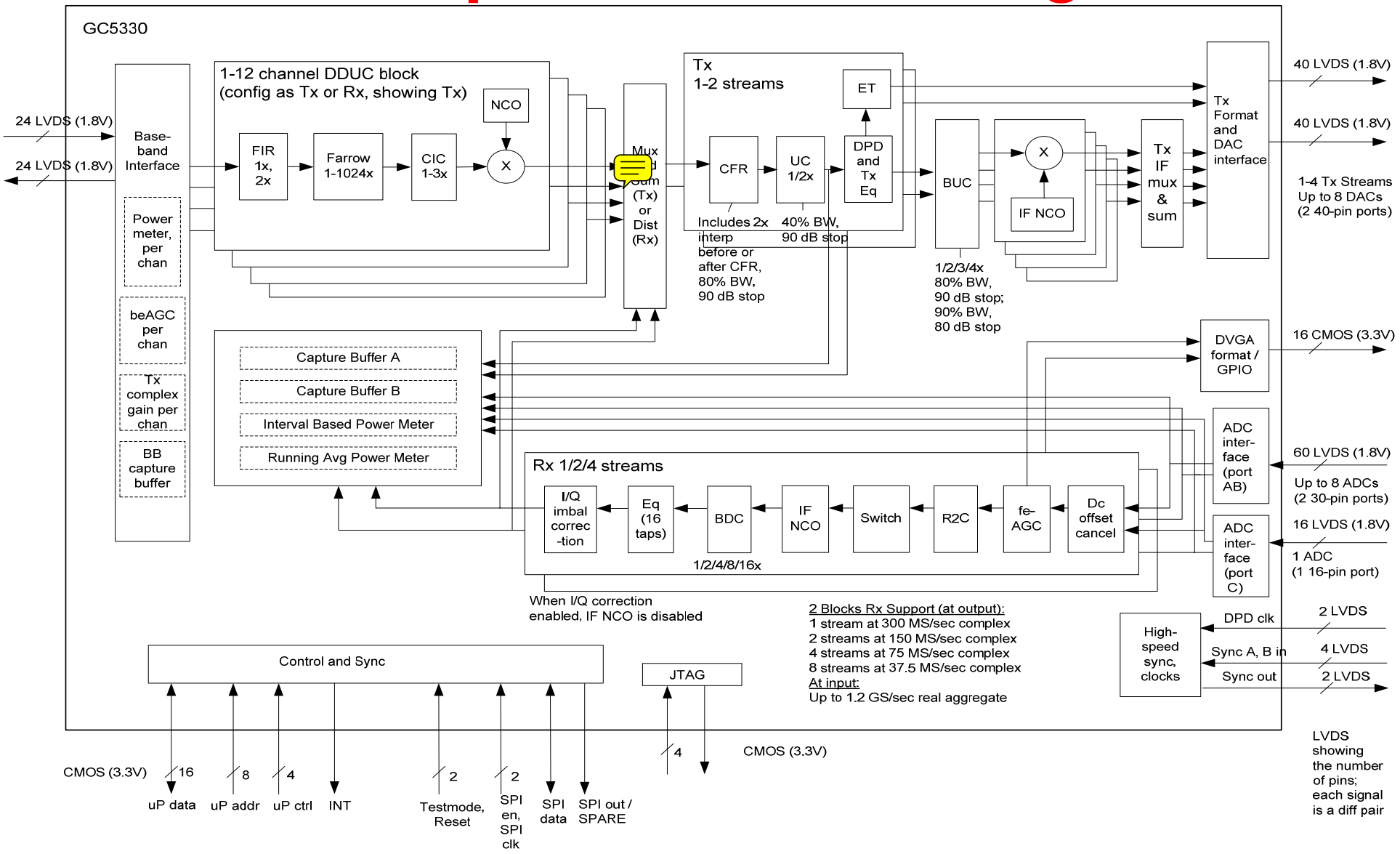
Key Requirements	GC532x	GC5330
Baseband Interface	CMOS – upto 70MhzDUC, 93Mhz 25	LVDS Tx, Rx upto 500Mbps, upto 3 rates
Number DUC channels	1, 2, 4, 12 common rate	4DDUC upto 3 unique rates Each DDUC 1-12 channels, DDUC for Tx or Rx
Block Converter, and DDC/DUC	DDC/DUC	Block Rx, DDC DUC, Block Tx
CFR	2nd generation CFR	3rd Generation CFR Pre and Post gain Additional Constant PAR, AGC
Number of Tx streams	1Tx, 1Tx and Env Tracking	1Tx(UW), 2(HP), 4(HB) 2Tx with Env Tracking
Interpolation after CFR	Resampler	Interpolate by 2, 4
DPD	Short, Long – upto 140Mhz	Multimodes, 600(1*), 300(2), 150(4)
Tx Equalizer	After DPD, 16 complex taps	17 to 34 complex taps, diff modes
DAC Interface	1DAC5682, 1DAC5688	4 DAC328x, 2DAC3484, 2DAC5682
ADC Interface	1 real, 1 complex feedback	1 real feedback 2 multiport Rx, feedback real or complex
Rx, WbAGC, DDC, NbAGC	No	Yes
Control Interface	EMIF-6727DSP	EMIF 6748DSP
Power	<3 W	<5 W, depends on channels And bandwidths

GC5016 vs GC6016 - Key Product Specifications

Key Requirements	GC5016	GC6016
ADC Converter Rates	(4)160,(2)320 MSPS	(1)1.2Ghz, 16(65Mhz)
DAC Converter Rates	(4)160	(4) 280, (2) 560Mhz
Data Converter Interface	4(Rx) or 4(Tx) or (2)each	4Rx(upto 16ADC) 4Tx (upto 4DAC)
Block Converter, and DDC/DUC	DDC/DUC	Block Rx, DDC DUC, Block Tx
Package	252-pin PBGA	484-pin PBGA
Delay adjust	Special PFIR programming	Farrow Resampler and PFIR programming
Number of ports	4	Up to 4 Tx and 8 Rx
Number of channels	4	1 to 48 (4DDUC-12channels each)
Wideband AGC	none	Yes
Control Interface	Microprocessor	3/4-wire SPI or EMIF
Power	<1 W	<3.5 W, depends on channels And bandwidths

GC5330 Specifications

GC5330 Top Level Block Diagram



GC5330 Features (1 of 3)

- **Modes**
  - 5330 – DUC + CFR + DPD; or DUC + CFR + DPD + DDC + Eq
  - 6016 – DUC + CFR or DUC + CFR DDC + Eq
  - Up to 4 Tx streams; up to 8 Rx streams
- **DUC/DDC Functionality**
  - Configurable as DUC or DDC, in 4 groups of 12 channels each
  - Trade off number of channels for BW of channels
    - For example:
      - 1 DUC and 1 DDC, each up to 155 MS/sec
      - …
      - 48 each DUC or DDC, up to 3 MS/sec
  - Four fractional resamplers for multi-rate support
  - Programmable frequency hopper
  - Decimation and Interpolation range: 1-98,304 (after R2C in Rx chain)
  - Wideband AGC (prior to DDC channels) and Narrowband AGC (after DDC channels)
  - Power meters (per channel and per node/stream)
  - MIMO/smart antenna support (per stream and per channel gain, phase, delay adjustment)
    - Per stream provided with the Tx/Rx equalizers
    - Per channel gain/phase in input formatter, per channel phase in NCO, and per channel delay in Farrow and baseband interface block

GC5330 Features (2 of 3)

- **Tx / Rx stream processing**
  - IQ imbalance correction
    - Rx, 1-tap automatic, blind correction algorithm (after Rx equalizer; assumes IF-NCO disabled)
    - Host based external algorithm, using capture buffers – can be used to implement training based algorithms – for cases where poor signal statistics, or frequency dependent correction desired
  - Rx equalizer (16-taps), Tx equalizer (17-34 taps, depending on mode)
    - Tx path linear pre-distortion
    - I/Q imbalance correction (freq. dependent, determined externally and programmed into coefficients)
    - Gain/phase/delay adjust
    - Equalization of analog signal paths (e.g. DAC sin(x)/x correction)
  - Tx CFR
    - All WI signal types
    - Automatically handles frequency hopping
  - Tx DPD
    - Longer sample memory span than GC5322 for “diagonal terms” + extensive set of additional Volterra “cross terms”
    - Sub-sampled option
    - ET support (2 Tx, 30 MHz)
  - Power monitor / PA protection features
    - Power monitoring at the DPD input, DPD output, and Feedback path output
    - Option for hardware generated interrupt based on power level relative to a programmed threshold
      - Based on interrupt condition, optional gain reduction on Tx output signal

GC5330 Features (3 of 3)

- **Capture buffers**
  - Two 4k-word capture buffers for DPD adaptation, equalizer adaptation, diagnostics (e.g. observation of ADC samples)

- **General Specifications**
  - Power < 4-5W, all blocks on, at full-speed, all channels and streams
  - Power scaling capability for unused (or inactive) channels and lower data rates
  - 3/4-wire SPI or 28-pin microprocessor programming interface (CMOS 3.3V)
    - Parallel interface
      - 8 address, 16 data, 4 control
      - Paged (128 global registers and 256 pages, with 128 regs each) and auto-increment modes
  - Core voltage: 1.1V, LVDS power 1.8V, CMOS power 3.3V
  - Package – higher power (GC5330), lower power (GC6016)
    - Both are 484-ball 23 x 23 mm PBGA

GC5330/GC6016 Data Converter Interfaces

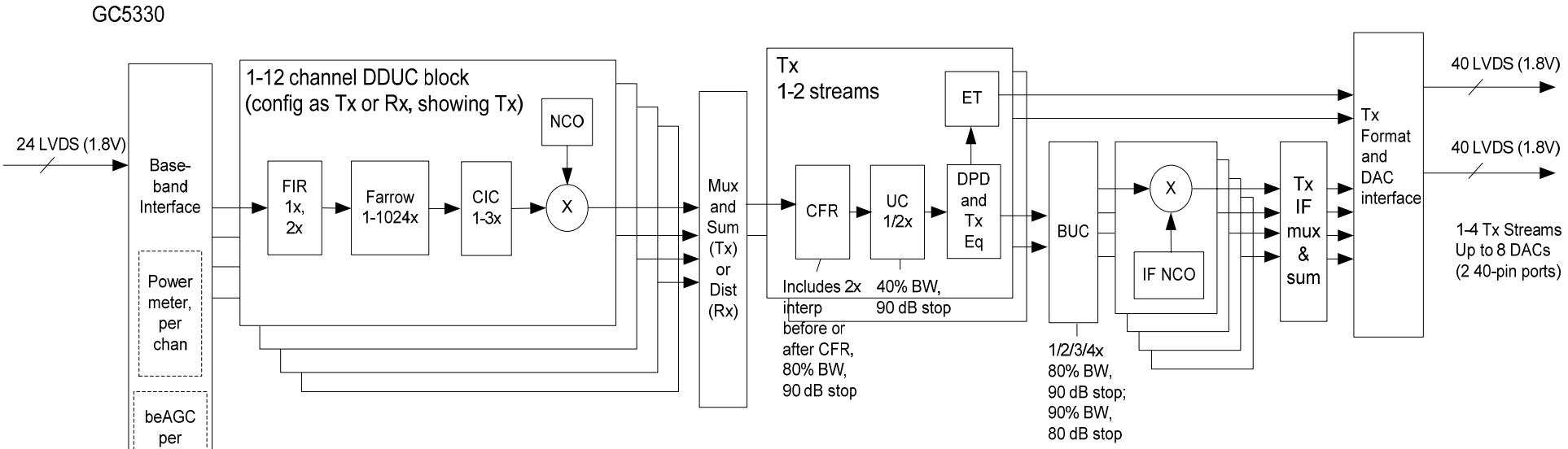
- **DAC digital interface**
  - 80 pins (40 diff pairs): LVDS outputs (1.8V supply)
  - 16-bit DACs, up to 921 MS/sec (complex or real)
  - In 2 or 4 antenna modes, max throughput of 921 MS/sec complex for all streams
  - Seamless interface to TI DACs (3282/3, 5682, and quad-DAC)

- **ADC digital interface**
  - 76 pins (38 diff pairs): LVDS inputs with internal termination (1.8V supply)
  - 16-bit ADCs, up to 1.2 GS/sec (real)
  - Maximum 1.2 GS/sec (600 MS/sec complex) total throughput for all streams
  - Maximum of 5 ADC chips supported (could be up to 9 ADCs total by using dual, quad ADCs, etc.)
  - Seamless interface to multiple ADC configurations
  - DVGA control (3.3V CMOS)

GC5330 BB Interface Modes

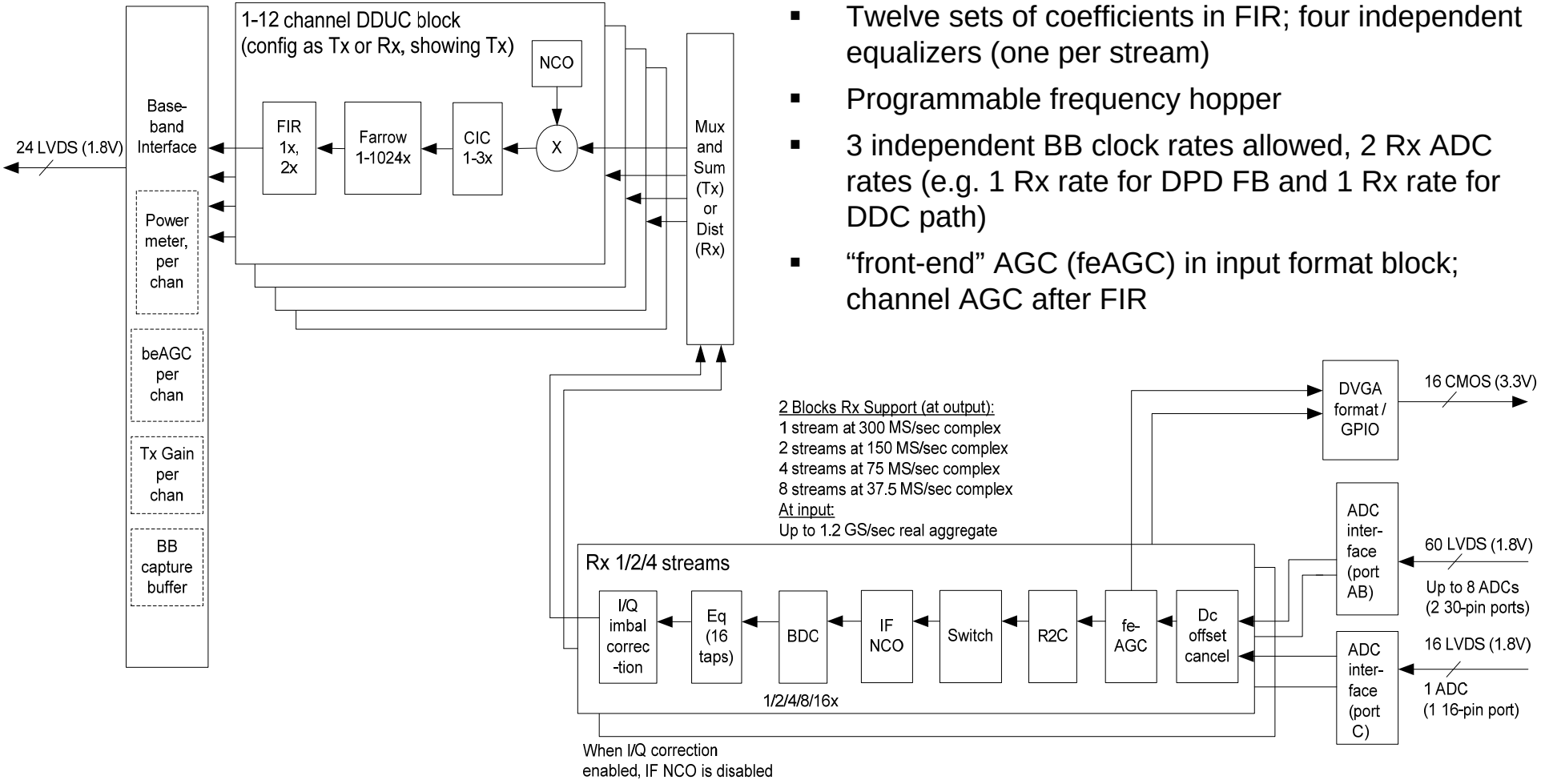
- Input (Tx)
  - 24 pins (12 diff pairs): LVDS inputs (1.8V supply)
  - Byte, nibble, and serial (2 data lines) modes
  - Can support 3 independent clock rates
  - Maximum sample rate 155 MS/sec complex
- Output (Rx)
  - 24 pins (12 diff pairs): LVDS outputs (1.8V supply)
  - Byte, nibble, and serial (2 data lines) modes
  - Can support 3 independent clock rates
  - Maximum sample rate 155 MS/sec complex
  - 3 data formats:
    - Floating point (6, 7, 14, or 16-bit mantissa, 4-bit exponent)
    - Fixed point without gain word (8, 9, 16, 18-bit options)
    - Fixed point with gain word (8 or 9 data, plus 16-bit gain word)

GC5330 Tx Mode



- Same interpolation factor for all channels; different time offset allowed in Farrow
- Twelve sets of coefficients in FIR; two independent CFR/DPD paths (per block)
- Programmable frequency hopper
- 3 independent BB clock rates allowed, 1 Tx DAC rate
- Up to 307 MS/sec out of mux and sum; up to 921 MS/sec total throughput out of BUC and output formatter (complex or real)

GC5330 Rx Mode

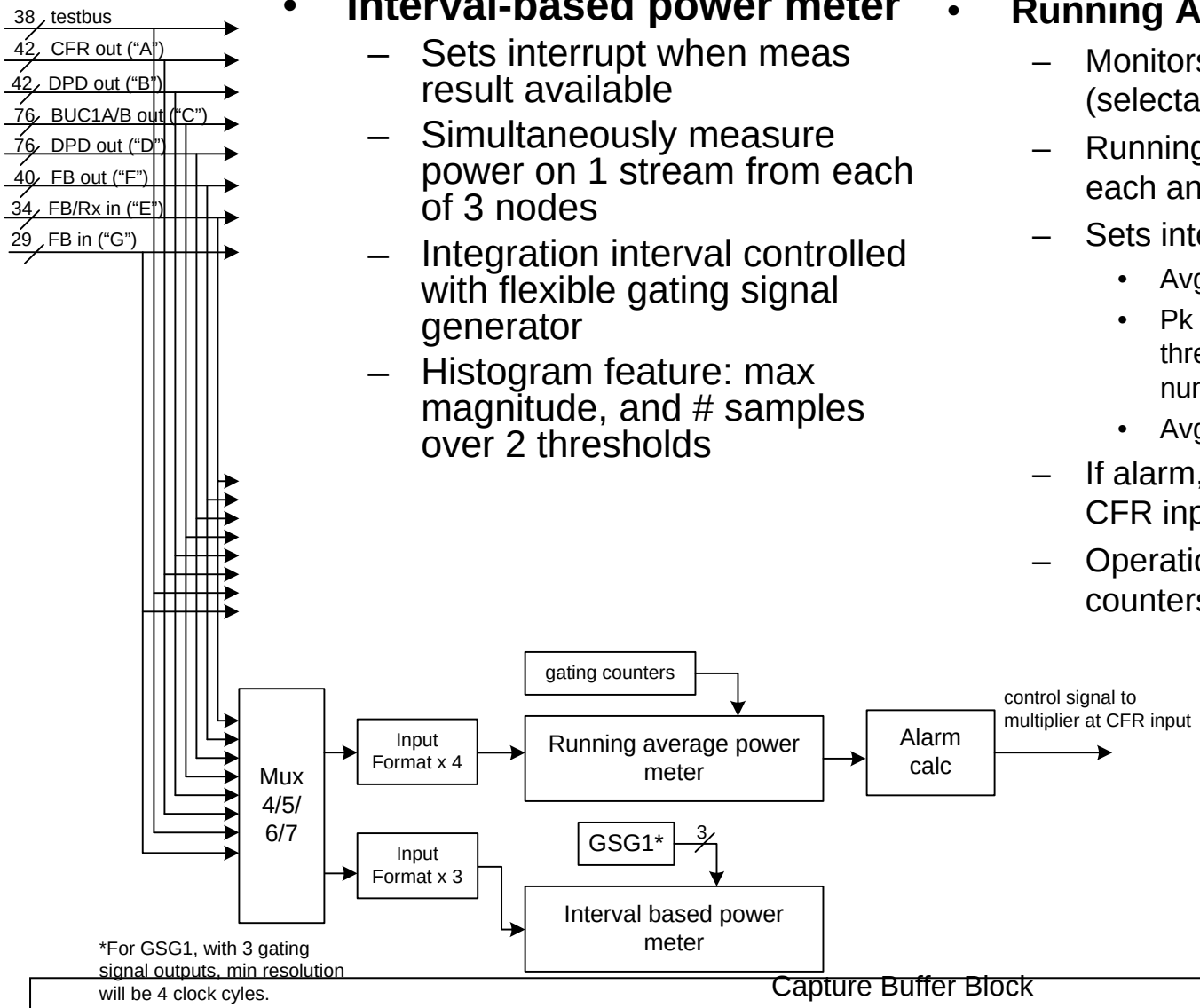


- Same decimation factor for all channels per block; different time offset allowed in Farrow
- Twelve sets of coefficients in FIR; four independent equalizers (one per stream)
- Programmable frequency hopper
- 3 independent BB clock rates allowed, 2 Rx ADC rates (e.g. 1 Rx rate for DPD FB and 1 Rx rate for DDC path)
- “front-end” AGC (feAGC) in input format block; channel AGC after FIR

Power Monitors / PA Protection

- **Interval-based power meter**
  - Sets interrupt when meas result available
  - Simultaneously measure power on 1 stream from each of 3 nodes
  - Integration interval controlled with flexible gating signal generator
  - Histogram feature: max magnitude, and # samples over 2 thresholds

- **Running Avg power meter**
  - Monitors 4 streams on a single node (selectable)
  - Running average and peak count for each ant stream
  - Sets interrupt on alarm condition
    - Avg power > or < thres
    - Pk count: # power vals above a threshold in a window exceeds prog number
    - Avg or Pk meas true
  - If alarm, can reduce signal gain at CFR input
  - Operation interval controlled with 3 counters as in 5322



DDUC

GC5330 Fractional Resampler Performance

- Each fractional resampler filter supports 1 real channel or 1-12 complex channels
- Decimation and interpolation factors from 1-1024x
- Performance
  - 95 dB stopband (accounting for droop) in range +/- 0.25 Fs, passband droop <0.1 dB
  - 83 dB stopband (accounting for droop) in range +/- 0.375 Fs
  - 56 dB stopband (accounting for droop) in range +/- 0.4 Fs, (passband droop ~4-5 dB)

GC5330 PFIR Filter

- 1 or 2x Decimation, Interpolation
  - 18bit data path, 18bit coefficients
  - Number of coefficients is 39 to 399 depending on number of channels in DDUC, ratio, number of stored filters, and computation clocks
  - Typical application
    - LTE20, 2 channels per DDUC common PFIR coef. - 79
    - LTE10, 4 channels per DDUC 2 sets PFIR coef. – 79
    - WCDMA, 6 channels per DDUC 2 sets PFIR coef. - 159
    - CDMA, 12 channels, non symmetric per DDUC 1 sets PFIR coef. - 120

CFR

GC5330 CFR

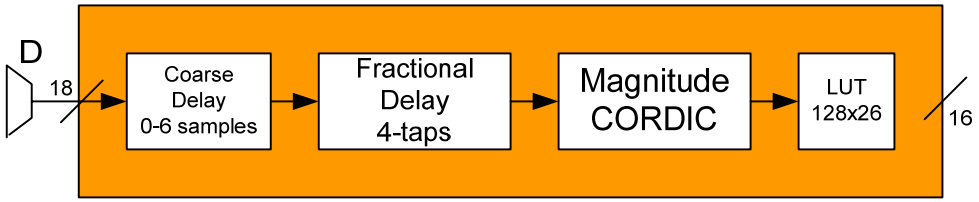
- **Next generation CFR algorithm provides the following improvements relative to the GC1115/GC5322**
- Enhanced PAR reduction and ACLR on narrowband signals such as MC-GSM
- Supports hopping signals (e.g. MC-GSM) without any interaction with the host or any external processor (unlike the GC5322)
- Provides a “constant PAR” mode in addition to a “constant peak power” mode as in the GC5322
- Supports setting of different target PAR levels for different time-slots in a signal (preamble vs. data vs. midamble, etc.)
- CFR input-to-output power tracking mode
- Flexible interpolation options before and after CFR to allow for optimum selection of signal oversampling ratio at CFR
- Up to 25% reduced latency compared to the 5322 CFR

DPD

GC5330 DPD

- **The GC5330 supports two modes of DPD operation depending on application: High Performance (HP-DPD) and High Bandwidth (HB-DPD) Modes**
  - **High Performance Mode**: Total 300 MHz DPD BW (60 MHz signal BW, assuming 5x expansion)
    - 1 TX stream @ 60 MHz
    - 2 TX streams @ 30 MHz each
    - 4 TX streams @ 15 MHz each
    - This mode provides more extensive nonlinear correction or longer DPD memory and is suitable for the most difficult and high performance DPD requirements or increased memory depth.
  - **High Bandwidth Mode:** increases total DPD BW to 600MHz (120MHz total signal BW, assuming 5X expansion BW)
    - 1 TX stream @ 60 MHz
    - 2 TX streams @ 60 MHz each
    - 4 TX streams @ 30 MHz each
    - Some restriction on CFR performance and number of non-linear DPD terms that can be used compared to high performance mode
    - DPD High bandwidth mode performance of GC5330 is better than GC5322
    - CFR High bandwidth mode of GC5330 can be slightly worse than GC5322 depending on sample rates.

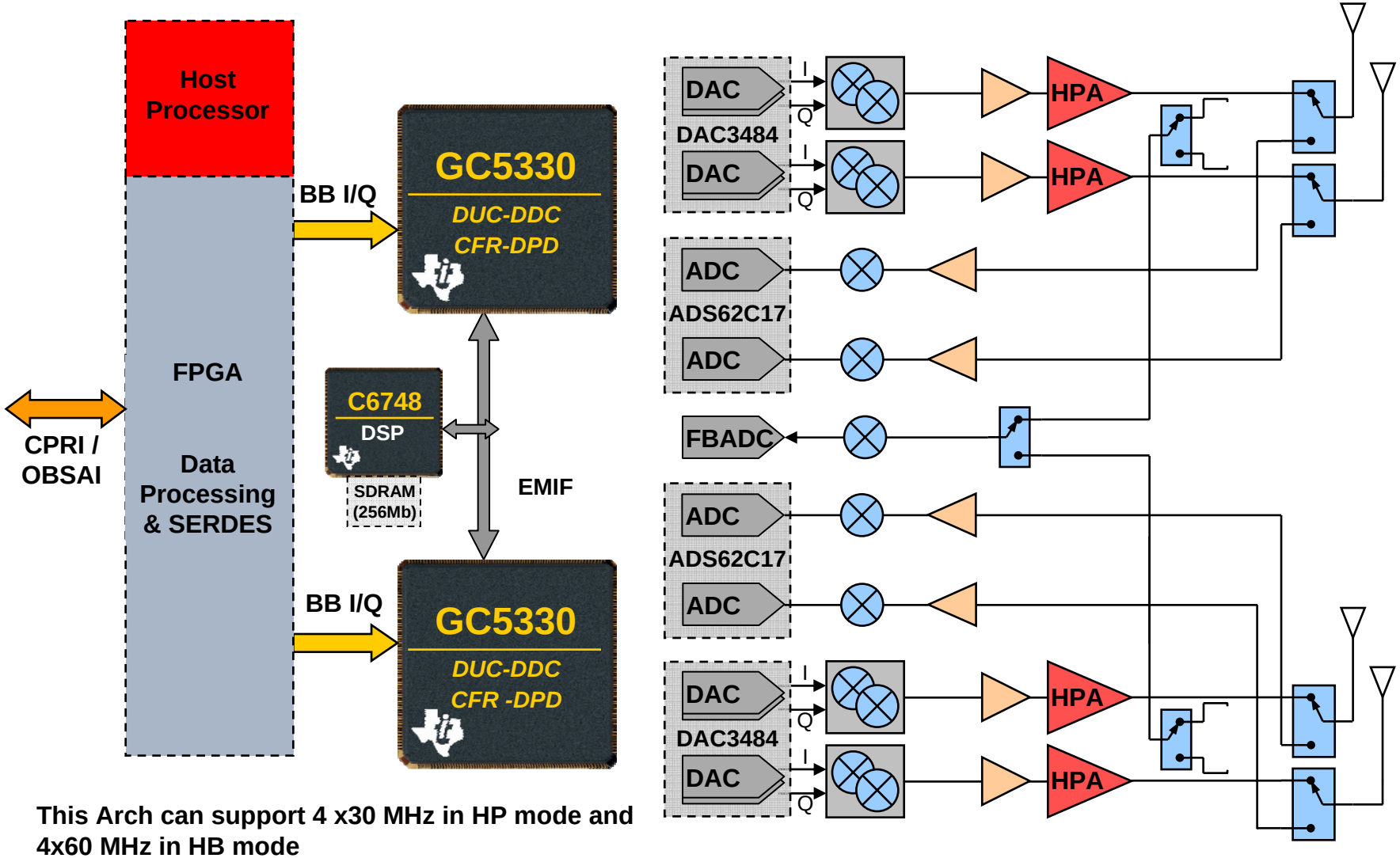
GC5330 ET



- Supports 2 Tx streams, up to 155 MS/sec each, 10, 12, or 14-bit real magnitude output (intended to support 30 MHz signal bandwidth for each stream)
- Interface – LVDS (reuse DAC interface pins) – two modes
  - Half-word DDR mode (1 or 2 antenna streams)
  - Full-word SDR mode (1 antenna stream)
- Coarse delay provides ability to track delay variation (that exceeds 1 sample time) in the ET modulator path due to effects such as temperature variation
- Fractional delay tracks delay variation within +/- 0.5 sample on the ET modulator path
- LUT provides the ability to correct for memoryless nonlinearity in the ET modulator path

Example GC5330 Configurations

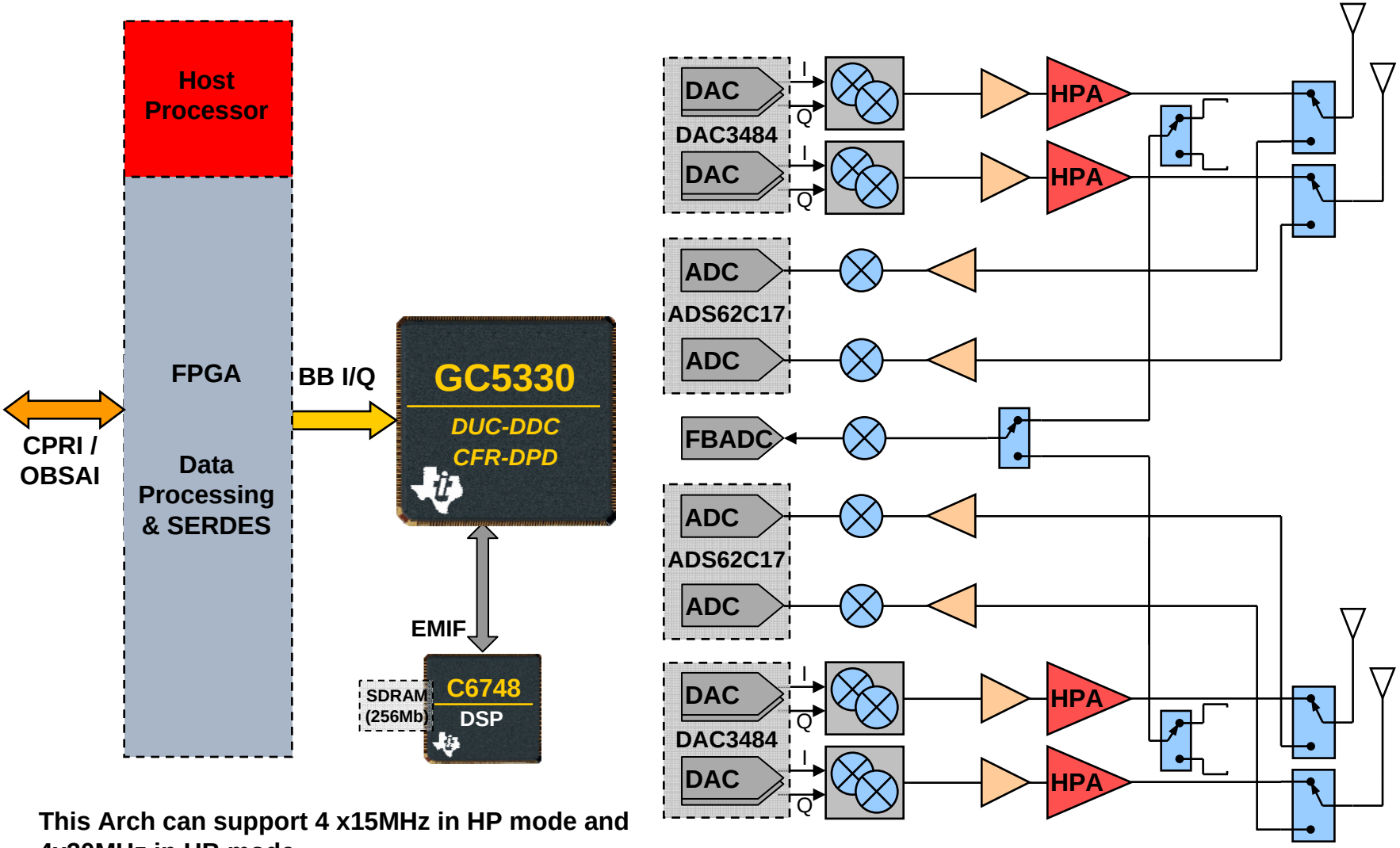
GC5330 4 Tx and 4 Rx will support ET



This Arch can support 4 x30 MHz in HP mode and 4x60 MHz in HB mode

48 TX and RX channels (12 channels per ANT)

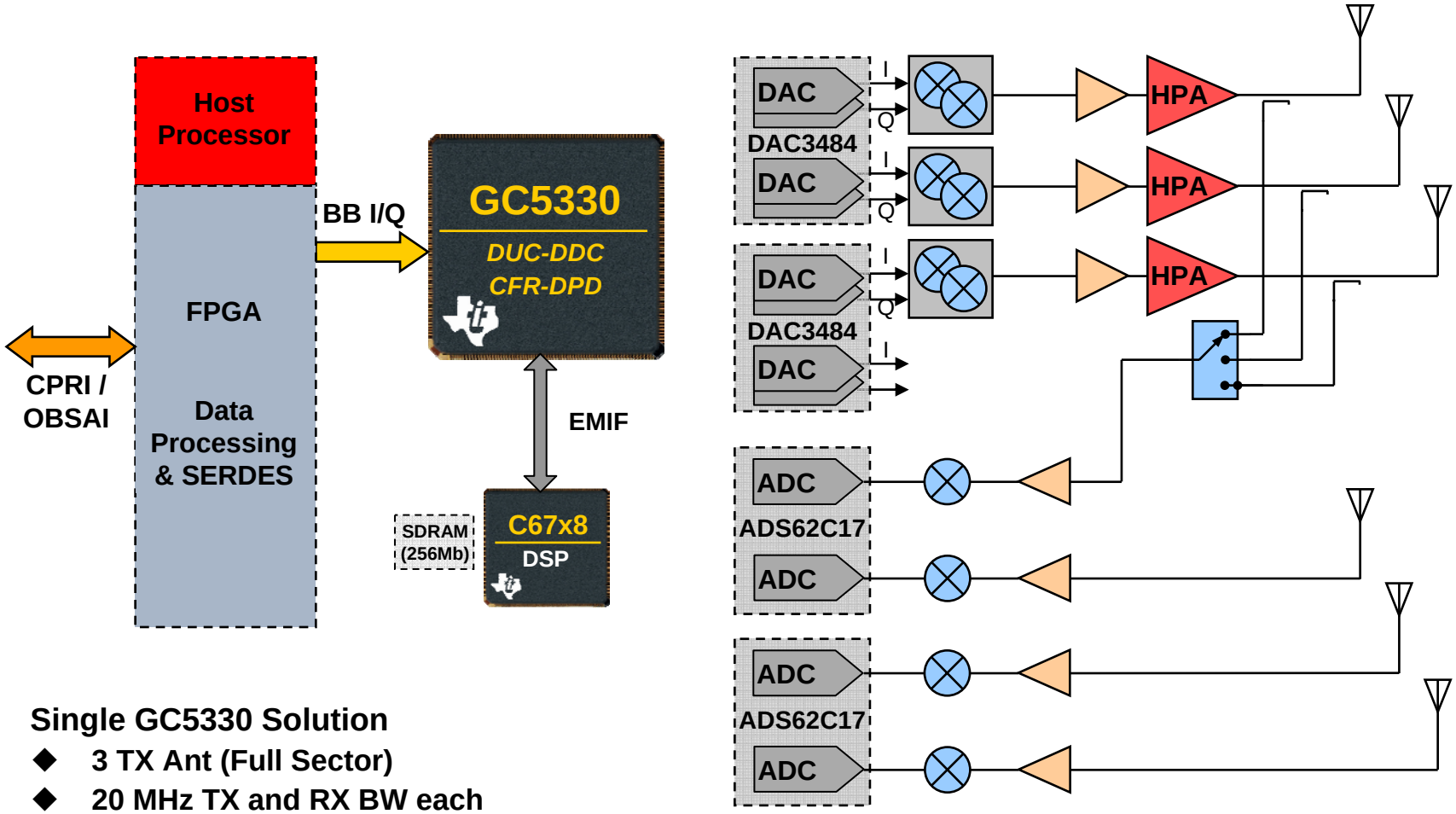
GC5330 4 Tx with 4 Rx no ET



This Arch can support 4 x15MHz in HP mode and 4x30MHz in HB mode

24 TX and RX channels (6 channels per ANT)

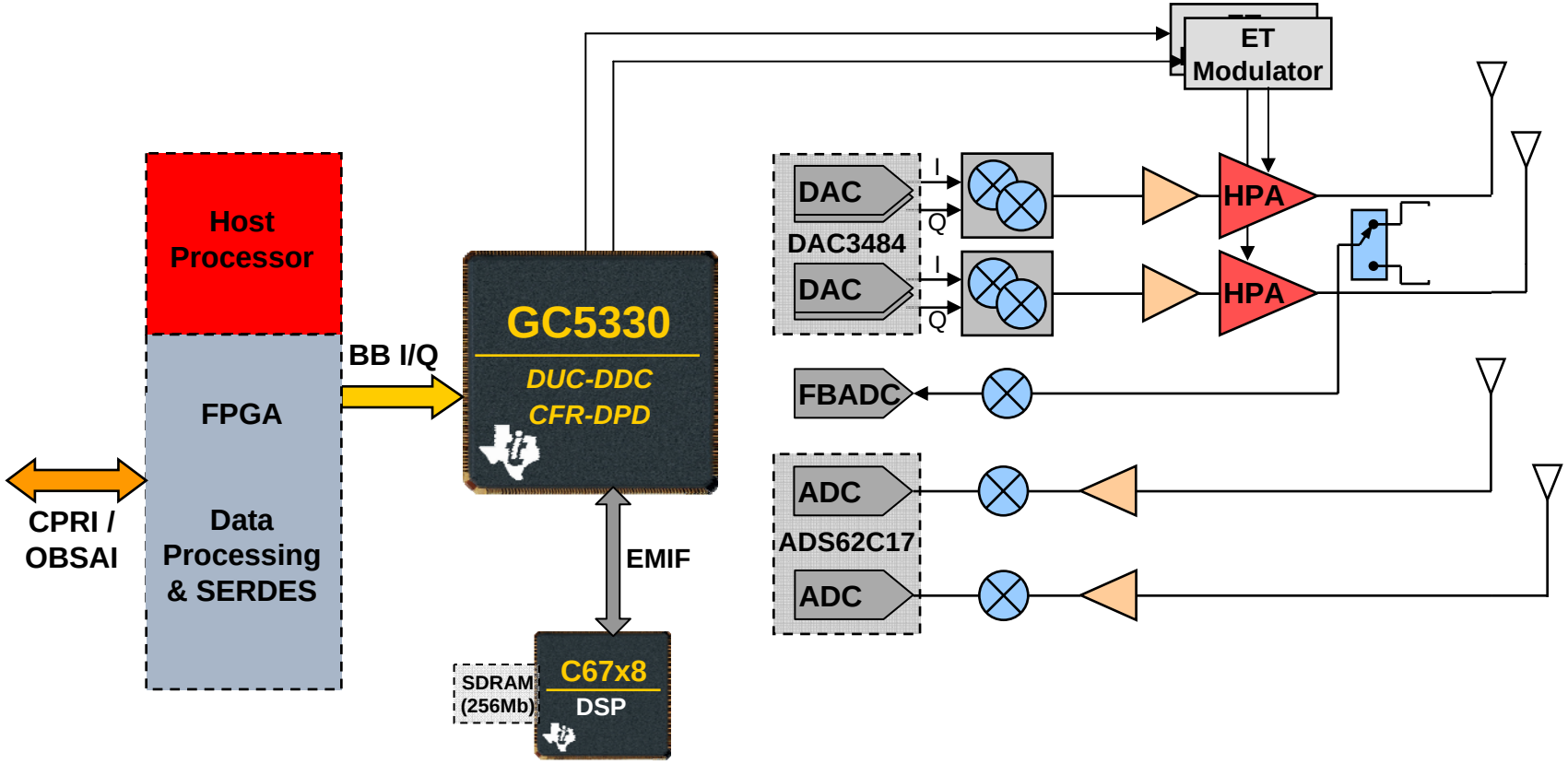
Single Chip GC5330 Full Sector RRU Solution



Single GC5330 Solution

- 3 TX Ant (Full Sector)
- 20 MHz TX and RX BW each
- 4 Carriers per Ant
- Can add diversity

GC5330 2x2 MIMO LTE Configuration with ET

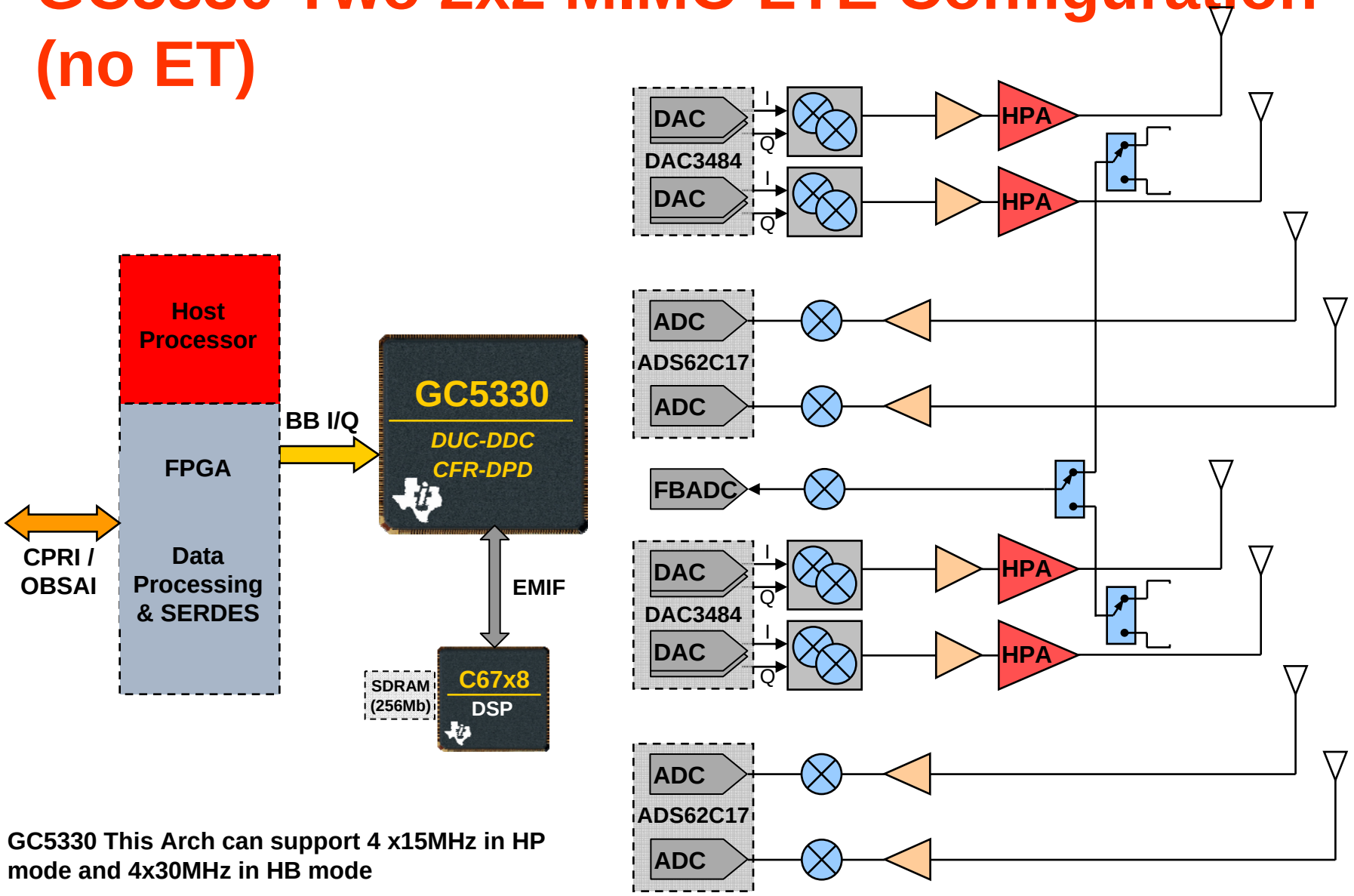


GC5330 This Arch can support 2 x30MHz in HP mode and 2x60MHz in HB mode

24 TX and RX channels(12 channels per ANT)

Note DSP can be shared for up to 4 GC5330

GC5330 Two 2x2 MIMO LTE Configuration (no ET)



GC5330 This Arch can support 4 x15MHz in HP mode and 4x30MHz in HB mode

24 TX and RX channels total (6 channels per ANT)