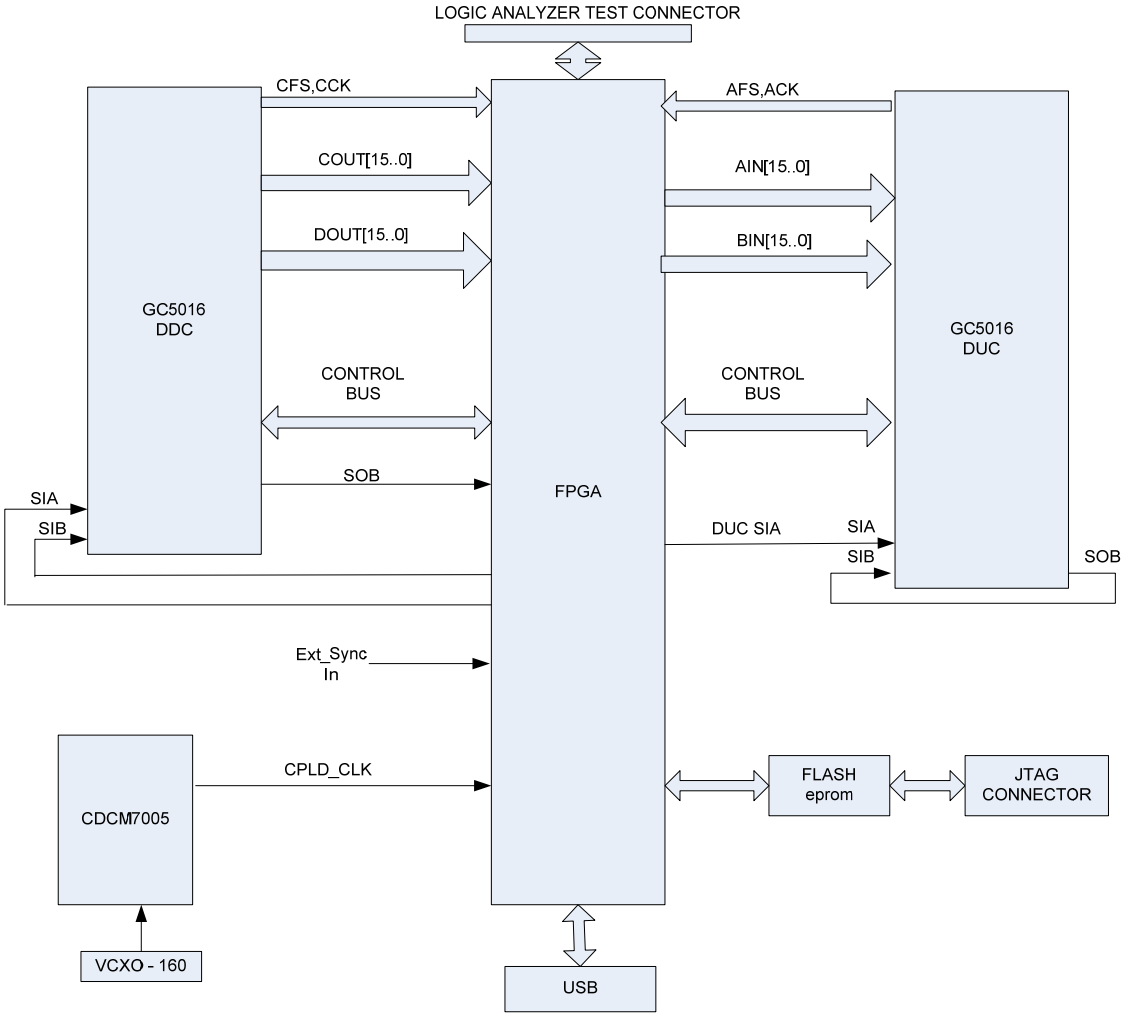
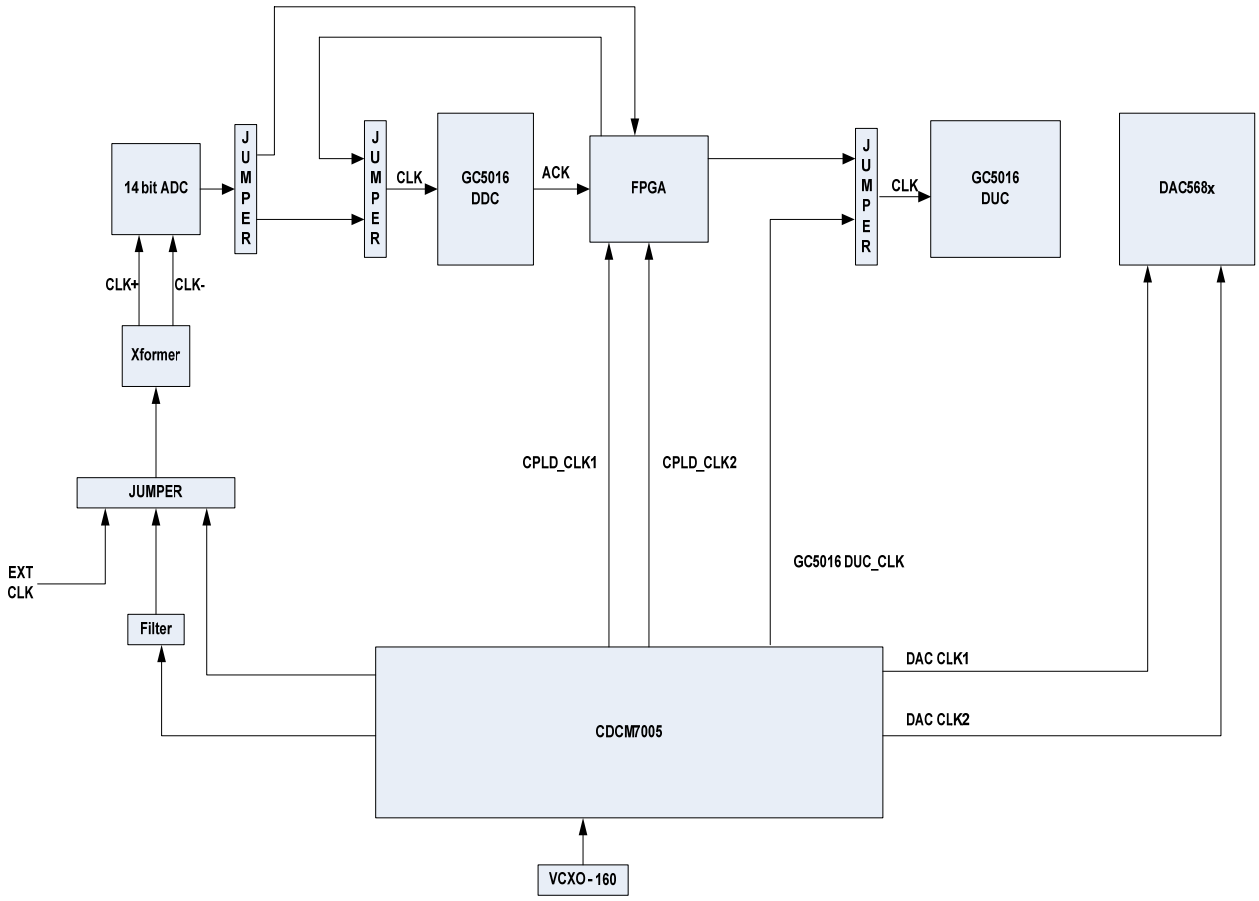
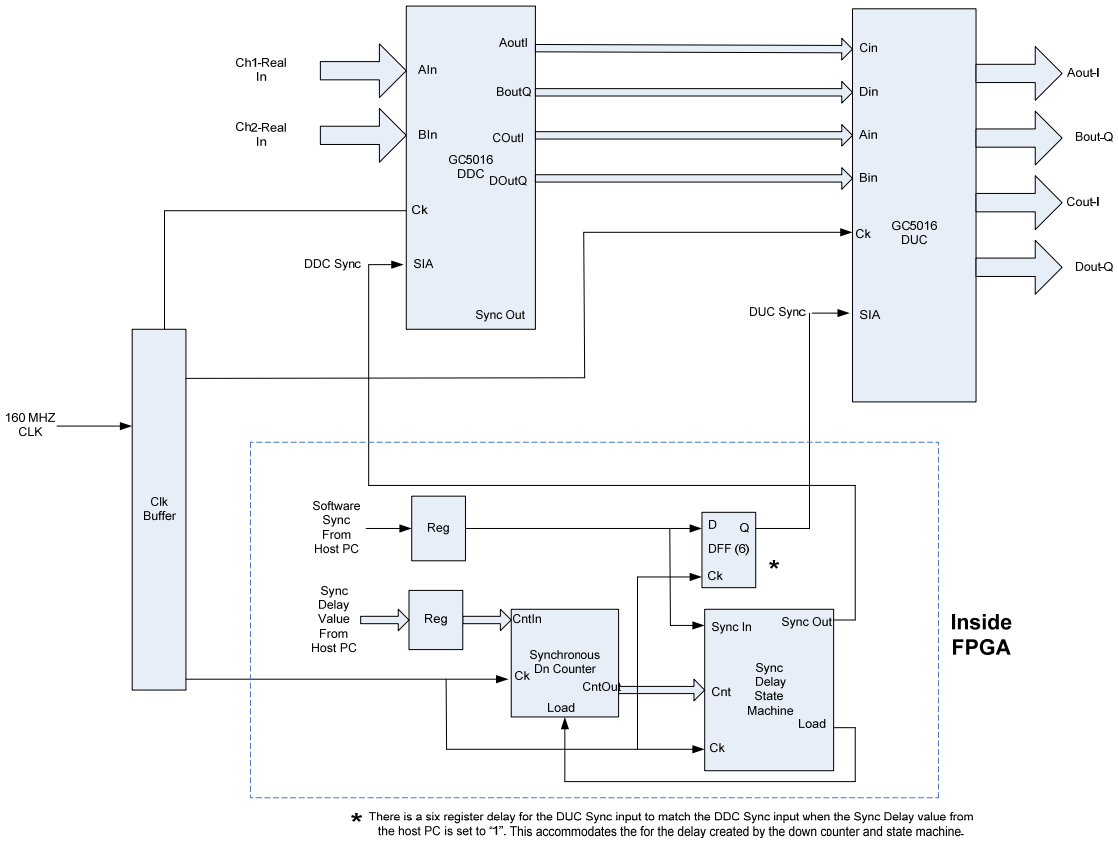
TSW4100 FPGA Description



TSW4100 FPGA Block Diagram



TSW4100 Clocking Block Diagram

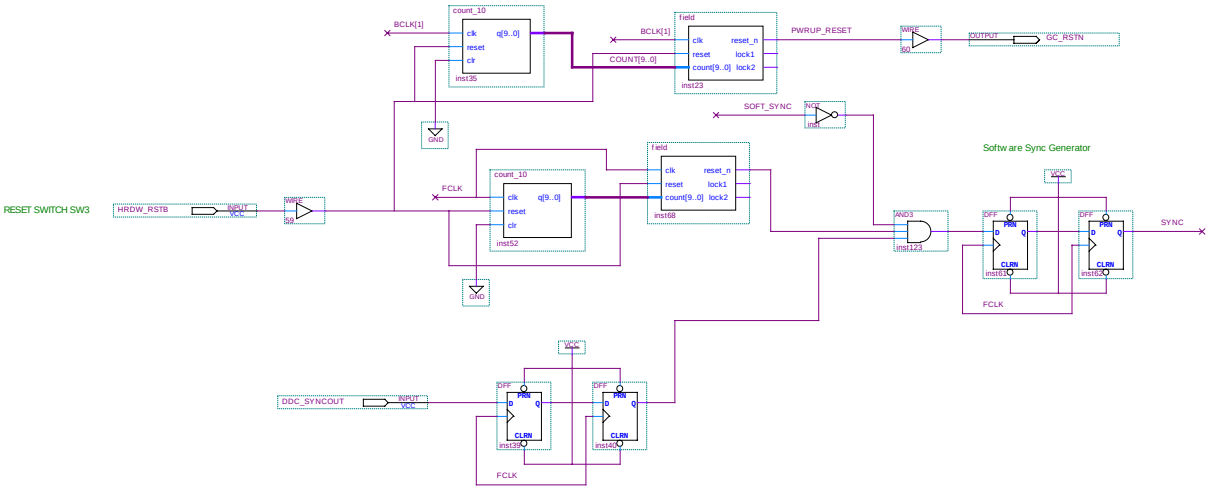


* There is a six register delay for the DUC Sync input to match the DDC Sync input when the Sync Delay value from the host PC is set to "1". This accommodates the for the delay created by the down counter and state machine.

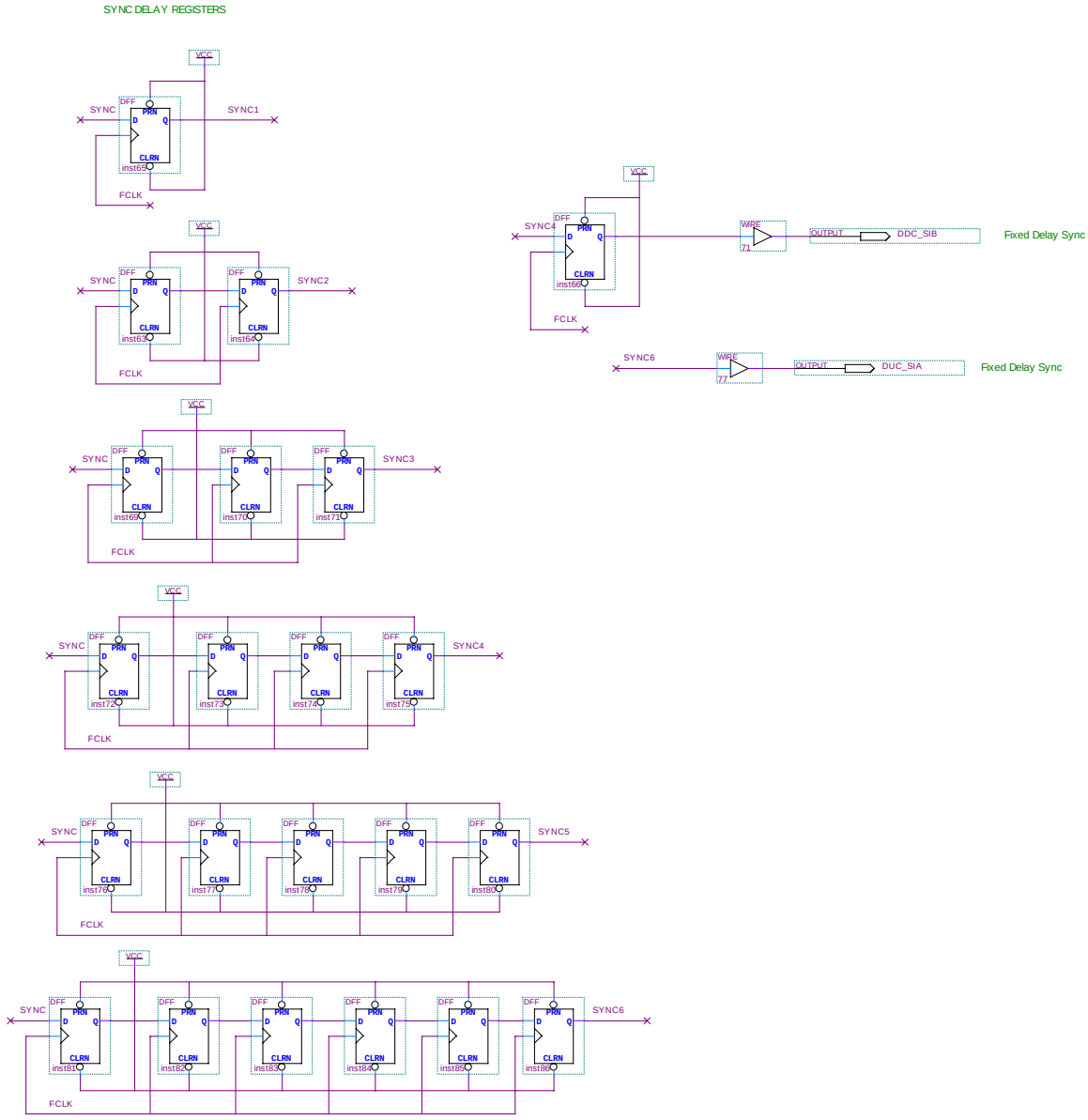
TSW4100 SYNC Block Diagram

FPGA Firmware (Generated by Altera Quartus version 6.1)

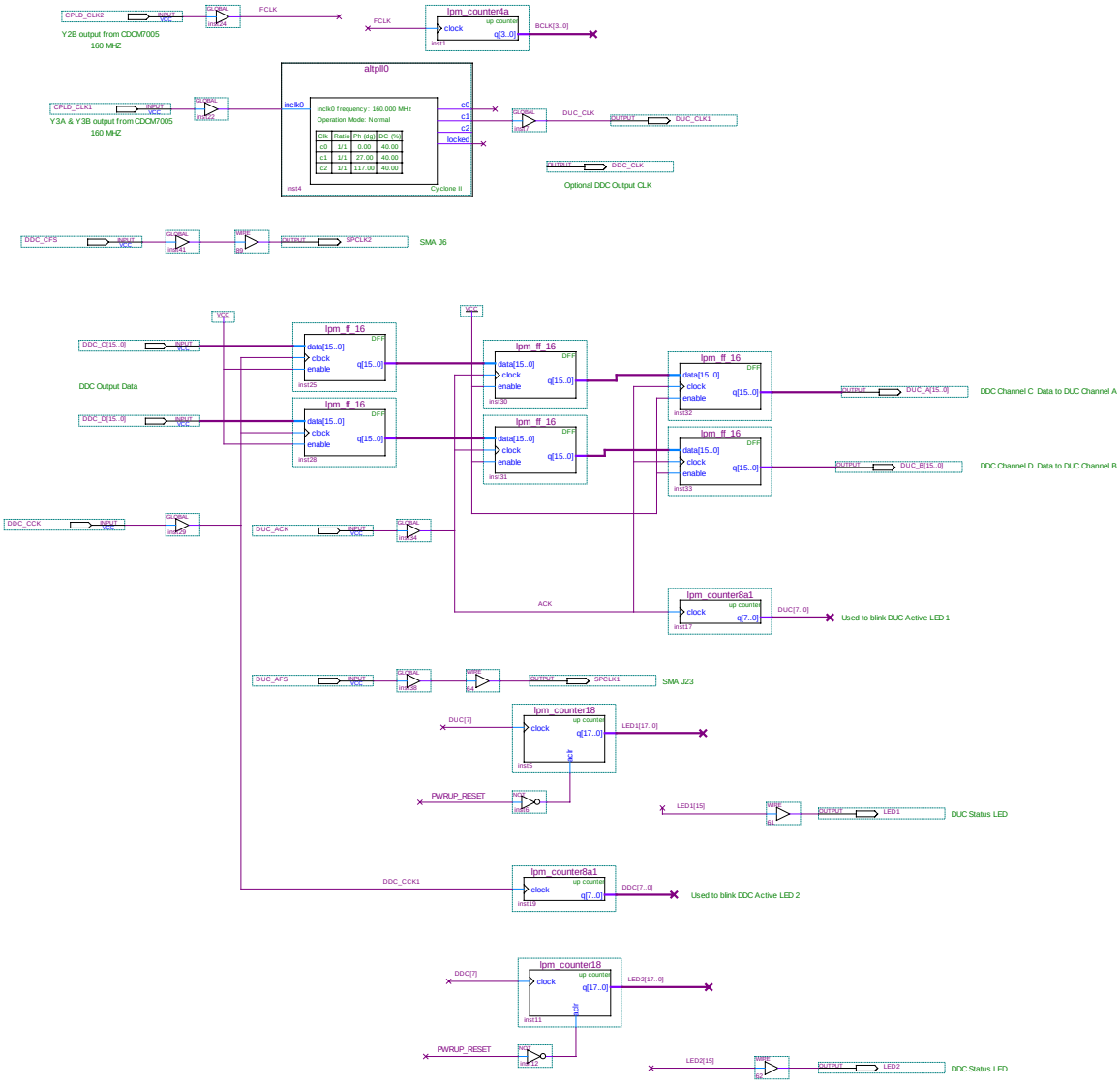
Power Up Reset
&
Software Sync Generator

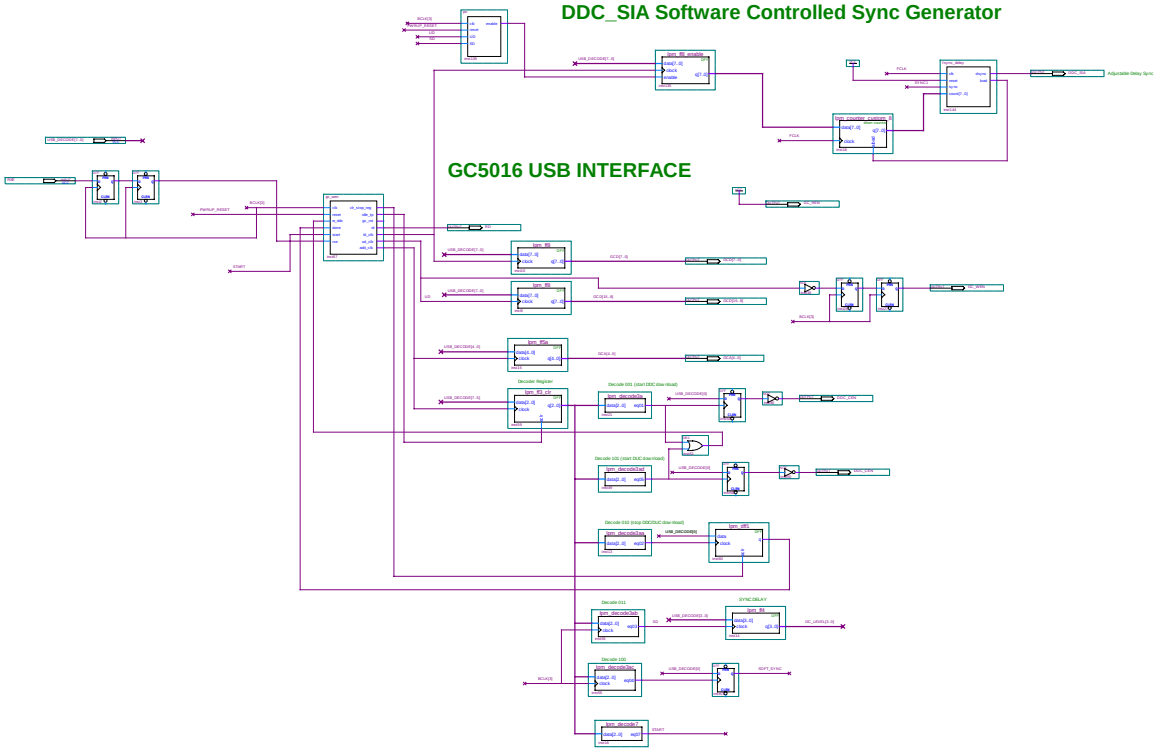


DDC_SIB & DUC_SIA Sync Outputs



DDC Output Data and DUC Input Data




DDC_SIA Software Controlled Sync Generator
GC5016 USB INTERFACE