CDCLVP1204

2:4 LVPECL buffer

100 MHz

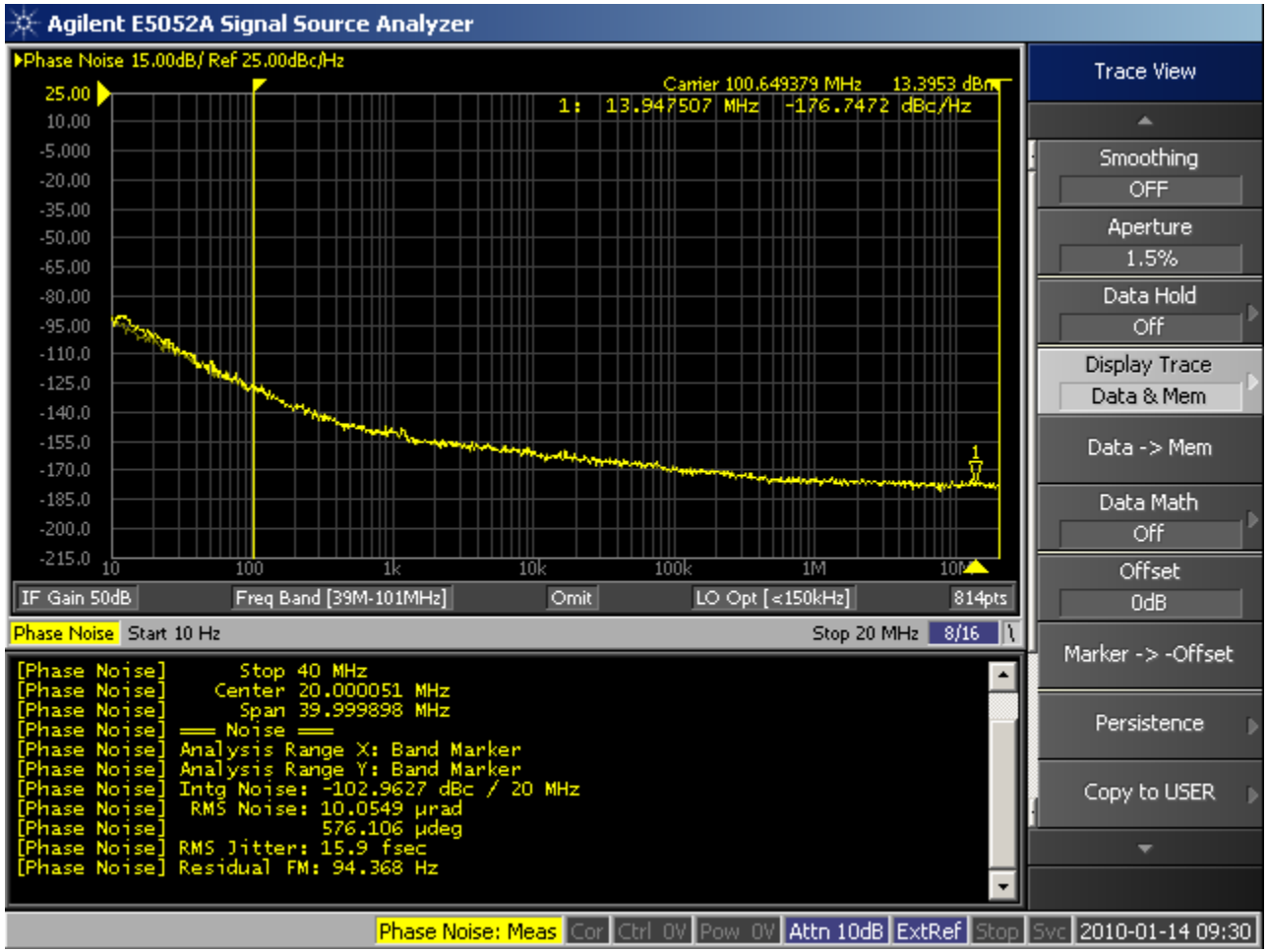
LVPECL Additive RMS Jitter

Test Conditions

- Results for:
  - CDCLVP1204
  - Room temperature
  - Nominal Supply 3.3V

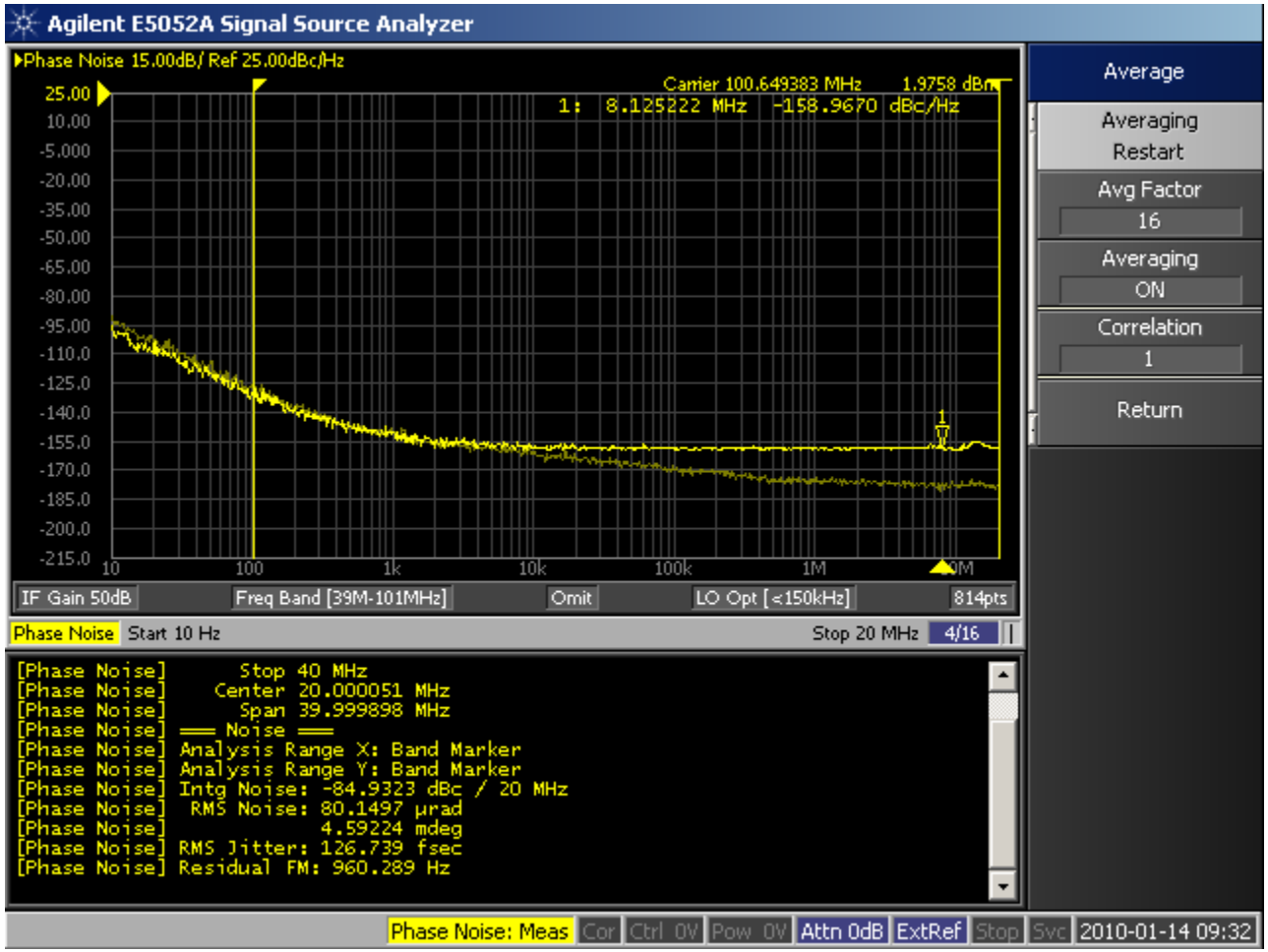
- Input/Output Clock frequency:
  - 100 MHz

Input Frequency (From Wenzel Osc.) = 100MHz



Input Jitter @ 100MHz (100 Hz – 40 MHz) = 15.9 fs RMS

Output Frequency = 100 MHz



Output Jitter @ 100 MHz (100 Hz – 40 MHz) = 126.739 fs RMS

Additive Jitter Calculation: 100 MHz

Input Jitter @ 100 MHz (100 Hz – 40 MHz) = 15.9 fs RMS

Output Jitter @ 100 MHz (100 Hz – 40 MHz) = 126.739 fs RMS

$$Additive\_Jitter = \sqrt{(rms\_jitter\_out)^2 - (rms\_jitter\_in)^2}$$

$$Additive\_Jitter = \sqrt{(126.739)^2 - (15.9)^2}$$

$$Additive\_Jitter = 125.737\ f\sec RMS(100Hz - 40Mhz)$$