Jitter Specifications - PCI Express REFCLK

Standard	Description	Measurement Setup	Symbol	Limit	Units
Common REFCLK Architecture					
PCIe1.1	Random Jitter		Rj	4.7	ps pk-pk
	Deterministic Jitter		Dj	41.9	ps pk-pk
	Total Jitter	Tj = Dj + 14.069 Rj (BER 10^{-12})	Tj	108	ps pk-pk
PCIe2.1	High Frequency RMS Jitter (1.5 MHz to $f_{REFCLK}/2$)		J_{RMS-HF}	3.1	ps RMS
	Low Frequency RMS Jitter (10 kHz to 1.5 MHz)		J_{RMS-LF}	3	ps RMS
	Total Jitter (1.5 MHz to $f_{REFCLK/2}$) (BER 10^{-12})	Specified in CEM2.0	Tj	43.6	ps pk-pk
PCIe3.0	Random Jitter		J_{RMS}	1	ps RMS
Data Clocked REFCLK Architecture					
PCIe 1.1	Not Defined in PCIe 1.1				
PCIe 2.1	High Frequency RMS Jitter (1.5 MHz to $f_{REFCLK}/2$)		J_{RMS-HF}	4	ps RMS
	Low Frequency RMS Jitter (10 kHz to 1.5 MHz)		J_{RMS-LF}	7.5	ps pk-pk
PCIe 3.0	Random Jitter		J_{RMS}	1	ps RMS

Spread Spectrum Clocking

Modulation Rate: 30 kHz - 33 kHz

Spread Factor: -0.5%, 0%