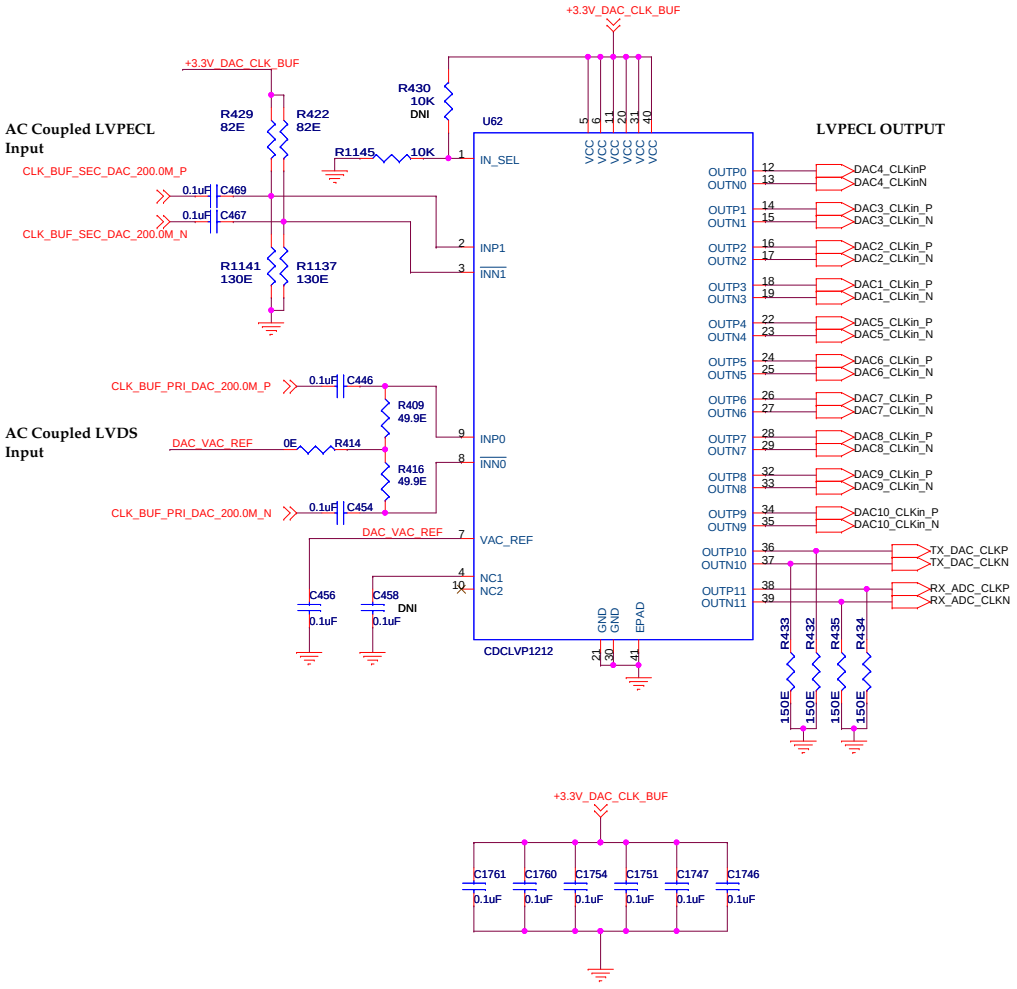
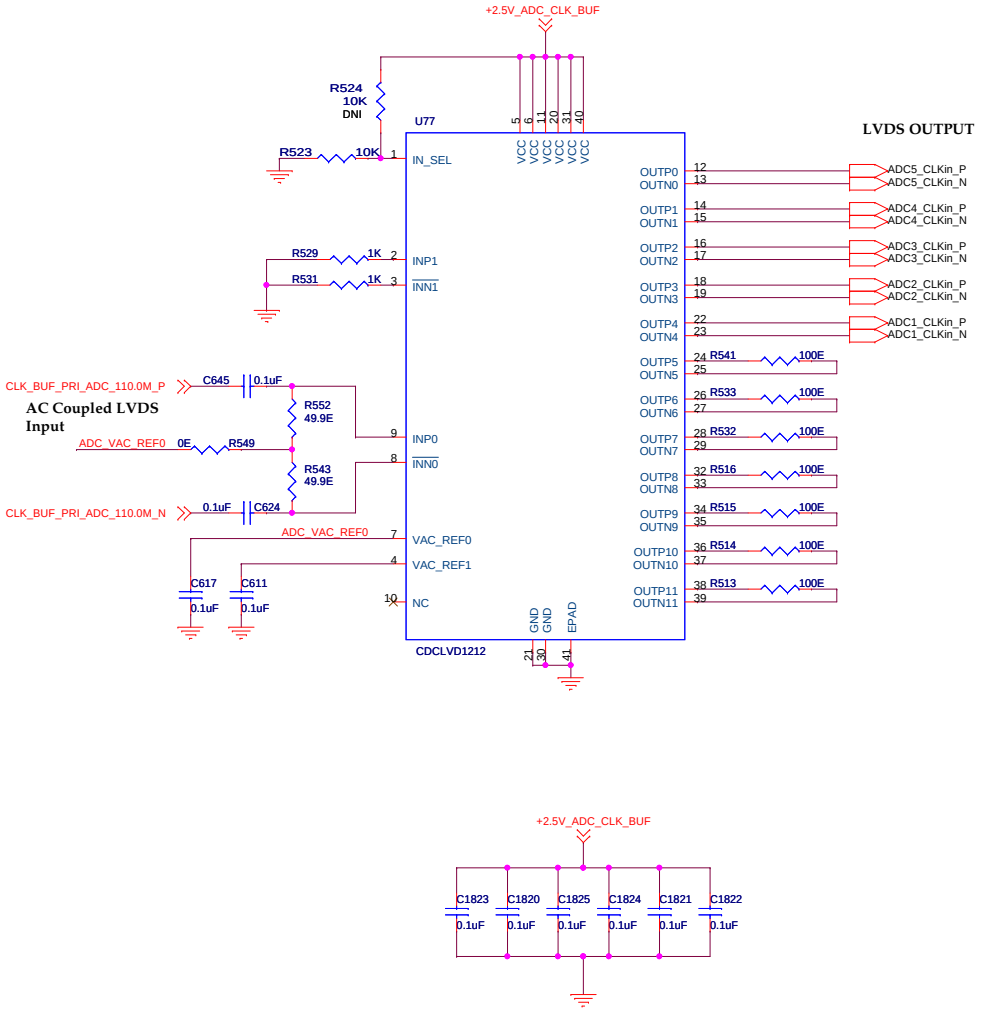
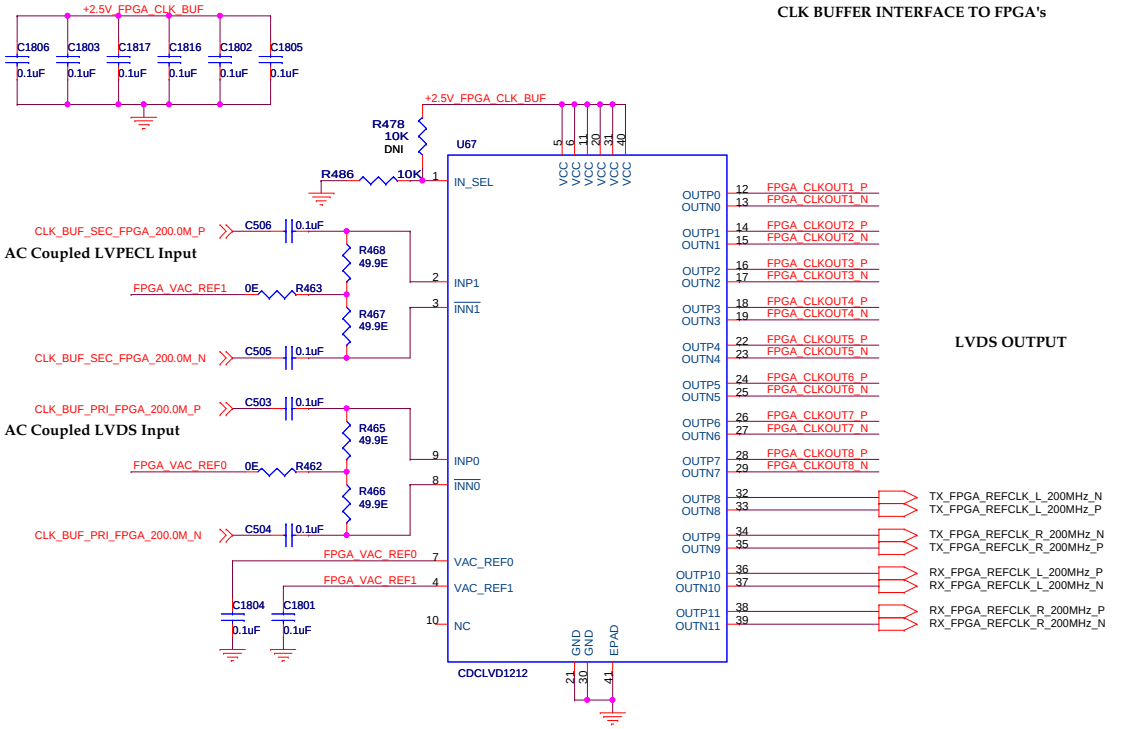
CLK BUFFER INTERFACE TO DAC



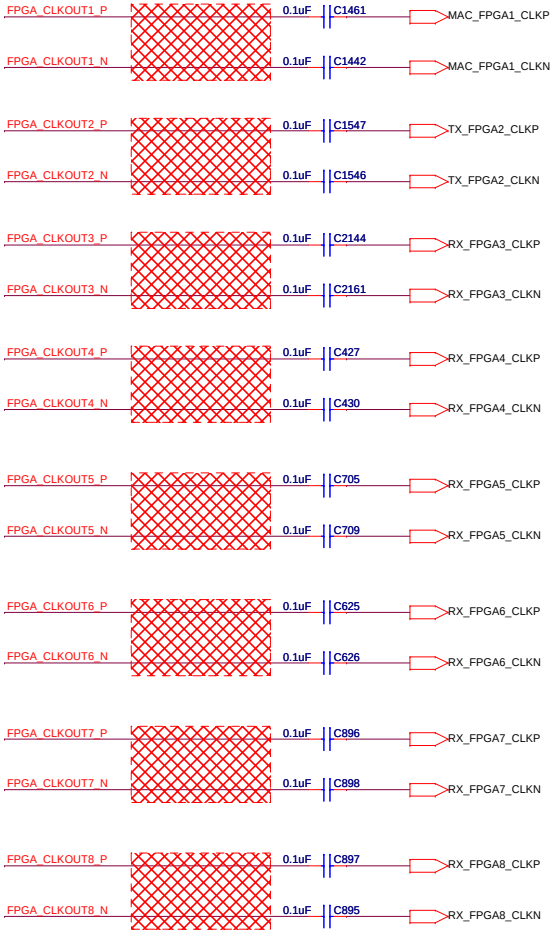
CLK BUFFER INTERFACE TO ADC



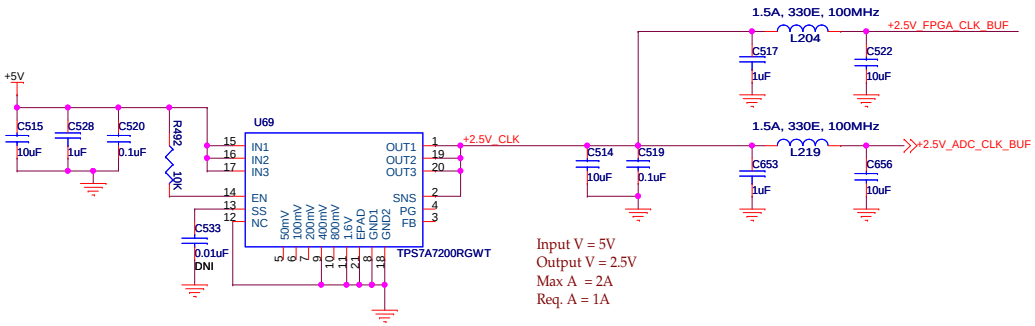
CLK BUFFER INTERFACE TO FPGA's



LVDS OUTPUT



LVDS Interface. Use FPGA Interncal 100E resisitor for parallel termination
100E Differential coupled Transmission Lines



Input V = 5V
Output V = 2.5V
Max A = 2A
Req. A = 1A

CLK_JITTER CLEANER INTERFACE