ADC Input						
Full-Scale Input Voltage	(V_{IN} = ADCINP – ADCINN)			±1.0$\overline{6}$$V_{REF}$		V

Voltage Reference Input						
Reference Input Voltage	(V_{REF} = VREFP – VREFN)		0.5	4.096	AVDD – AVSS	V
Negative Reference Input (VREFN)			AVSS – 0.1V		VREFP – 0.5	V
Positive Reference Input (VREFP)			VREFN + 0.5		AVDD + 0.1V	V

Output Data Scaling and Over-Range

The ADS1258 is scaled such that the output data code resulting from an input voltage equal to ±V_{REF} has a margin of 6.$\overline{6}$% before clipping. This architecture allows operation of applied input signals at or near full-scale without overloading the converter.

Specifically, the device is calibrated so that:

1LSB = V_{REF}/780000h,

and the output clips when:

$|V_{IN}| \geq 1.0\overline{6} \times V_{REF}$.

Table 8 summarizes the ideal output codes versus input signals.

Table 8. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} (ADCINP – ADCINN)	IDEAL OUTPUT CODE(1)	DESCRIPTION
≥ +1.0$\overline{6}$ V_{REF}	7FFFFFh	Maximum Positive Full-Scale Before Output Clipping
+V_{REF}	780000h	V_{IN} = +V_{REF}
+1.0$\overline{6}$ V_{REF}/(2^{23} – 1)	000001h	+1LSB
0	000000h	Bipolar Zero
–1.0$\overline{6}$ V_{REF}/(2^{23} – 1)	FFFFFFh	–1LSB
–V_{REF}	87FFFFh	V_{IN} = –V_{REF}
≤ –1.0$\overline{6}$ V_{REF} × (2^{23}/2^{23} – 1)	800000h	Maximum Negative Full-Scale Before Output Clipping

(1) Excludes effects of noise, linearity, offset, and gain errors.