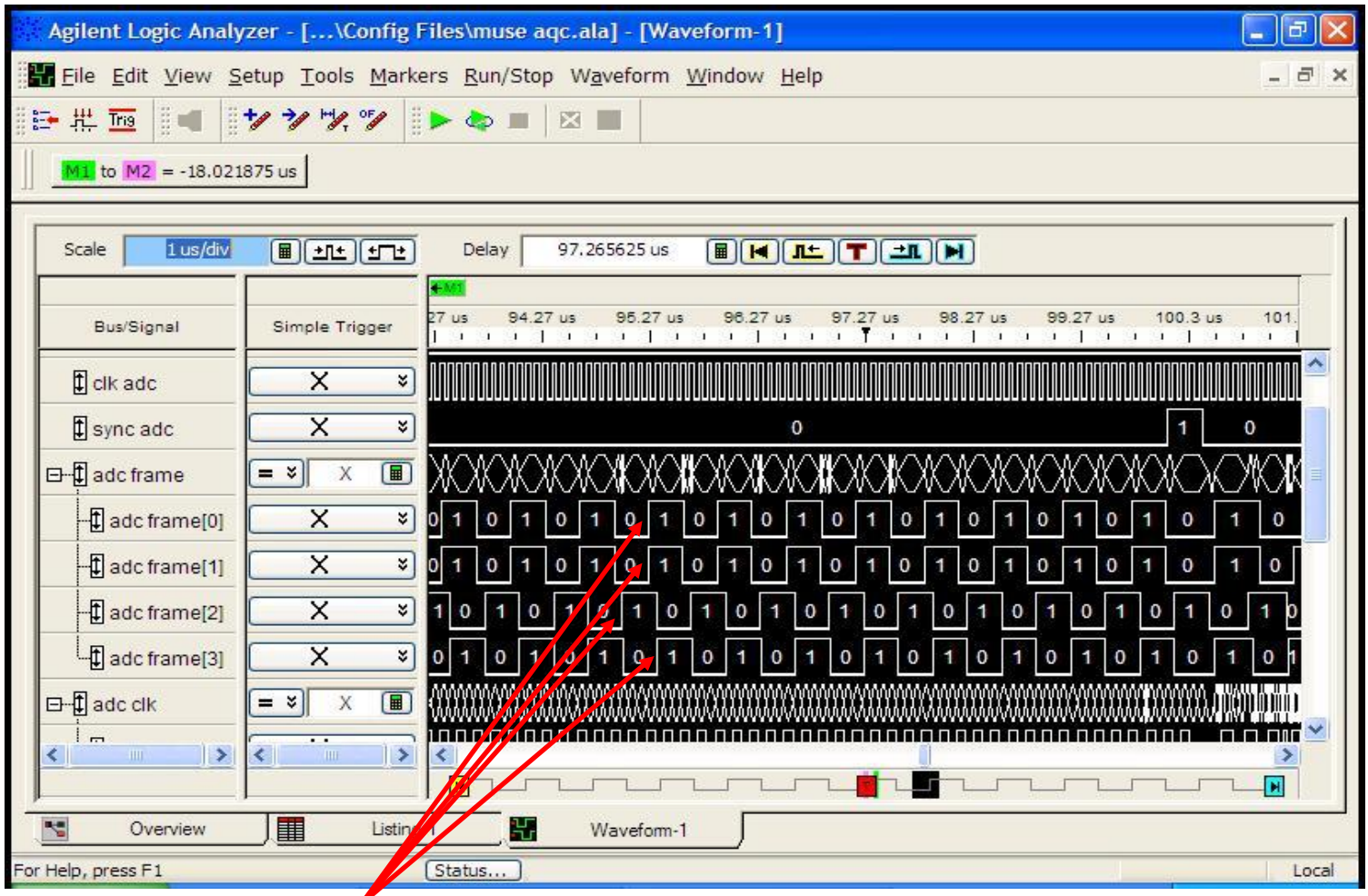
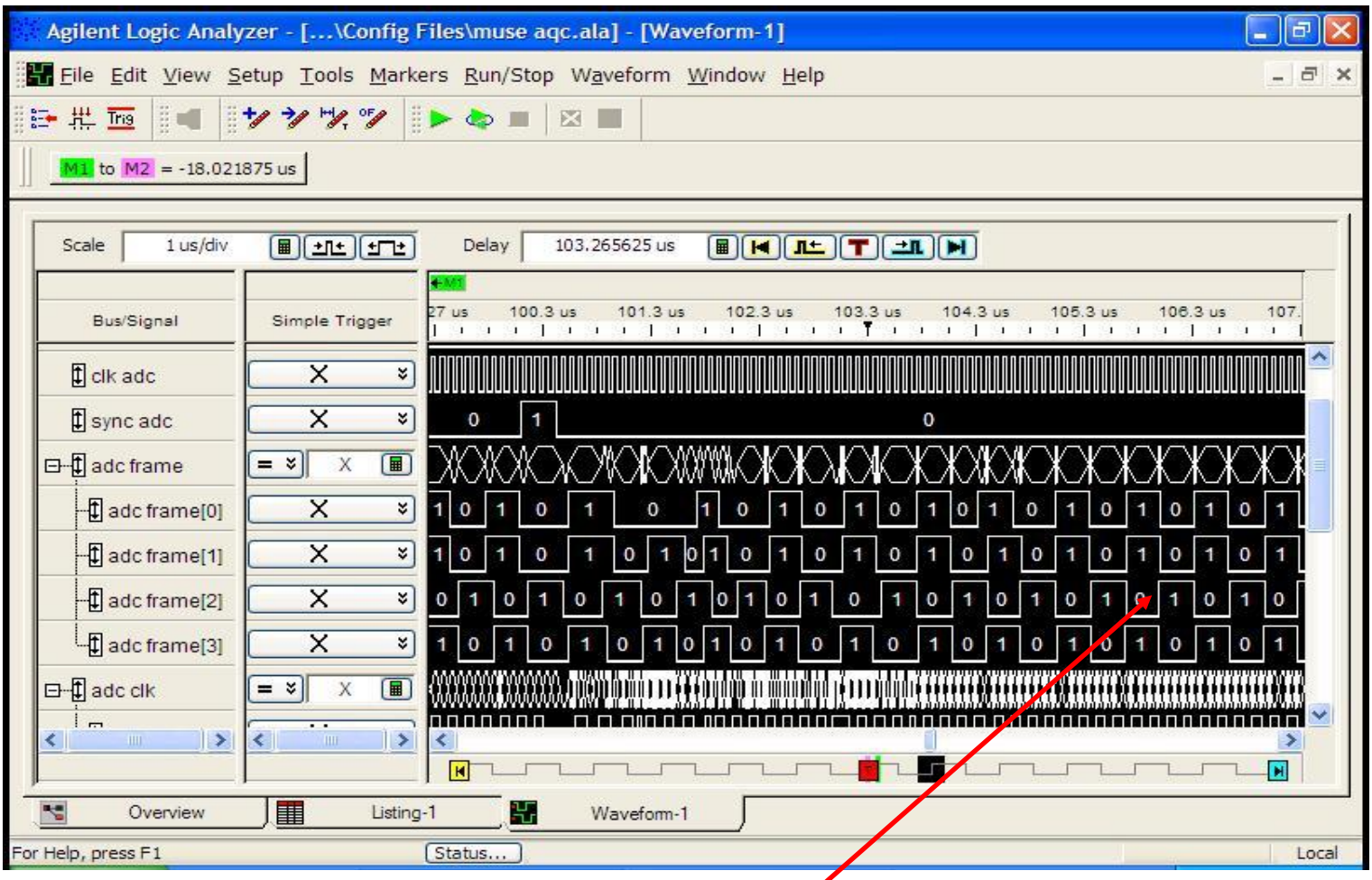
Before first SYNC signal



Random phase on ADCLK

After first SYNC signal



Opposit phase on ADCLK