

# *TVP5158*

*Four-Channel PAL/NTSC Video Decoder*

*With Independent Scalers, Noise Reduction,*

*Pixel-Interleaved and Line-Interleaved Multiplexed Output,*

*Cascade Connection, and Audio ADCs Integrated*

*For Security Applications*

## *Data Manual*

*REV 0.03*

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Literature Number SLES243  
December 2008

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**Revision History**

REV	DATE	DESCRIPTION	By
0.01	04/29/08	Initial version	ChengNing Wang
0.02	08/12/08	Update Pin-out	ChengNing Wang
0.03	12/19/08	Add Functional Description Info	ChengNing Wang

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# 1. Introduction

The TVP5158 device is a 4-channel, high-quality NTSC/PAL video decoder that digitizes and decodes all popular base-band analog video formats into digital video output. Each channel of this decoder includes 10-bit 27-MSPS A/D converter (ADC). Preceding each ADC in the device, the corresponding analog channel contains an analog circuit that clamps the input to a reference voltage and applies the gain.

Composite input signal is sampled at 2 X the ITU-R BT.601 clock frequency, line-locked alignment, and is then decimated to the 1X pixel rate. CVBS decoding uses five-line adaptive comb filtering for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts. A chroma trap filter is also available. On CVBS inputs, the user can control video characteristics such as contrast, brightness, saturation, and hue via an I2C host port interface. Furthermore, luma peaking (sharpness) with programmable gain is included.

All 4 channels of the TVP5158 are independently controllable. The decoders share single clock input for all channels and for all supported standards.

TVP5158 has Glue-less video and audio output interface to TI DaVinci™ video processors. TVP5158 video output ports support 8-bit ITU-R BT.656 and 16-bit 4:2:2 YUV with embedded synchronization. TVP5158 also supports multiplexed video output by pixel-interleaved and line-interleaved modes with metadata insertion. TVP5158 integrates 4-Ch audio ADC to reduce the BOM cost for surveillance market. The multiple TVP5158 devices can be cascade connected to support up to 8-Ch Video or 16-Ch Audio processing.

Noise reduction and auto contrast functions improve the video quality under low light condition which is very critical for surveillance products.

The TVP5158 can be programmed by using a single I<sup>2</sup>C serial interface. I2C commands can be sent to one or more decoder cores simultaneously, reducing the amount of I2C activity necessary to configure each core. This is especially useful for fast downloading modified firmware to the decoder cores.

TVP5158 uses 1.1 V, 1.8 V, and 3.3 V power supplies for the analog/digital core and the I/O. Available in a 128-pin TQFP package.

## 1.1 Features

- Four Separate Video Decoder channels having the following features for each channel.
  - Accepts NTSC (J, M, 4.43) and PAL (B, D, G, H, I, M, N, Nc, 60) video data
  - Composite video inputs, Pseudo-differential video inputs to improved noise immunity
  - Input voltage range 1.4 Vpp, no external attenuator required
  - High-speed 10-bit ADC
  - Fully differential CMOS analog preprocessing channels with clamping
  - Integrated Anti-Aliasing filter
  - 2D 5-line (5H) adaptive comb filter
  - Noise reduction and auto contrast
  - Robust automatic video standard detection (NTSC/PAL) and switching
  - Programmable hue, saturation, sharpness, brightness and contrast
  - Luma-peaking processing
  - Patented architecture for locking to weak, noisy, or unstable signals
- Four independent scalers support horizontal and/or vertical 2:1 downscaling
- Extensive channel multiplexing capabilities with metadata insertion
  - Supports pixel-interleaved and line-interleaved modes
  - Four-channel D1 multiplexed output at 8 bit at 108 MHz
  - Video Cascade Connection for 8-Ch CIF, 8-Ch Half-D1, and 8-Ch CIF + 1-Ch D1 outputs
  - Supports concurrent NTSC and PAL inputs
- Integrated four-channel audio ADC with audio sample rate of 8 kHz or 16 kHz
- Support I2S output at Master and Slave mode
- Support audio cascade connection
- Support crystal interface with on-chip oscillator and single clock input mode
- Single 27-MHz clock input or crystal for all standards and all channels
- Internal phase-locked loop (PLL) for line-locked clock (separate for each channel) and sampling
- Standard programmable video output format:
  - ITU-R BT.656, 8-bit 4:2:2 with embedded syncs
  - YUV 16-bit 4:2:2 with embedded syncs
- Macrovision copy protection detection
- 3.3-V Compatible I/O
- Typical consumption: 750 mW
- 128-pin TQFP package

## 1.2 Applications

The following is a partial list of suggested applications:

- Security/surveillance digital video recorders/servers and PCI products
- Automotive infotainment video hub
- Large format video wall displays
- Game Systems

## 1.3 Related Products

*TVP5154A*

*TVP5150AM1*

*TVP5146M2*

*TVP5147M1*

## 1.4 Ordering Information

T <sub>A</sub>	PACKAGED DEVICES
	TQFP 128-Pin Package with PowerPAD
0°C to 70°C	TVP5158PNP
-40°C to 85°C	TVP5158IPNP

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## 1.5 Functional Block Diagram

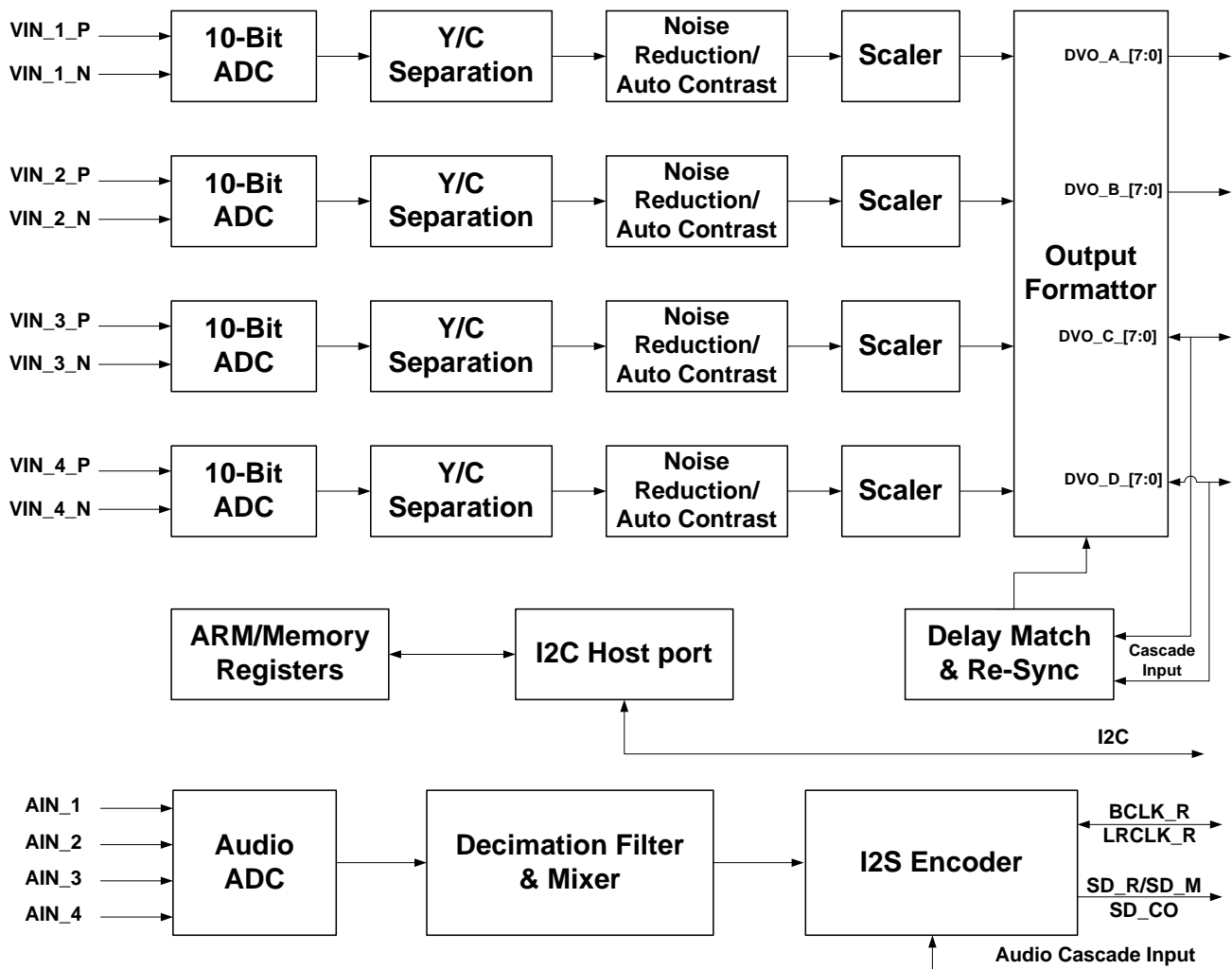


Figure 1-1. Functional Block Diagram



## 2. Terminal Assignments

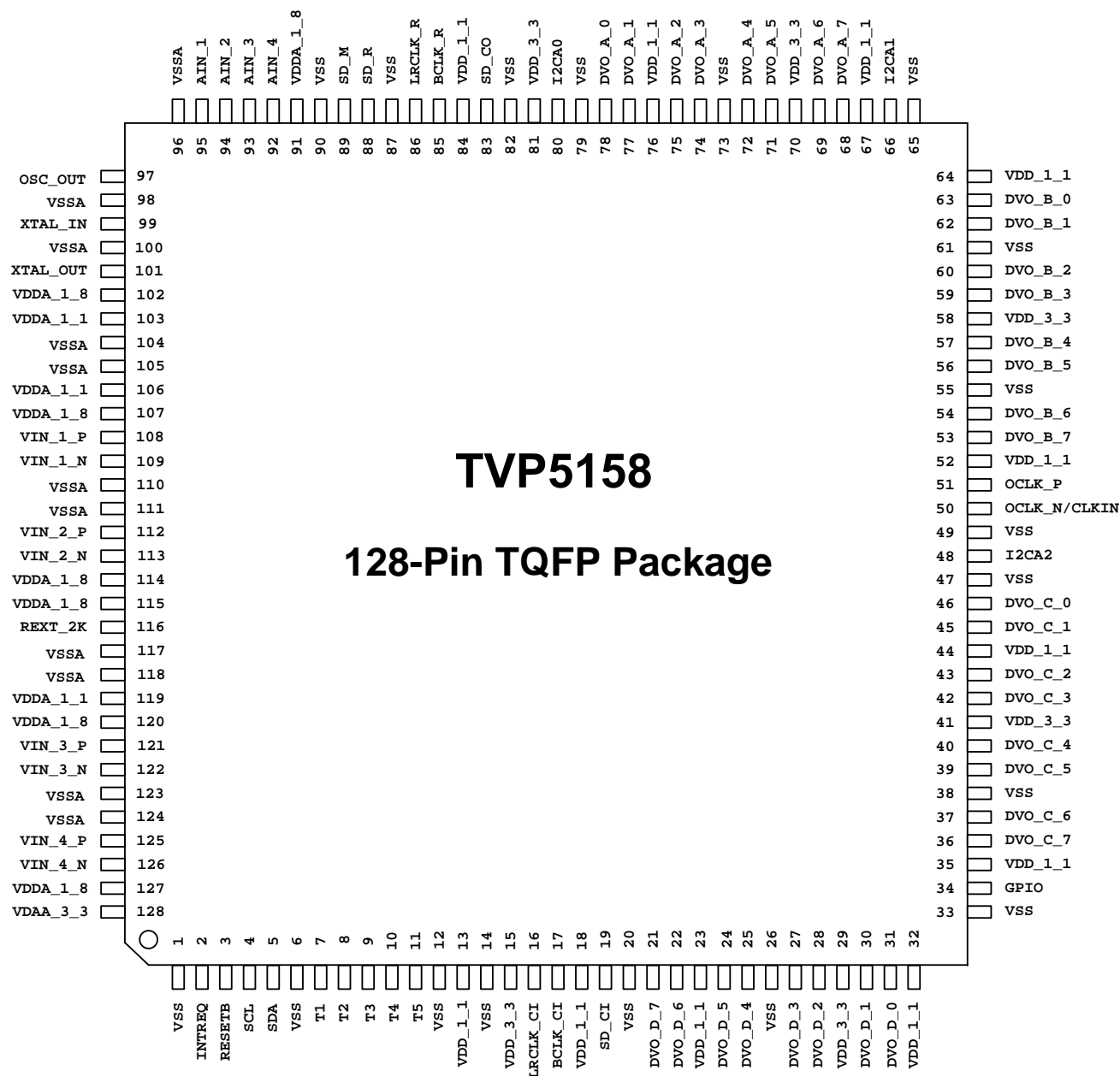


Figure 2-1. Terminal Assignment

## 2.1 Terminal Functions

**Table 2-1. Terminal Functions**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Analog Section			
VIN_1_P	108	I	Analog video input for ADC channel 1.
VIN_1_N	109	I	Common-mode reference input for ADC channel 1.
VIN_2_P	112	I	Analog video input for ADC channel 2.
VIN_2_N	113	I	Common-mode reference input for ADC channel 2.
VIN_3_P	121	I	Analog video input for ADC channel 3.
VIN_3_N	122	I	Common-mode reference input for ADC channel 3.
VIN_4_P	125	I	Analog video input for ADC channel 4.
VIN_4_N	126	I	Common-mode reference input for ADC channels.
REXT_2K	116	I	External resistor for AFE bias generator. Connect external 1.8kΩ resistor to ground.
AIN_1	95	I	Analog audio input for channel 1
AIN_2	94	I	Analog audio input for channel 2
AIN_3	93	I	Analog audio input for channel 3
AIN_4	92	I	Analog audio input for channel 4
Analog Power			
VDDA_1_1	103,106, 119	P	1.1V analog supply
VDDA_1_8	91,102,107, 114,115, 120,127	P	1.8V analog supply
VDDA_3_3	128	P	3.3V analog supply for all 4 video channels
VSSA	96,98,100, 104, 105, 110, 111, 117, 118, 123, 124	G	Analog ground.
Digital Power			
VSS	1,6,12,14,20,26, 33,38,47,49,55, 61,65,73,79,82, 87,90	G	Digital ground
VDD_1_1	13,18,23,32,35, 44,52,64,67,76, 84	P	Digital core supply. Connect to 1.1V digital supply.
VDD_3_3	15,29,41,58,70, 81	P	Digital I/O supply. Connect to 3.3V digital supply.
Digital Section			
INTREQ	2	O	Interrupt request. Interrupt signal to host processor.
RESETB	3	I	Reset. An active low signal that controls the reset state.
SCL	4	I/O	I <sup>2</sup> C serial clock (open drain)
SDA	5	I/O	I <sup>2</sup> C serial data (open drain)
XTAL_IN	99	I	External clock reference input. It may be connected to external oscillator with 1.8-V compatible clock signal or 27.0-MHz crystal oscillator.
XTAL_OUT	101	O	External clock reference output. Not connected if XTAL_IN is driven by an external single-ended oscillator.
OSC_OUT	97	O	Buffered crystal oscillator output. 1.8-V compatible.
OCLK_P	51	O	Output data clock+. All 4 digital video output ports are synchronized to this clock.
OCLK_N/CLKIN	50	I/O	Output data clock- for 2-Ch time-multiplexed mode or data clock input for 8-Ch video cascade mode
DVO_A_[7:0]	68,69,71,72,74, 75,77,78	O	Digital video output data bus.

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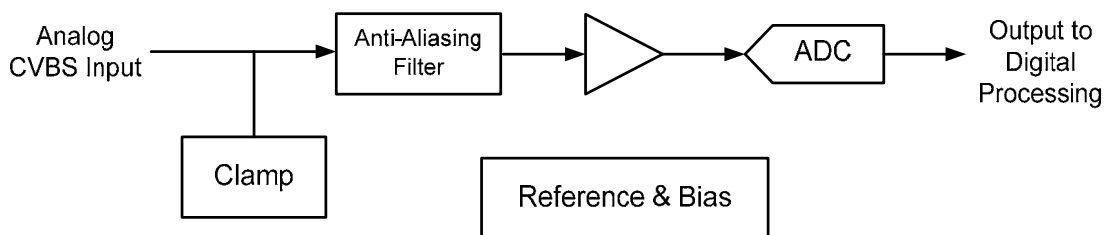
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TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DVO_B_[7:0]	53,54,56,57,59,60,62,63	O	Digital video output data bus.
DVO_C_[7:0]	36,37,39,40,42,43,45,46	I/O	Digital video output data bus. In cascade mode, all pins operate as input from another TVP5158 device.
DVO_D_[7:0]	21,22,24,25,27,28,30,31	I/O	Digital video output data bus. In cascade mode, all pins operate as input from another TVP5158 device.
I2CA0	80	I	I2C slave address bit 0.
I2CA1	66	I	I2C slave address bit 1.
I2CA2	48	I	I2C slave address bit 2.
GPIO	34	I/O	GPIO port.
<b>Digital Audio Section</b>			
BCLK_R	85	I/O	I2S bit clock for recording. Also known as I2S serial clock (SCK). Supports master and slave modes.
LRCLK_R	86	I/O	I2S left/right clock for recording. Also known as I2S word select (WS). Supports master and slave modes.
SD_R	88	O	I2S serial data output for recording.
SD_M	89	O	I2S serial data output for mixed audio or recording.
SD_CO	83	O	Audio serial data output for cascade mode
LRCLK_CI	16	I	I2S left/right clock input for cascade mode. Also known as I2S word select (WS).
BCLK_CI	17	I	I2S bit clock input for cascade mode. Also known as I2S serial clock (SCK).
SD_CI	19	I	Audio serial data input for cascade mode.
<b>No Connect Pins</b>			
T1, T2, T3, T4, T5	7,8,9,10,11	NC	For normal operation, no connect.

## 3. Functional Description

### 3.1 Video Analog Processing and A/D Converters

Each channel of the TVP5158 decoder accepts one composite video input and performs video clamping, anti-aliasing filter, video amplification, A/D conversion, and gain and offset adjustments to center the digitized video signal. Figure 3-1 shows the block diagram of TVP5158 video analog processing and ADC.



**Figure 3-1. The Block Diagram of Video Analog Processing and ADC**

#### 3.1.1 Analog Video Input

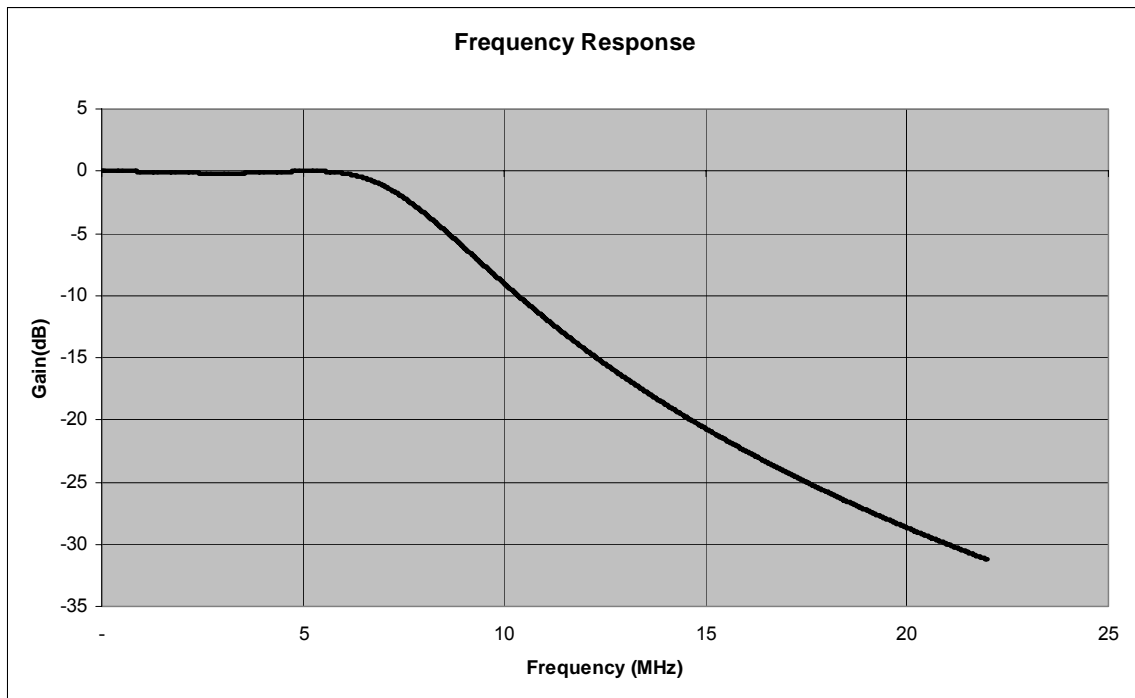
TVP5158 accepts NTSC (J, M, 4.43) and PAL (B, D, G, H, I, M, N, Nc, 60) video standard. Each video decoder channel supports composite video input with pseudo-differential pin which improves the noise immunity and analog performance.

The decoder supports a maximum input voltage range of 1.4 V<sub>pp</sub>, which should be ac-coupled through 0.1-μF capacitor. The nominal parallel termination resistor before the input to the device is 75 Ω.

TVP5158 also integrates anti-aliasing filter to provide good stop-band rejection on analog video input signal. Figure 3-2 shows the frequency response of TVP5158 anti-aliasing filter.

#### 3.1.2 Analog Input Clamping

An internal clamping circuit restores the ac-coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video sync level to a fixed dc reference voltage.



**Figure 3-2. The Frequency Response of Anti-Aliasing Filter**

### 3.1.3 A/D Converter

All ADCs have a resolution of 10 bits and can operate at 27 MSPS. Each A/D channel receives a clock from the on-chip phase-locked loop (PLL) at a frequency 27 MHz. All ADC reference voltages are generated internally.

## 3.2 Digital Video Processing

Digital Video Processing block receives digitized video signals from the ADCs and performs composite processing and YCbCr signal enhancements. The digital data output can be programmed to two formats: ITU-R BT.656 8-bit 4:2:2 with embedded syncs or 16-bit 4:2:2 with embedded syncs. The circuit also detects pseudo-sync pulses, AGC pulses, and color striping in Macrovision-encoded copy-protected material.

### 3.2.1 2x Decimation Filter

All input signals are typically over-sampled by a factor of 2 (By 27 MHz Clock). The A/D outputs initially pass through decimation filters that reduce the data rate to 1x the pixel rate. The decimation filter is a half-band filter. Over-sampling and decimation filtering can effectively increase the overall signal-to-noise ratio by 3 dB.

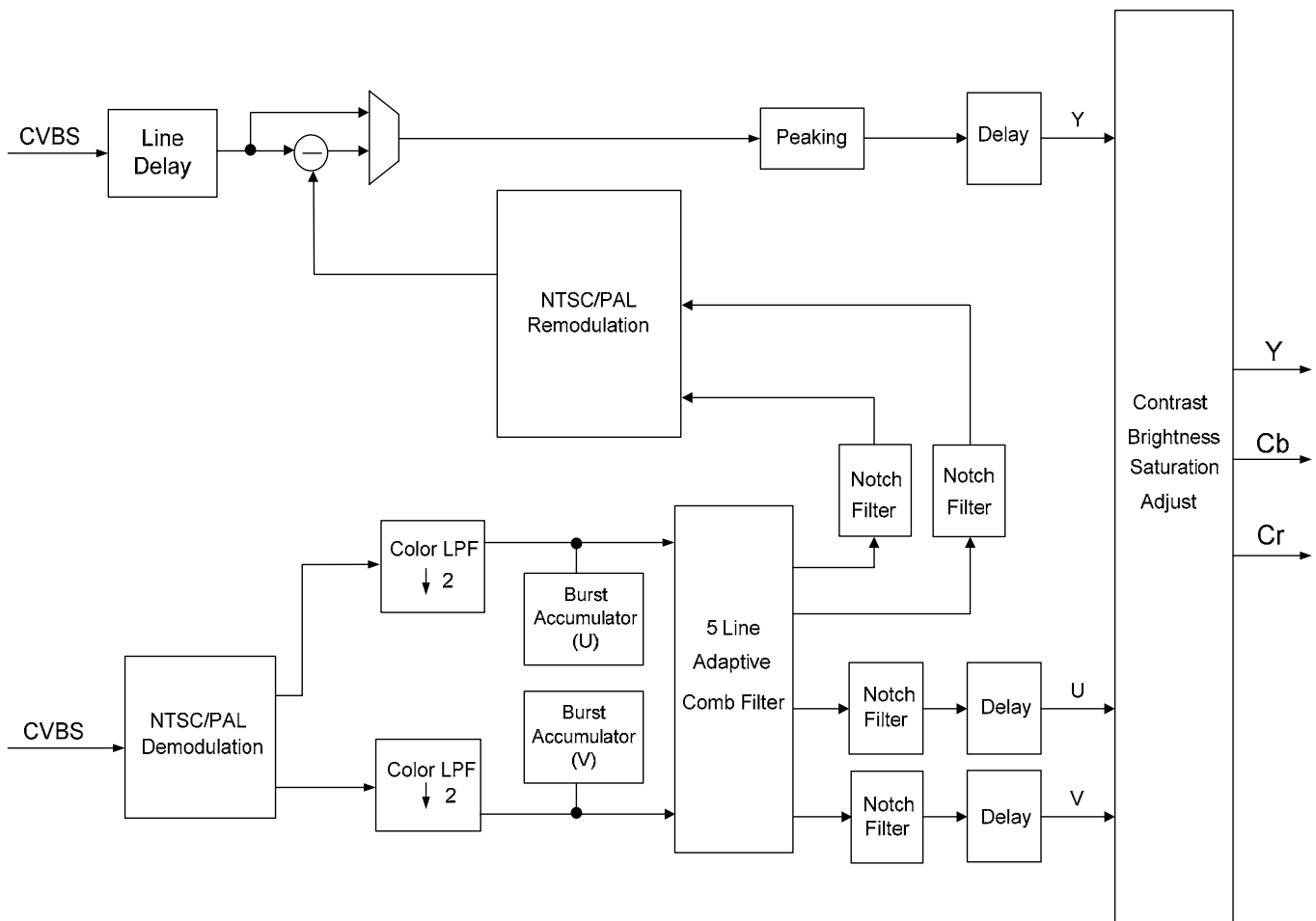
### 3.2.2 Automatic Gain Control

The automatic gain control (AGC) can be enabled and can adjust the signal amplitude controlled by 14-bit digital gain stage after the ADC. The AGC algorithms can use up to four amplitude references: sync height, color burst amplitude, composite peak, and luma peak.

The specific amplitude references being used by the AGC algorithms can be controlled using the AGC white peak processing register located at sub-address 2Dh. The gain increment speed and gain increment delay can be controlled using the AGC increment speed register located at sub-address 29h and the AGC increment delay register located at sub-address 2Ah. The gain decrement speed and gain decrement delay can be controlled using the AGC decrement speed register located at sub-address 2Bh and the AGC decrement delay register located at sub-address 2Ch.

### 3.2.3 Composite Processor

This Composite Processor circuit receives a digitized composite signal from the ADCs and performs Y/C separation, chroma demodulation for PAL/NTSC, and YUV signal enhancements. The 10-bit composite video is multiplied by the sub carrier signals in the quadrature demodulator to generate color difference signals U and V. The U and V signals are then sent to low-pass filters to achieve the desired bandwidth. An adaptive 5-line comb filter separates UV from Y based on the unique property of color phase shifts from line to line. The chroma is re-modulated through a quadrature modulator and subtracted from line-delayed composite video to generate luma. This form of Y/C separation is completely complementary, thus there is no loss of information. However, in some applications, it is desirable to limit the U/V bandwidth to avoid crosstalk. In that case, notch filters can be turned on. To accommodate some viewing preferences, a peaking filter is also available in the luma path. Contrast, brightness, sharpness, hue, and saturation controls are programmable through the I2C host port. Figure 3-3 shows the block diagram of Composite Processor.

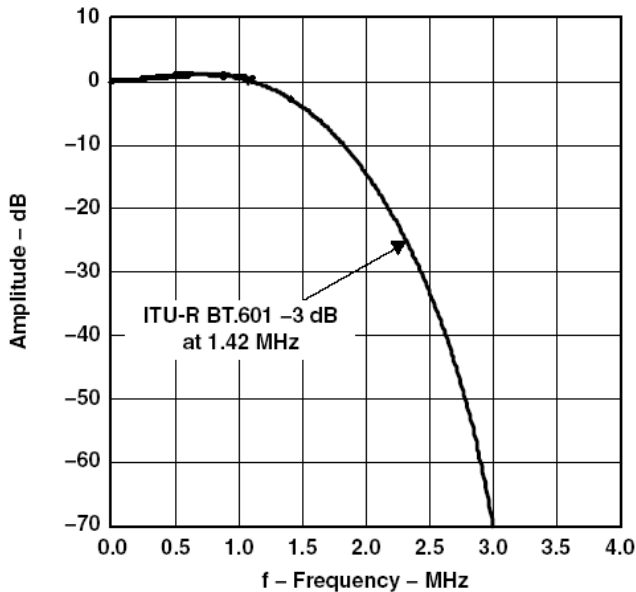


**Figure 3-3. The Block Diagram of Composite Processor**

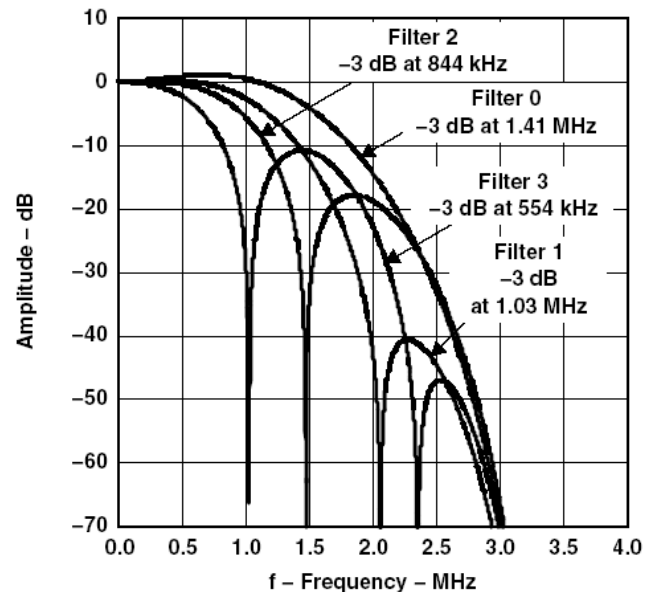
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### 3.2.3.1 Color Low-Pass Filter

High filter bandwidth preserves sharp color transitions and produces crisp color boundaries. However, for nonstandard video sources that have asymmetrical U and V side bands, it is desirable to limit the filter bandwidth to avoid UV crosstalk. The color low-pass filter bandwidth is programmable to enable one of the three notch filters. Figure 3-4 and Figure 3-5 represent the frequency responses of the wideband color low-pass filters.



**Figure 3-4. Color Low-Pass Filter Frequency Response**

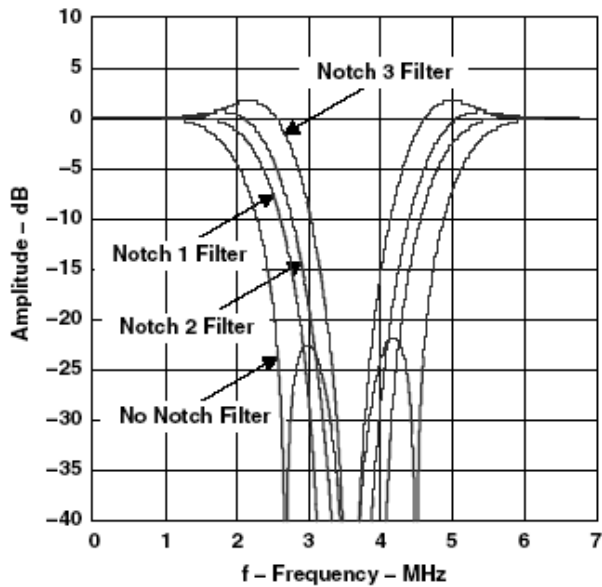


**Figure 3-5. Color Low-Pass Filter with Filter Characteristics, NTSC/PAL ITU-R BT.601 Sampling**

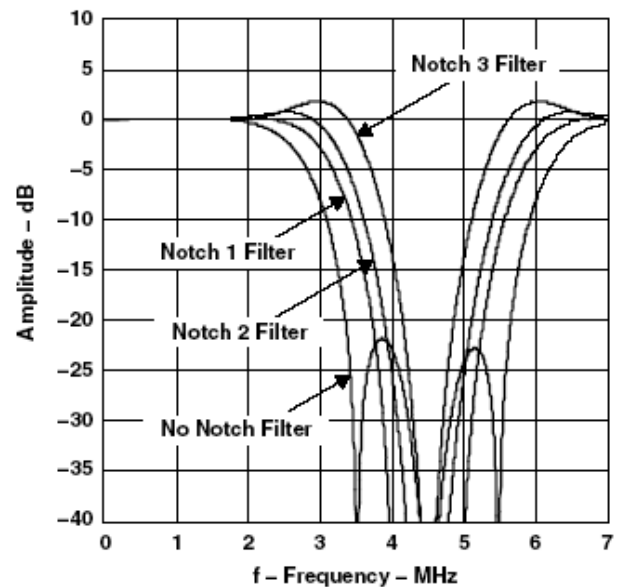
### 3.2.3.2 Y/C Separation

Y/C separation can be done using adaptive 5-line (5-H delay) comb filters or a chroma trap filter. The comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma trap filters are used which are shown in Figure 3-6 and Figure 3-7. The TI patented adaptive comb filter algorithm reduces artifacts such as hanging dots at color boundaries. It detects and properly handles false colors in high-frequency luminance images such as a multiburst pattern or circle pattern.





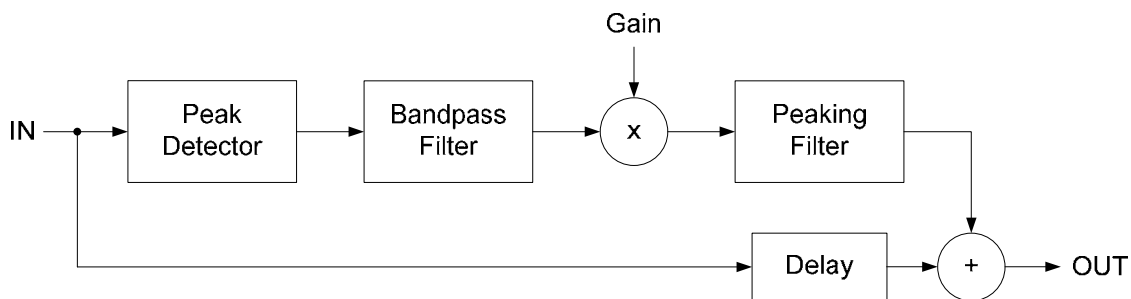
**Figure 3-6. Chroma Trap Filter Frequency Response, NTSC ITU-R BT.601 Sampling**



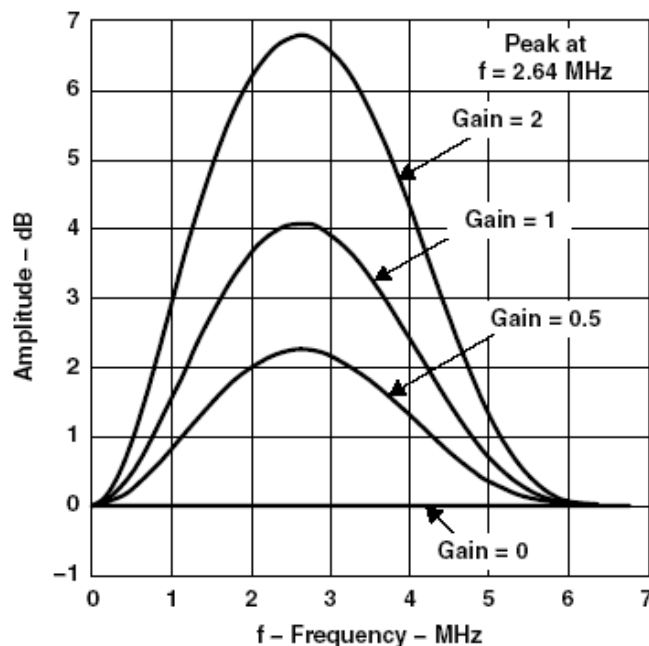
**Figure 3-7. Chroma Trap Filter Frequency Response, PAL ITU-R BT.601 Sampling**

### 3.2.4 Luminance Processing

The digitized composite video signal passes through either a luminance comb filter or a chroma trap filter, either of which removes chrominance information from the composite signal to generate a luminance signal. The luminance signal is then fed into the input of a peaking circuit. Figure 3-8 shows the basic functions of the luminance data path. A peaking filter (edge enhancer) amplifies high-frequency components of the luminance signal. Figure 3-9 shows the characteristics of the peaking filter at four different gain settings that are user-programmable via the I2C interface.



**Figure 3-8. Luminance Edge-Enhancer Peaking Block Diagram**



**Figure 3-9. Peaking Filter Response, NTSC/PAL ITU-R BT.601 Sampling**

### 3.3 AVID Cropping

AVID or active video cropping provides a means to decrease the amount of video data output. This is accomplished by horizontally blanking a number of AVID pulses and by vertically blanking a number of lines per frame. Horizontal cropping can be enabled/disabled using bit-6 of address B1h. When line cropping is enabled, active video will be reduced from 720 to 704 pixels for un-scaled video and from 360 to 352 pixels for down-scaled video.

When line cropping is enabled, the end of the active video line is actually cropped. Register 8Ch can be used to delay both the start and end of active video. It allows selecting which 704 pixels out of 720 are actually being used for active video when line cropping is enabled.

### 3.4 Embedded Syncs

Standards with embedded syncs insert SAV and EAV codes into the data stream at the beginning and end of horizontal blanking. These codes contain the V and F bits which also define vertical timing. F and V change on EAV. Table 3-1 gives the format of the SAV and EAV codes.

H equals 1 always indicates EAV. H equals 0 always indicates SAV. The alignment of V and F to the line and field counter varies depending on the standard. Please refer to ITU-R BT.656 for more information on embedded syncs.

The P bits are protection bits:

$$\begin{aligned} P3 &= V \text{ xor } H \\ P2 &= F \text{ xor } H \\ P1 &= F \text{ xor } V \\ P0 &= F \text{ xor } V \text{ xor } H \end{aligned}$$

**Table 3-1. EAV and SAV Sequence**

	8-BIT DATA							
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
Preamble	1	1	1	1	1	1	1	1
Preamble	0	0	0	0	0	0	0	0
Preamble	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0

### 3.5 Scaler

Each video decoder channel of TVP5158 has independently horizontal and vertical scaler, which supports D1 to half-D1 or CIF conversion. Table 3-2 gives the details of video resolution including un-cropped and cropped. Table 3-3 shows the video resolutions converted by the Scaler.

**Table 3-2. The Video Resolution**

Format	Uncropped		Cropped	
	NTSC	PAL	NTSC	PAL
D1	720 x 480	720 x 576	704 x 480	704 x 576
Half-D1	360 x 480	360 x 576	352 x 480	352 x 576
CIF	360 x 240	360 x 288	352 x 240	352 x 288

**Table 3-3. The Video Resolutions Converted by the Scaler**

Scaling Ratio	Format	Horizontal Scaling	Vertical Scaling	Total Pixel	Active Output Resolution
D1	NTSC	1:1	1:1	858 x 525	720 x 480
	PAL	1:1	1:1	864 x 625	720 x 576
D1 to Half-D1	NTSC	2:1	1:1	429 x 525	360 x 480
	PAL	2:1	1:1	432 x 625	360 x 576
D1 to CIF	NTSC	2:1	2:1	429 x 262	360 x 240
	PAL	2:1	2:1	432 x 312	360 x 288

### 3.6 Noise Reduction

A video sequence shot under low light condition, which is typical of video surveillance applications, can contain lots of noise. Human eyes are very sensitive to oscillating signals, the visual quality degenerates significantly even when the noise level is small.

TVP5158 uses a wavelet based spatial filter to reduce video noise. For each field of image, the video noise filter (VNF) produces an estimate of the Y/U/V noise. Based on the noise estimates, the firmware adjusts the threshold for Y/U/V filtering. The filtered video shows improved video quality and lower compression bit-rate. The firmware can also utilize the Y/U/V noise estimates to make decisions to disable color, should the video noise is determined to be too high. This “color killer” decision bit can be used to control another module that implements the color killing function.

The Noise Reduction can be controlled using I2C registers from 50h to 5Fh. This module can also be set to bypass mode by I2C register 5Dh (Bit 0).

### 3.7 Auto Contrast

The Auto Contrast (AC) module can adjust the picture brightness automatically or manually (user programmable) for better image quality. The goal of AC processing is to make the dark area brighter and high-light area dimmer. This makes it possible for the viewer to see details hidden in the shadows. It also prevents loss of details in the washed-out high light area. The AC processing is mostly for video surveillance market.

For each field of image, the auto contrast module collects the statistics of its Y (luminance) values. The AC algorithm implemented in the firmware processes the statistics and generates a look-up-table (LUT). This LUT is used to map each incoming pixel Y value to an output pixel Y value for the next field of image. The LUT is updated during the blanking period between two fields.

The Auto Contrast Mode can be controlled by using I2C registers 0Fh. This module can also be set to disable mode by I2C register 0Fh (Bit 1:0).

### 3.8 Output Formatter

The output formatter is responsible for generating the output digital video stream. Table 3-4 shows the Summary of Line Frequencies, Data Rates, and Pixel Counts for different Standards. TVP5158 supports non-interleave output mode, pixel-interleaved output mode and line-interleaved output mode. The non-interleave mode is almost compatible with TVP5154A device, except using single clock output. The interleave mode is to multiplex the video output data from multiple decoder channels and then output single bitstream through 8-bit or 16-bit ports. The video output data from selected channels can be interleaved by pixel or line base.

**Table 3-4. Summary of Line Frequencies, Data Rates, and Pixel Counts for different Standards**

STANDARDS (ITU-R BT.601)	PIXELS PER LINE	ACTIVE PIXELS PER LINE	LINES PER FRAME	PIXEL FREQUENCY (MHz)	COLOR SUB- CARRIER FREQUENCY (MHz)	HORIZONTAL LINE RATE (KHz)
NTSC-J, M	858	720	525	13.5	3.579545	15.73426
NTSC-4.43	858	720	525	13.5	4.43361875	15.73426
PAL-M	858	720	525	13.5	3.57561149	15.73426
PAL-60	858	720	525	13.5	4.43361875	15.73426
PAL-B, D, G, H, I	864	720	625	13.5	4.43361875	15.625
PAL-N	864	720	625	13.5	4.43361875	15.625
PAL-Nc	864	720	625	13.5	3.58205625	15.625

#### 3.8.1 Non-interleave output mode

For non-interleave mode, the YCbCr digital output can be programmed as 8-bit ITU-R BT.656 parallel interface standard. Depending on which output mode is selected, the output for each channel can be un-scaled data or scaled data. Also each video output port can be selected to output the video data from any one of 4 video decoders. Table 3-5 shows the detailed information about non-interleave mode.

**Table 3-5. The output ports configuration for Non-interleave mode**

Video Output Formats	Data Clock Rate (MHz)	I/F Type	DVO_A	DVO_B	DVO_C	DVO_D
1-Ch D1	27	Quad BT.656	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch
1-Ch Half-D1	27	Quad BT.656	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch
1-Ch CIF	27	Quad BT.656	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch

### 3.8.2 Pixel-interleaved mode

TVP5158 supports multiplexing two or four channels ITU-R BT.656 format data together by pixel base. The output from each video decoder channel is still ITU-R BT.656 format. After the processing in output formatter, two or four channels video data has been interleaved together by strictly one pixel from each channel.

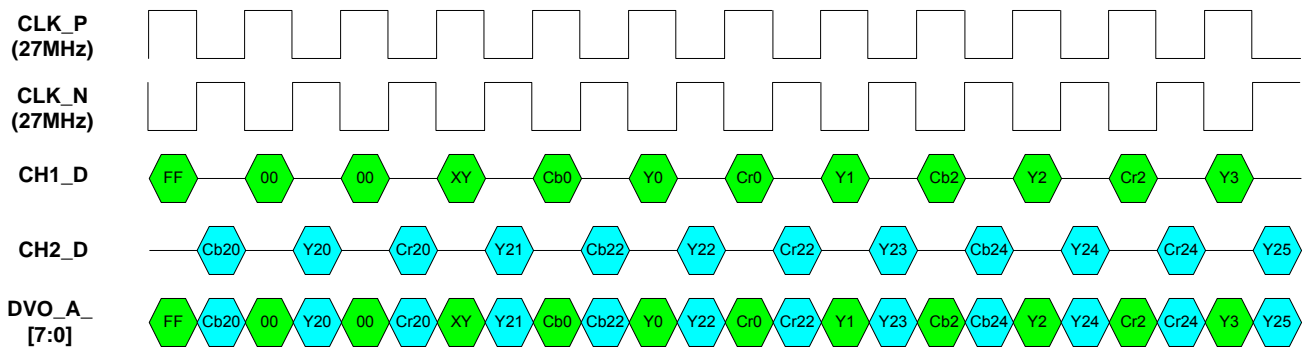
The pixel-interleaved mode is dedicated for the backend chip which has limited video input ports. Table 3-6 gives the output port configuration for pixel-interleaved mode.

**Table 3-6. The output ports configuration for pixel-interleaved mode**

Video Output Formats	Data Clock Rate (MHz)	I/F Type	Interleave Mode	DVO_A	DVO_B	DVO_C	DVO_D
2-Ch D1	54	Dual BT.656	Pixel Based	Any 2 of 4 Ch	Any 2 of 4 Ch	Hi-Z	Hi-Z
4-Ch D1	108	Single BT.656	Pixel Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch Half-D1	54	Single BT.656	Pixel Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch CIF	54	Single BT.656	Pixel Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z

#### 3.8.2.1 2-Ch pixel-interleaved mode

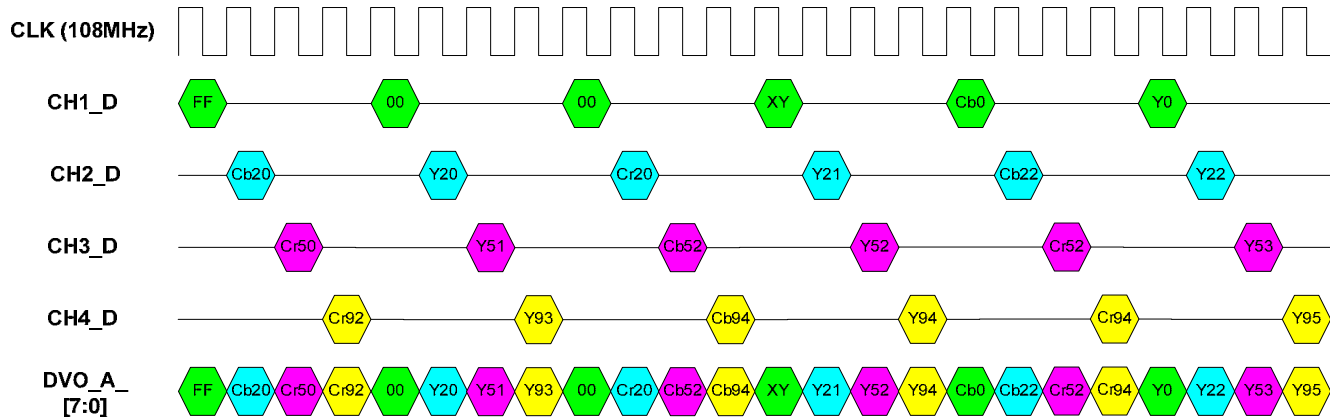
In 2-Ch pixel-interleaved mode, the video output data with D1 resolution from two video channels is multiplexed pixel by pixel at 54 MHz. The output ports DVO\_A and DVO\_B are used in this mode. The output clocks OCLK\_P and OCLK\_N are synchronized with each channel so that the backend chip can de-multiplexed each video channel data easily. The video output from each channel is compatible with ITU-R BT. 656 format. Figure 3-10 shows the timing diagram for 2-Ch pixel-interleaved mode.



**Figure 3-10. The timing diagram for 2-Ch pixel-interleaved mode**

### 3.8.2.2 4-Ch pixel-interleaved mode

In 4-Ch pixel-interleaved mode, the video output data with D1 resolution from four video channels is multiplexed pixel by pixel at 108 MHz. The output DVO\_A is used in this mode. The output clock OCLK\_P is synchronized with all four channels data. Each channel video data is compatible with ITU-R BT.656 format. Figure 3-11 shows the timing diagram for 4-Ch pixel-interleaved mode.



**Figure 3-11. The timing diagram for 4-Ch pixel-interleaved mode**

In 4-Ch pixel-interleaved mode, TVP5158 also supports Half-D1 and CIF format data multiplexed at 54 MHz. The output DVO\_A is used in this mode. The output clock OCLK\_P is synchronized with all four channels data.

### 3.8.2.3 Metadata Insertion for non-interleave mode and pixel-interleaved mode

In non-interleaved mode and pixel-interleaved mode, the video detection status (VDET) has also been inserted in MSB of SAV/EAV control byte. Table 3-7 shows VDET status insertion in SAV/EAV codes.

**Table 3-7. VDET Statuses Insertion in SAV/EAV Codes**

Condition			FVH Value			SAV/EAV Code Sequence				
Field	V time	H time	F	V	H	1st	2nd	3rd	4th	
									VDET=1	VDET=0
1	Active	SAV	0	0	0	FFh	00h	00h	80h	00h
1	Active	EAV	0	0	1	FFh	00h	00h	9Dh	1Dh
1	Blank	SAV	0	1	0	FFh	00h	00h	ABh	2Bh
1	Blank	EAV	0	1	1	FFh	00h	00h	B6h	36h
2	Active	SAV	1	0	0	FFh	00h	00h	C7h	47h
2	Active	EAV	1	0	1	FFh	00h	00h	DAh	5Ah
2	Blank	SAV	1	1	0	FFh	00h	00h	ECh	6Ch
2	Blank	EAV	1	1	1	FFh	00h	00h	F1h	71h

In the pixel-interleaved mode, Channel ID is inserted in the horizontal blanking code as Table 3-8. The backend chip can easily identify the video data from which video decoder channel by inserted Channel ID.

**Table 3-8. Channel ID Insertion in Horizontal Blanking Code**

Channel	H Blanking Code with Channel ID		
	Y	Cb	Cr
Ch1	10h	80h	80h
Ch2	11h	81h	81h
Ch3	12h	82h	82h
Ch4	13h	83h	83h

### 3.8.3 Line-interleaved modes

TVP5158 also supports line-interleaved modes to multiplex 2 or 4 video channels outputs together line by line. Compared to pixel-interleaved mode, the line-interleaved mode significantly reduces the code complexity and MIPS consumption of the backend DSP.

TVP5158 support 2-Ch and 4-Ch line-interleaved modes. Each mode supports different resolutions including D1, Half-D1 and CIF. Table 3-9 includes all line-interleaved mode supported by single TVP5158 chip.

**Table 3-9. TVP5158 line-interleaved modes**

Video Output Formats	Data Clock Rate (MHz)	I/F Type	Interleave Mode	DVO_A	DVO_B	DVO_C	DVO_D
2-Ch D1	54	Dual BT.656	Line Based	Any 2 of 4 Ch	Any 2 of 4 Ch	Hi-Z	Hi-Z
4-Ch D1	108	Single BT.656	Line Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch Half-D1	54	Single BT.656	Line Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch CIF	27	Single BT.656	Line Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch D1	54	16-Bit YUV 4:2:2	Line Based	All 4 Ch (Y data)	All 4 Ch (C data)	Hi-Z	Hi-Z
4-Ch Half-D1	27	16-Bit YUV 4:2:2	Line Based	All 4 Ch (Y data)	All 4 Ch (C data)	Hi-Z	Hi-Z
4-Ch CIF + 1-Ch D1	54	Single BT.656	Line Based	All 4 Ch CIF + Any 1 of 4 D1	Hi-Z	Hi-Z	Hi-Z
4-Ch Half-D1 + 1-Ch D1	81	Single BT.656	Line Based	All 4 Ch Half-D1 + Any 1 of 4 D1	Hi-Z	Hi-Z	Hi-Z



### 3.8.3.1 2-Ch line-interleaved mode

TVP5158 supports 2-Ch line-interleaved mode at 54 MHz. The video output data with D1 resolution from any two video channels is multiplexed together by line base. The output DVO\_A and DVO\_B are used in this mode. The output clock OCLK\_P is synchronized with two channels data.

### 3.8.3.2 4-Ch line-interleaved mode

In 4-Ch line-interleaved mode, the video output data from all 4 channels is multiplexed together by line base. The resolution of video data can be D1, Half-D1 or CIF. For D1 and Half-D1 output modes, the video output port can be configured to support 8-Bit BT.656 or 16-Bit YUV 4:2:2 data with embedded sync. The port DVO\_A is used for 8-Bit output. The port DVO\_A and DVO\_B are used for 16-Bit output. The output clock OCLK\_P is synchronized with all four channels data.

TVP5158 supports multiplexing 4-Ch CIF and 1-Ch D1 data together and then output through DVO\_A at 54 MHz. 1-Ch D1 can be from any one of 4 video channels. In surveillance product, CIF format is for the recording and D1 format is for video preview.

TVP5158 also supports multiplexing 4-Ch Half-D1 and 1-Ch D1 data together and then output through DVO\_A at 81 MHz. The backend chip can use Half-D1 to generate CIF format by dropped one field.

Please note, the line-interleaved mode is NOT strictly output one line from each decoder channel. The order of multiplexed the video line data is based on the availability of video output data from each decoder channel. Therefore it is possible to output two consecutive lines from same decoder channel or skip one decoder channel output.

### 3.8.3.3 Video Cascade mode

Two TVP5158 devices can be cascade connected and work as single 8-Ch video decoder. In cascade mode, the port DVO\_C and DVO\_D of master TVP5158 (1<sup>st</sup> stage) can be configured as the video input interface. The DVO\_A and DVO\_B of master TVP5158 are configured as the output interface for 2 devices. This mode is dedicated for the backend chip with extremely limited input ports. Table 3-10 includes all cascade modes in TVP5158.

For the modes of 4-Ch CIF + 1 - Ch D1 at 54 MHz and 8-Ch CIF + 1 - Ch D1 at 81 MHz modes, the D1 line is broken into two equal-length half lines and then multiplex with other CIF lines. Therefore, all video data is actually multiplexed by CIF line length. Additionally, in these two modes, both the scaled and un-scaled data streams must use the same line cropping setting. The cropping setting can be controlled by I2C register B1h (Bit 6).

**Table 3-10. TVP5158 Video Cascade Modes**

Video Output Formats	Cascade Stage	Data Clock Rate (MHz)	I/F Type	Interleave Mode	DVO_A	DVO_B	DVO_C	DVO_D
8-Ch CIF	2 <sup>nd</sup> Stage	27	Single BT.656	Line Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
	1 <sup>st</sup> Stage	54	Single BT.656	Line Based	All 8 Ch	Hi-Z	Hi-Z	4-Ch CIF Input
8-Ch Half-D1	2 <sup>nd</sup> Stage	54	Single BT.656	Line Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
	1 <sup>st</sup> Stage	108	Single BT.656	Line Based	All 8 Ch Half-D1	Hi-Z	Hi-Z	4-Ch Half-D1 Input
8-Ch CIF + 1-Ch D1	2 <sup>nd</sup> Stage	27/27	Dual BT.656	Line Based (2 <sup>nd</sup> Stage)	All 4 Ch CIF	Any 1 of 4 Ch D1	Hi-Z	Hi-Z
	1 <sup>st</sup> Stage	81	Single BT.656	Line Based	All 8 Ch CIF + Any 1 of 8 D1	Hi-Z	1-Ch D1 Input	4-Ch CIF Input

The typical applications with cascade mode show on next several pages.

Figure 3-12 shows the Cascade Connection for 16-Ch CIF Recoding and Multi-Ch CIF Preview.

Figure 3-13 shows the Cascade Connection for 16-Ch CIF Recoding and Multi-Ch Half-D1 Preview.

Figure 3-14 shows the Cascade Connection for 16-Ch CIF Recoding and 2-Ch D1/Multi-Ch CIF Preview.

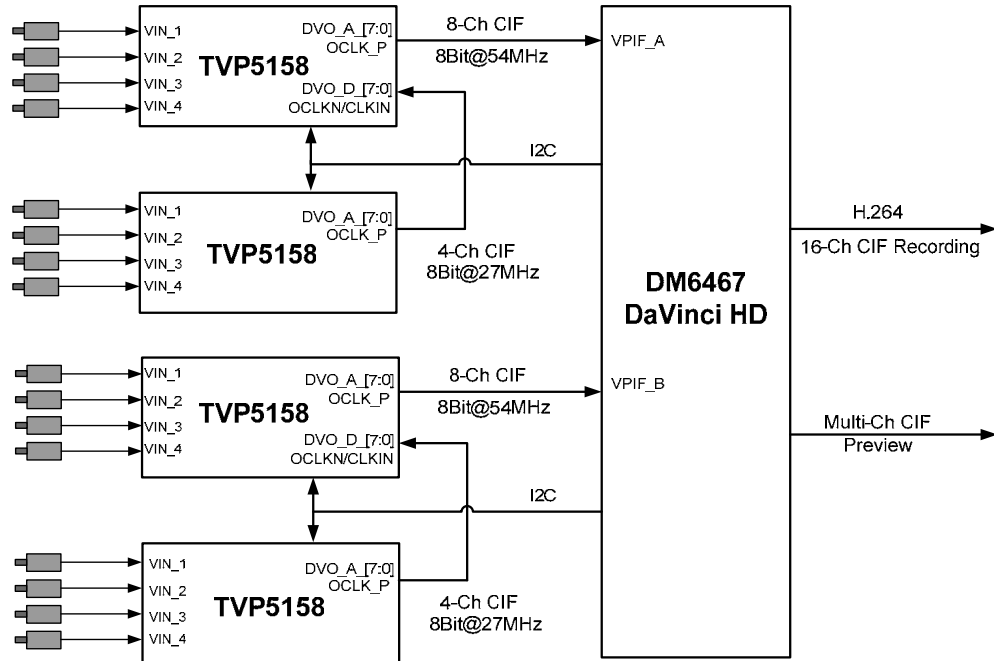


Figure 3-12. The Cascade Connection for 16-Ch CIF Recoding and Multi-Ch CIF Preview

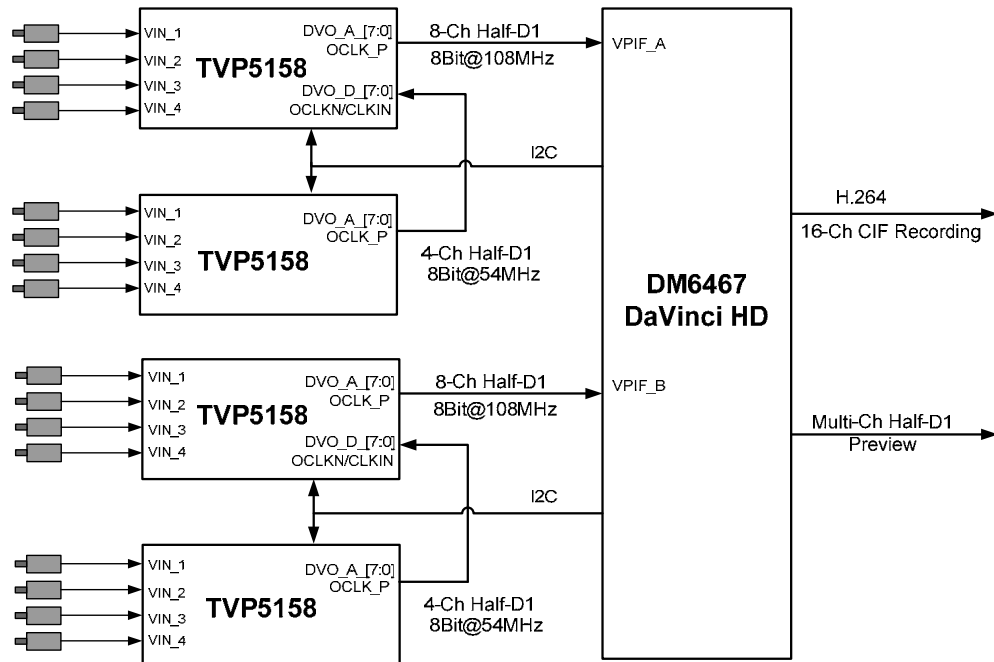
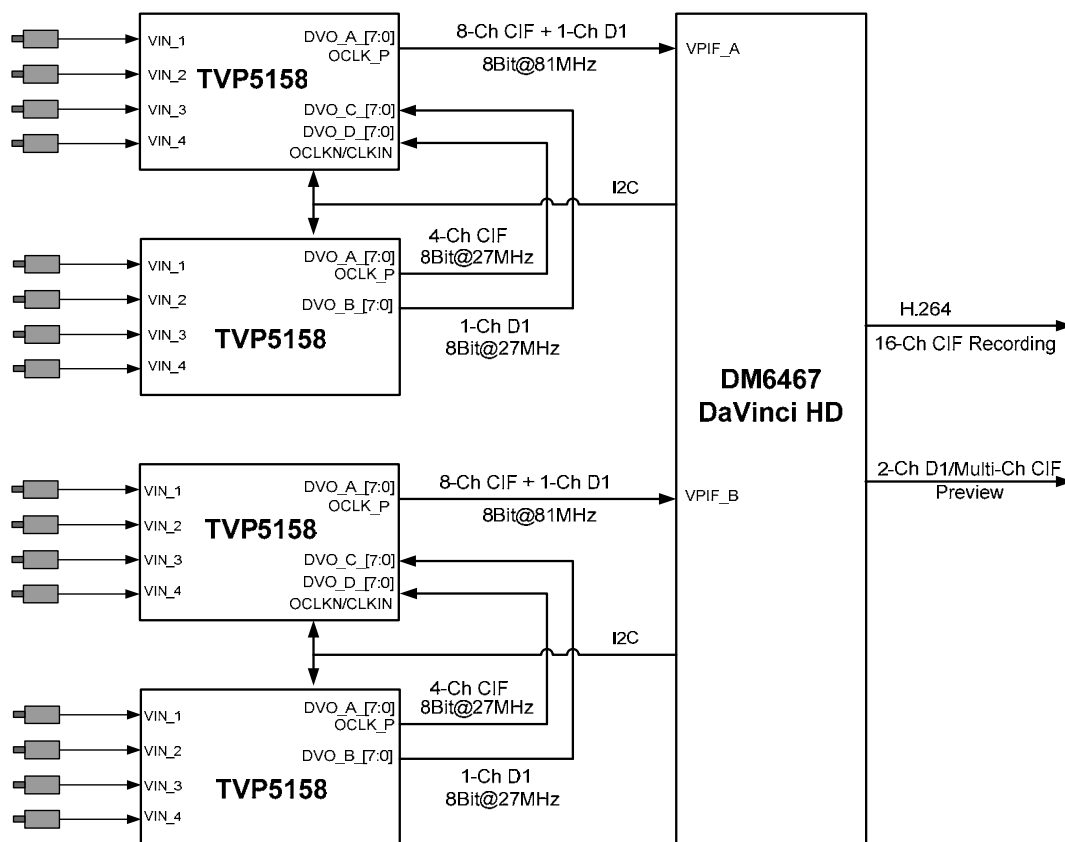


Figure 3-13. The Cascade Connection for 16-Ch CIF Recoding and Multi-Ch Half-D1 Preview



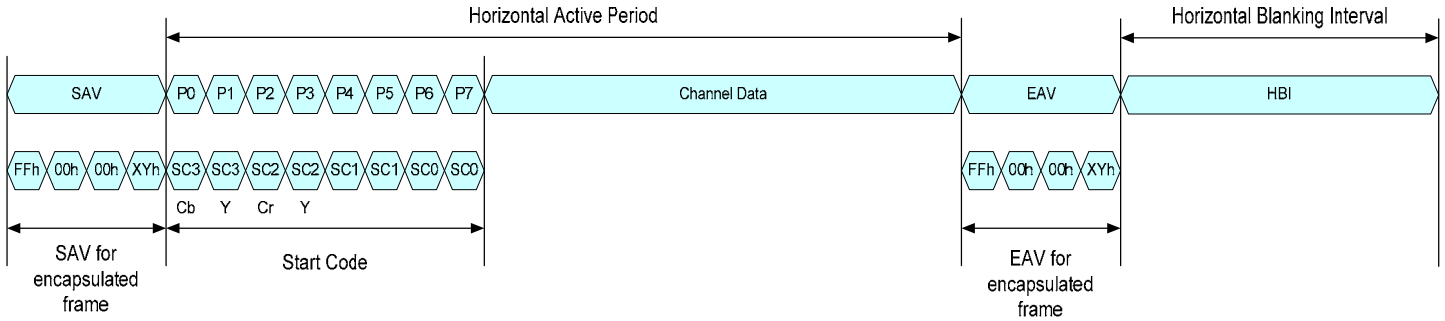
**Figure 3-14. The Cascade Connection for 16-Ch CIF Recoding and 2-Ch D1/Multi-Ch CIF Preview**

### 3.8.3.4 Metadata Insertion for line-interleaved mode

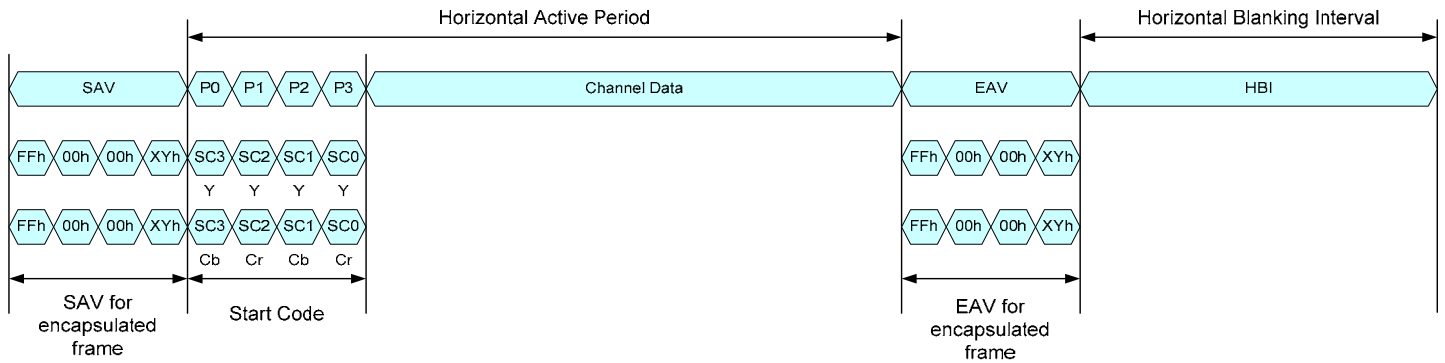
In the line-interleaved mode, the video data is rearranged on a line-by-line basis. So there can be no guarantee output line order since all analog video inputs are not synchronized. In order to be compatible with general backend BT.656 decoder, the video data is encapsulated on TVP5158 output so that all input data is preserved and output data is understandable to the BT decoder.

To prevent confusion over image line count and vertical blanking appearing haphazardly, SAV/EAV codes will have FID and V data stripped and replaced with FID=V=0. Since vertical blanking in the input is being masked out, artificial vertical sync will be inserted every encapsulated frame (Also called as Super Frame). Thus to the unaware BT decoder, the stream will appear to be progressive data with 2 lines of vertical blanking.

4-Byte Start Code (SC3:SC0) is inserted immediately after SAV code for encapsulated frame. Figure 3-15 and Figure 3-16 show the start code details.



**Figure 3-15. Start Code in 8-Bit BT.656 Interface**



**Figure 3-16. Start Code in 16-Bit YUV 4:2:2 Interface**

Table 3-11 and Table 3-12 shows the bit assignment and field definition of 4-Byte start code for Active Video Line.

**Table 3-11. The bit assignment of 4-Byte Start Code for Active Video Line**

Byte	7	6	5	4	3	2	1	0
SC[3]	1	RSVD	RSVD	RSVD		VCS_ID	CH_ID[1:0]	
SC[2]	0	BOL	EOL	VDET	RSVD		LN_ID[8:7]	
SC[1]	~LD_ID[6]	LN_ID[6:0]						
SC[0]	1	F	V	H	P3	P2	P1	P0

**Table 3-12. The Bit Field Definition of 4-Byte Start Code for Active Video Line**

Bit	Name	Function
31	1	Reserved. Must be set to 1.
30	RSVD	Reserved.
29	RSVD	Reserved.
[28:27]	RSVD	Reserved (to support up to 32 video channels)
26	VCS_ID	Video cascade stage ID. Set to 0 for normal operation. In cascade mode, the back-end device (e.g. TMS320DM6467) interfaces to the first stage. 0: First stage (channels 1 - 4) 1: Second stage (channels 5 - 8)
[25:24]	CH_ID[1:0]	2-bit Channel ID. Video decoder channel number. 00: Channel 1 01: Channel 2 10: Channel 3 11: Channel 4
23	0	Reserved. Must be set to 0.
22	BOL	Active-high beginning of line flag. Used in split-line mode which may be required for hybrid formats (e.g. 1-Ch D1 + 8-Ch CIF). Set high when the current encapsulated line of channel data includes the beginning of a video line. 0: BOL not included (2nd half of split line) 1: BOL included (1st half of split line or full line)
21	EOL	Active-high end of line flag. Used in split-line mode which may be required for hybrid formats (e.g. 1-Ch D1 + 8-Ch CIF). Set high when the current line of channel data includes the end of a video line. 0: EOL not included (1st half of split line) 1: EOL included (2nd half of split line or full line)
20	VDET	Active-high video detection status 0: Video not detected 1: Video detected
[19:18]	RSVD	Reserved
[17:16]	LN_ID[8:7]	2 MSBs of 9-bit Line ID, active video line number. Line counter resets to 000h at beginning of active video (i.e. resets once per field). During the vertical blanking interval, the line counter may either continue counting or hold the terminal count determined at the end of active video.
15	~LN_ID[6]	Reserved. Must be set to the complement of bit 14 (LN_ID[6]).
[14:8]	LN_ID[6:0]	7 LSBs of 9-bit Line ID, active video line number. Line counter resets to 000h at beginning of active video (i.e. resets once per field). During the vertical blanking interval, the line counter may either continue counting or hold the terminal count determined at the end of active video.
7	1	Reserved. Must be set to 1.
6	F	F-bit 0: First field of frame 1: Second field of frame
5	V	V-bit 0: when not in vertical blanking 1: during vertical blanking

Bit	Name	Function
4	H	H-bit. Always set to 0. 0: SAV 1: EAV (never used)
3	P3	$P3 = V \text{ XOR } H$ , Protection bits used for error detection/correction
2	P2	$P2 = F \text{ XOR } H$ , Protection bits used for error detection/correction
1	P1	$P1 = F \text{ XOR } V$ , Protection bits used for error detection/correction
0	P0	$P0 = F \text{ XOR } V \text{ XOR } H$ , Protection bits used for error detection/correction

Please note, for line-interleaved output mode, if none of video decoder channels has the data ready at a given time, TVP5158 will output the dummy line until any one of video decoder channels is ready to output a line. The backend chip needs to keep only active video line and ignore the dummy line.

The start code of the dummy line is different with active video line. Table 3-13 shows the bit assignment and field definition of 4-Byte start code for the Dummy Line.

**Table 3-13. The bit assignment of 4-Byte Start Code for the Dummy Line**

Byte	7	6	5	4	3	2	1	0
SC[3]	0	0	0	0	0	0	0	1
SC[2]	0	0	0	0	0	0	0	1
SC[1]	0	0	0	0	0	0	0	1
SC[0]	0	0	0	0	0	0	0	1

Note: The Dummy Line can be easily distinguished from active video line by simply looking at the MSB of byte SC[0].

## 3.9 Audio Sub-system

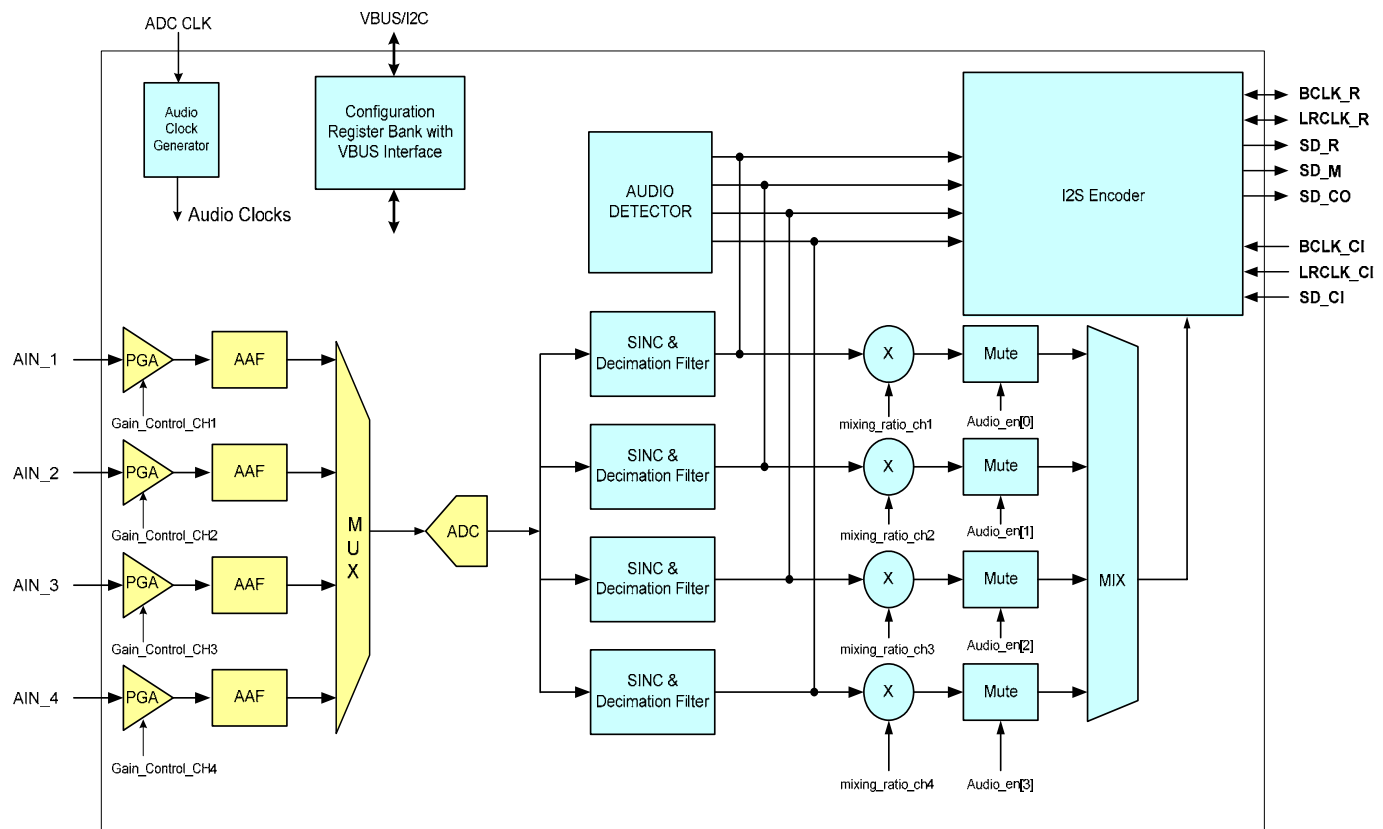
The audio sub-system integrates 4-Ch audio Analog-to-Digital converters, digital processing and I2S Encoder. TVP5158 audio sub-system supports 4-Ch mono analog audio input and standard/multiple I2S output. TVP5158 also supports Audio Cascade Connection up to 4 devices cascade connected for 16-Ch audio input.

### 3.9.1 Features

- Four channel mono analog audio inputs
  - Input Voltage Range : 1 Vpp (Max)
  - Requires external passive attenuator to support 2.828-Vpp analog audio input
- Programmable Gain Amplifier (PGA)
  - Gain range : -12 ~ 10.5 dB, Gain Step : 1.5 dB
- Integrated Anti-Aliasing Filter (AAF)
- 10-Bit Analog-to-Digital Converter
- Integrates Audio High-pass filter to eliminate low frequency hum
- Digital serial audio interface
  - 16-Bit Linear PCM, 8-Bit A-Law and 8-Bit  $\mu$ -Law Data
  - I2S or DSP Format
  - Master and Slave mode operation
  - Up to 16 slots TDM output
  - 64  $f_s$  or 256  $f_s$  system clock
- Sampling Rate : 16 kHz , 8 kHz
- Audio Cascade connection
  - Up to 4 cascaded devices
  - I2S format
  - 256  $f_s$  system clock
- Audio Mixing Output
  - Audio ADC has one register to set mix ratio.
  - The Mixing output pin SD\_M can also be used for recording. Combined with the recording output pin SD\_R, TVP5158 can output two I2S bit-streams simultaneously.



### 3.9.2 Audio Sub-System Functional Diagram



**Figure 3-17. Audio Sub-System Functional Diagram**

PRODUCT PREVIEW

### 3.9.3 Audio Cascade Connection

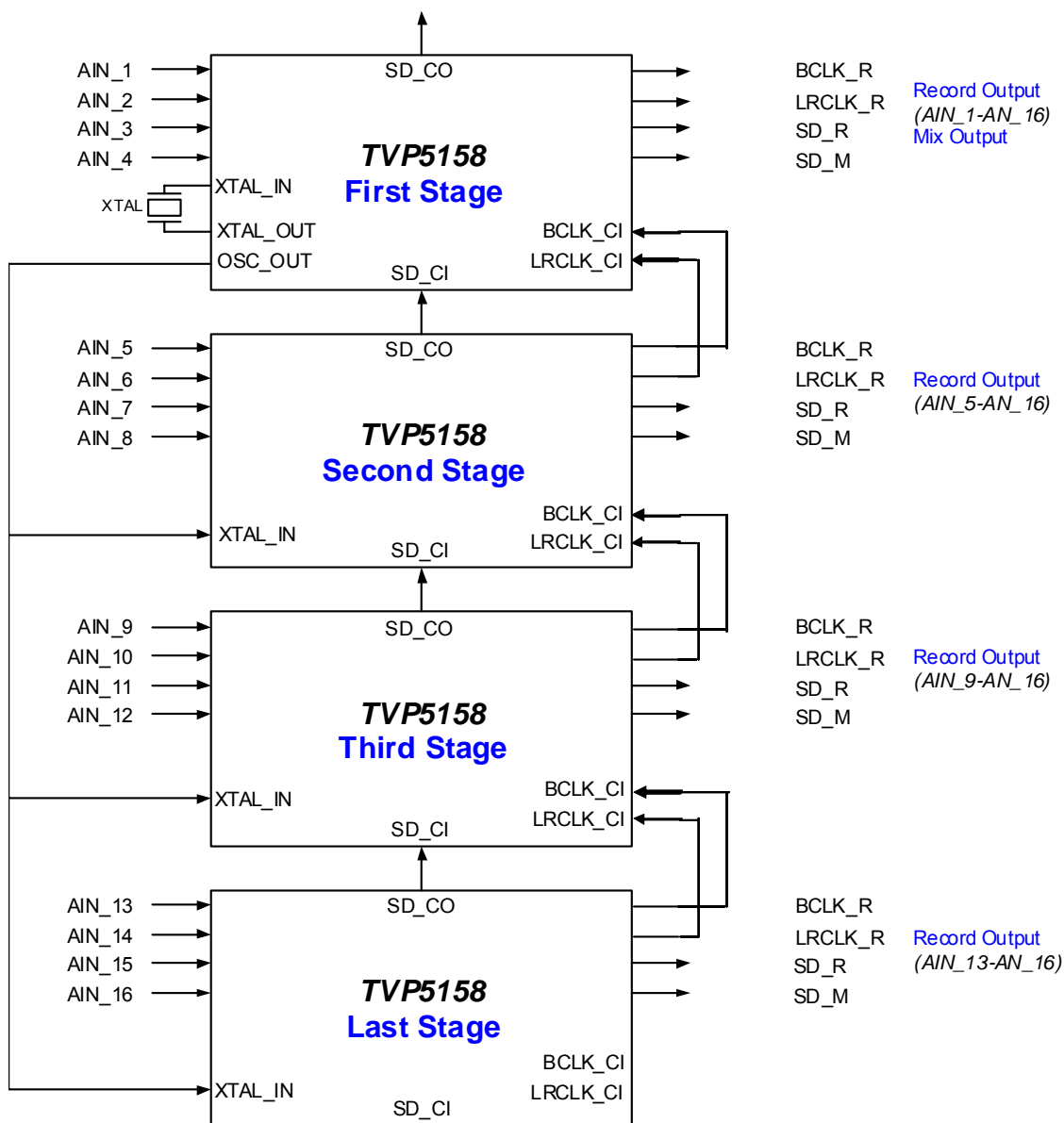


Figure 3-18. Audio Cascade Connection

TVP5158 supports up to 4 devices cascade together for Audio Cascade Connection. The I2S output of master TVP5158 (1<sup>st</sup> stage) combines all audio channel data from slave TVP5158 devices.

### Key features on Audio Cascade Connection

- 16-Bit Linear PCM Data
- I2S Format
- Bit Clock: 256 Fs
- All cascade inputs are always in slave mode
- 2nd to 4th stage serial audio outputs are always in master mode
- 1st stage serial audio output can be in either master or slave mode
- Common clock source for all cascaded devices is required

The Serial Audio Output Channel Assignment shown on Table 3-14.

I2S

			LRCLK_R Left								LRCLK_R Right							
Number of Audio channels to TDM (I2C addr C4 Bit[2:0])	TDM out pin select (I2C addr C3 Bit [0])		Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8	Slot 9	Slot 10	Slot 11	Slot 12	Slot 13	Slot 14	Slot 15	Slot 16
0 (2 channel)	0	SD_R	AIN_1								AIN_2							
		SD_M																
	1	SD_R	AIN_1															
		SD_M	AIN_2															
1 (4 channel)	0	SD_R	AIN_1	AIN_3							AIN_2	AIN_4						
		SD_M																
	1	SD_R	AIN_1								AIN_2							
		SD_M	AIN_3								AIN_4							
2 (8 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7					AIN_2	AIN_4	AIN_6	AIN_8				
		SD_M																
	1	SD_R	AIN_1	AIN_5							AIN_2	AIN_6						
		SD_M	AIN_3	AIN_7							AIN_4	AIN_8						
3 (12 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_9	AIN_11			AIN_2	AIN_4	AIN_6	AIN_8	AIN_10	AIN_12		
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_9						AIN_2	AIN_6	AIN_10					
		SD_M	AIN_3	AIN_7	AIN_11						AIN_4	AIN_8	AIN_12					
4 (16 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_9	AIN_11	AIN_13	AIN_15	AIN_2	AIN_4	AIN_6	AIN_8	AIN_10	AIN_12	AIN_14	AIN_16
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_9	AIN_13					AIN_2	AIN_6	AIN_10	AIN_14				
		SD_M	AIN_3	AIN_7	AIN_11	AIN_15					AIN_4	AIN_8	AIN_12	AIN_16				

SD\_M output is selected by Audio mixer output select register (I2C addr C4 Bit[7:3])

DSP Format

Number of Audio channels to TDM (I2C addr C4 Bit [2:0])	TDM out pin select (I2C addr C3 Bit [0])																	
		Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8	Slot 9	Slot 10	Slot 11	Slot 12	Slot 13	Slot 14	Slot 15	Slot 16	
0 (2 channel)	0	SD_R	AIN_1	AIN_2														
		SD_M																
	1	SD_R	AIN_1															
		SD_M	AIN_2															
1 (4 channel)	0	SD_R	AIN_1	AIN_3	AIN_2	AIN_4												
		SD_M																
	1	SD_R	AIN_1	AIN_2														
		SD_M	AIN_3	AIN_4														
2 (8 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_2	AIN_4	AIN_6	AIN_8								
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_2	AIN_6												
		SD_M	AIN_3	AIN_7	AIN_4	AIN_8												
3 (12 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_9	AIN_11	AIN_2	AIN_4	AIN_6	AIN_8	AIN_10	AIN_12				
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_9	AIN_2	AIN_6	AIN_10										
		SD_M	AIN_3	AIN_7	AIN_11	AIN_4	AIN_8	AIN_12										
4 (16 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_9	AIN_11	AIN_13	AIN_15	AIN_2	AIN_4	AIN_6	AIN_8	AIN_10	AIN_12	AIN_14	AIN_16
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_9	AIN_13	AIN_2	AIN_6	AIN_10	AIN_14								
		SD_M	AIN_3	AIN_7	AIN_11	AIN_15	AIN_4	AIN_8	AIN_12	AIN_16								

SD\_M output is selected by Audio mixer output select register (I2C addr C4 Bit[7:3])

**Table 3-14. The Serial Audio Output Channel Assignment**

### 3.10 I<sup>2</sup>C Host Interface

The I<sup>2</sup>C standard consists of two signals, serial input/output data line (SDA) and input/output clock line (SCL), which carry information between the devices connected to the bus. The input pins I2CA0, I2CA1 and I2CA2 are used to select the slave address to which the device responds. Although the I<sup>2</sup>C system can be multi-mastered, the TVP5158 decoder functions as a slave device only.

Both SDA and SCL must be connected to IOVDD via pullup resistors. When the bus is free, both lines are high. The slave address select terminals (I2CA0, I2CA1 and I2CA2) enable the use of eight TVP5158 decoders on the same I<sup>2</sup>C bus. At the trailing edge of reset the status of the I2CA0, I2CA1 and I2CA2 lines are sampled to determine the device address used. Table 3-15 summarizes the terminal functions of the I<sup>2</sup>C-mode host interface. Table 3-16 shows the device address selection options.

**Table 3-15. I2C Terminal Description**

SIGNAL	TYPE	DESCRIPTION
I2CA0	I	Slave address selection
I2CA1	I	Slave address selection
I2CA2	I	Slave address selection
SCL	I/O (open drain)	Input/output clock line
SDA	I/O (open drain)	Input/output data line

**Table 3-16. I2C Host Interface Device Addresses**

A6	A5	A4	A3	A2(I2CA2)	A1(I2CA1)	A0 (I2CA0)	R/W	HEX
1	0	1	1	0	0	0	1/0	B1/B0
1	0	1	1	0	0	1	1/0	B3/B2
1	0	1	1	0	1	0	1/0	B5/B4
1	0	1	1	0	1	1	1/0	B7/B6
1	0	1	1	1	0	0	1/0	B9/B8
1	0	1	1	1	0	1	1/0	BB/BA
1	0	1	1	1	1	0	1/0	BD/BC
1	0	1	1	1	1	1	1/0	BF/BE

Data transfer rate on the bus is up to 400 kbits/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the SCL except for start and stop conditions. The high or low state of the data line can only change with the clock signal on the SCL line being low. A high-to-low transition on the SDA line while the SCL is high indicates an I<sup>2</sup>C start condition. A low-to-high transition on the SDA line while the SCL is high indicates an I<sup>2</sup>C stop condition.

Every byte placed on the SDA must be 8 bits long. The number of bytes which can be transferred is unrestricted. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the I<sup>2</sup>C master.

To simplify programming of each of the 4 decoder channels a single I2C write transaction can be transmitted to any one or more of the 4 cores in parallel. This reduces the time required to download firmware or to configure the

device when all channels are to be configured in the same manner. It also enables the addresses for all registers to be common across all decoders.

I2C sub-address 0xFE contains 4 bits with each bit corresponding to one of the decoder cores. If this bit is set, then I2C write transactions will be sent to the corresponding decoder core. If the bit is 0 then the corresponding decoder will not receive the I2C write transactions.

I2C sub-address 0xFF contains 4 bits with each bit corresponding to one of the decoder cores. If this bit is set, then I2C read transactions will be sent to the corresponding decoder core. Note, only one of the bits in this register should be set at a given time, ensuring that only one decoder core is accessed at a time for read operations. If more than one bit is set then the lowest set bit number will correspond to the core that will respond to the read transaction.

Note, when register 0xFE is written to with any value then register 0xFF will be set to 0x00. Likewise when register 0xFF is written to with any value then register 0xFE will be set to 0x00.

### 3.10.1 I<sup>2</sup>C Write Operation

Data transfers occur utilizing the following formats.

An I<sup>2</sup>C master initiates a write operation to the TVP5158 decoder by generating a start condition (S) followed by the TVP5158 I<sup>2</sup>C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TVP5158 decoder, the master presents the sub-address of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The TVP5158 decoder acknowledges each byte after completion of each transfer. The I<sup>2</sup>C master terminates the write operation by generating a stop condition (P).

<b>Step 1</b>	<b>0</b>
I <sup>2</sup> C Start (master)	S

<b>Step 2</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C General address (master)	1	0	1	1	1	0	X	0

<b>Step 3</b>	<b>9</b>
I <sup>2</sup> C Acknowledge (slave)	A

<b>Step 4</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C Write register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

<b>Step 5</b>	<b>9</b>
I <sup>2</sup> C Acknowledge (slave)	A

<b>Step 6</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

<b>Step 7<sup>†</sup></b>	<b>9</b>
I <sup>2</sup> C Acknowledge (slave)	A

<b>Step 8</b>	<b>0</b>
I <sup>2</sup> C Stop (master)	P

<sup>†</sup> Repeat steps 6 and 7 until all data have been written.

### 3.10.2 I<sup>2</sup>C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I<sup>2</sup>C master initiates a write operation to the TVP5158 decoder by generating a start condition (S) followed by the TVP5158 I<sup>2</sup>C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TVP5158 decoder, the master presents the sub-address of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I<sup>2</sup>C master initiates a read operation to the TVP5158 decoder by generating a start condition followed by the TVP5158 I<sup>2</sup>C address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TVP5158 decoder, the I<sup>2</sup>C master receives one or more bytes of data from the TVP5158 decoder. The I<sup>2</sup>C master acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the TVP5158 decoder to the master, the master generates a not acknowledge followed by a stop.

#### Read Phase 1

<b>Step 1</b>	<b>0</b>
I <sup>2</sup> C Start (master)	S

<b>Step 2</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C General address (master)	1	0	1	1	1	0	X	0

<b>Step 3</b>	<b>9</b>
I <sup>2</sup> C Acknowledge (slave)	A

<b>Step 4</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C Read register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

<b>Step 5</b>	<b>9</b>
I <sup>2</sup> C Acknowledge (slave)	A

<b>Step 6</b>	<b>0</b>
I <sup>2</sup> C Stop (master)	P

#### Read Phase 2

<b>Step 7</b>	<b>0</b>
I <sup>2</sup> C Start (master)	S

<b>Step 8</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C General address (master)	1	0	1	1	1	0	X	1

<b>Step 9</b>	<b>9</b>
I <sup>2</sup> C Acknowledge (slave)	A

<b>Step 10</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
I <sup>2</sup> C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

<b>Step 11<sup>†</sup></b>	<b>9</b>
I <sup>2</sup> C Not acknowledge (master)	A

<b>Step 12</b>	<b>0</b>
I <sup>2</sup> C Stop (master)	P

<sup>†</sup> Repeat steps 10 and 11 for all bytes read. Master does not acknowledge the last read data received.

### 3.10.3 I<sup>2</sup>C Timing Requirements

The TVP5158 decoder requires delays in the I<sup>2</sup>C accesses to accommodate its internal processor's timing. In accordance with I<sup>2</sup>C specifications, the TVP5158 decoder holds the I<sup>2</sup>C clock line (SCL) low to indicate the wait period to the I<sup>2</sup>C master. If the I<sup>2</sup>C master is not designed to check for the I<sup>2</sup>C clock line held-low condition, then the maximum delays must always be inserted where required. These delays are of variable length; maximum delays are indicated in the following diagram:

Normal register writing address 00h-8Fh (addresses 90h-FFh do not require delays)

Start	Slave address (B8h)	Ack	Subaddress	Ack	Data (XXh)	Ack	Wait 128 $\mu$ s*	Stop
-------	---------------------	-----	------------	-----	------------	-----	-------------------	------

If the SCL pin is not monitored by the master to enable pausing, then a delay of 128  $\mu$ s should be inserted between transactions for registers 00h through 8Fh.



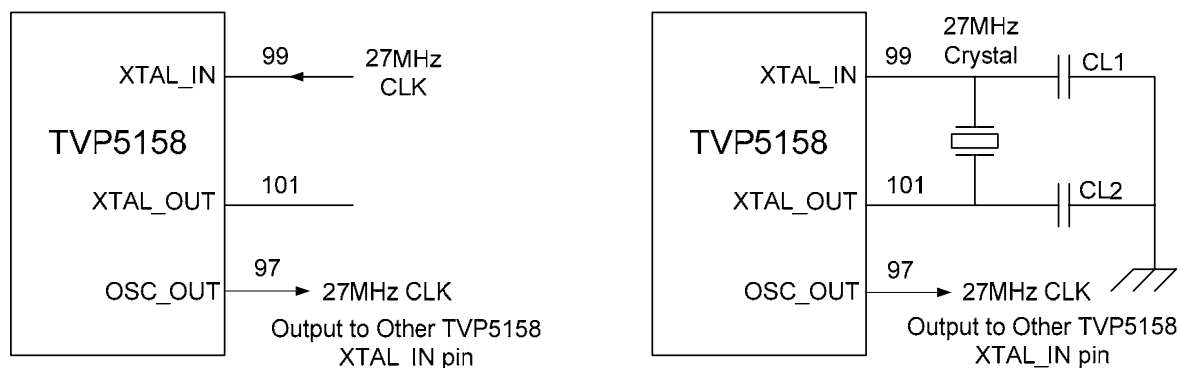
### 3.11 Clock Circuits

An internal line-locked PLL generates the system and pixel clocks. A 27-MHz clock is required to drive the PLL. This may be clock input to the TVP5158 decoder on terminal 99 (XTAL\_IN), or a crystal of 27-MHz fundamental resonant frequency may be connected across terminals 99 and 101 (XTAL\_OUT). Figure 3-20 shows the reference clock configurations. For the example crystal circuit shown (a parallel-resonant crystal with 27-MHz fundamental frequency), the external capacitors must have the following relationship:

$$C_{L1} = C_{L2} = 2C_L - C_{STRAY},$$

where  $C_{STRAY}$  is the terminal capacitance with respect to ground.

Terminal 97 (OSC\_OUT) outputs 27-MHz clock which can be connected to the XTAL\_IN pin of other TVP5158 devices.



**Figure 3-19. Clock and Crystal Connectivity.**

### 3.12 Reset Mode

Terminals 3 (RESETB) is active low signal to hold the TVP5158 decoder into reset modes.

Table 3-17 shows the configuration of reset mode. Table 3-18 describes the status of the TVP5158 terminals during and immediately after reset.

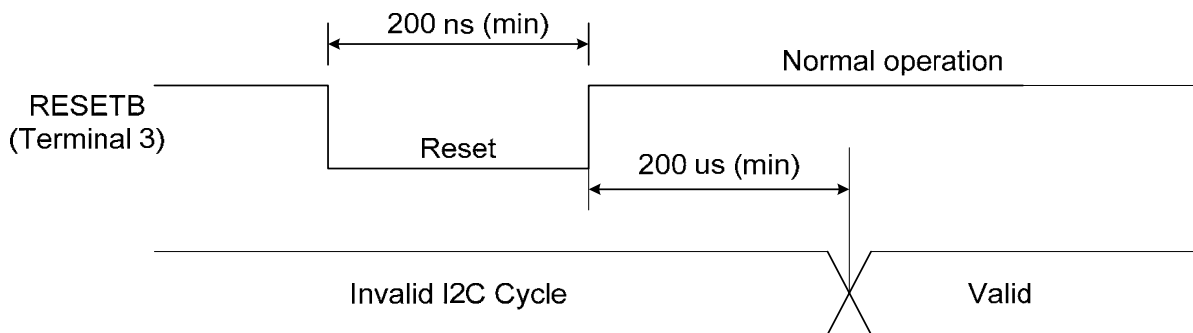
After power-up the device will be in an unknown state, with it's outputs undefined, until it receives a RESETB active low for at least 200 ns. The power supplies should be active and stable for 10 ms before RESETB becomes inactive. There are no power sequencing requirements except that all power supplies should become active and stable within 500 ms of each other.

**Table 3-17. Reset Mode**

RESETB	CONFIGURATION
0	Resets the decoder
1	Normal operation

**Table 3-18. Reset Sequence**

SIGNAL NAME	DURING RESET	RESET COMPLETED
DVO_A_[7:0], DVO_B_[7:0], DVO_C_[7:0], DVO_D_[7:0], OCLK_P, OCLK_N, INTREQ, OSC_OUT, I2CA[2:0], GPIO, BCLK_R, LRCLK_R, SD_R, SD_M, SD_CO, XTAL_OUT	Input	High-impedance
RESETB, SDA, SCL, LRCLK_CI, BCLK_CI, SD_CI, XTAL_IN	Input	Input



**Figure 3-20. Reset Timing**

## 4. Internal Control Registers

The TVP5158 decoder is initialized and controlled by a set of internal registers which set all device operating parameters. Communication between the external controller and the TVP5158 decoder is through I<sup>2</sup>C. Table 3-19 shows the summary of these registers. The reserved registers must not be written. Reserved bits in the defined registers must be written with 0s, unless otherwise noted. The detailed programming information of each register is described in the following sections.

I2C register 0xFE controls which of the four decoders will receive I2C commands. I2C register 0xFF controls which decoder core responds to I2C reads. Note, for a read operation it is necessary to perform a write first in order to set the desired sub-address for reading.

Compared to previous video decoder TVP5154A, TVP5158 adds decoder auto increment and address auto increment bits control. If decoder auto increment bit is set, the next read/write is from/to the next decoder that is enabled. If address auto increment bit is set, the address will be increment after all the decoders enabled read/write completed. The detail of I2C registers FEh and FFh shows below:

- Decoder write enable**

Address	FEh
Default	0Fh

7	6	5	4	3	2	1	0
Reserved		Addr Auto Incr	Decoder Auto Incr	Decoder 4	Decoder 3	Decoder 2	Decoder 1

This register controls which of the four decoder cores receives I2C write transactions. A '1' in the corresponding bit position will enable the decoder to receive write commands.

Any combination of decoders can be configured to receive write commands, allowing all four decoders to be programmed concurrently.

A '1' in Decoder Auto Increment will write the next byte to the next enable decoder. For example, if 2 bytes need to be written and Decoder 1 and Decoder 3 are enabled, the 1<sup>st</sup> byte will go to Decoder 1 and the 2<sup>nd</sup> byte will go to Decoder 2. A '0' in Decoder Auto Increment makes the operation same as TVP5154A.

A '1' in Address Auto Increment will increment the address after a write to decoder completed. For example, if 4 bytes need to be written and Decoder 1 and Decoder 3 are enabled, the first byte goes to Decoder1, the second byte goes to Decoder3, the third byte goes to next address of Decoder 1, the fourth byte goes to the next address of Decoder3.

- **Decoder read enable**

Address	FFh
Default	00h

7	6	5	4	3	2	1	0
Reserved	Addr Auto Incr	Decoder Auto Incr	Decoder 4	Decoder 3	Decoder 2	Decoder 1	

This register controls which of the four decoder cores responds to I2C read transactions. A '1' in the corresponding bit position will enable the decoder to respond to read commands.

If more than one decoder is enabled for reading then the lowest numbered decoder only will respond. Reads from multiple decoders at the same time is not possible.

A '1' in Decoder Auto Increment will read the next byte to the next enable decoder. For example, if 2 bytes need to be read and Decoder 1 and Decoder 3 are enabled, the 1<sup>st</sup> byte is from Decoder1 and the 2<sup>nd</sup> byte is from Decoder3.

A '1' in Address Auto Increment will increment the address after a read to decoder completed. For example, if 4 bytes need to be read and Decoder 1 and Decoder 3 are enabled, the 1<sup>st</sup> byte from Decoder 1, the 2<sup>nd</sup> byte from Decoder 3, the 3<sup>rd</sup> byte from the next address of Decoder 1, the 4<sup>th</sup> byte from the next address of Decoder 3.

**Table 4-1. Registers Summary**

REGISTER NAME	I2C SUBADDRESS	DEFAULT	R/W
Status 1	00h		R
Status 2	01h		R
Color Subcarrier Phase Status	02h		R
Reserved	03h		
ROM Version	04h		R
Reserved	05h - 07h		
Chip ID MSB	08h	51h	R
Chip ID LSB	09h	58h	R
Reserved	0Ah - 0Bh		
Video Standard Status	0Ch		R
Video Standard Select	0Dh	00h	R/W
CVBS/S-Video Autoswitch Mask	0Eh	03h	R/W
Auto Contrast Mode	0Fh	03h	R/W
Luminance Brightness	10h	80h	R/W
Luminance Contrast	11h	80h	R/W
Reserved	12h	00h	R/W
Chrominance Saturation	13h	80h	R/W
Chrominance Hue	14h	00h	R/W
CTI Control	15h	00h	R/W
Color Killer	16h	10h	R/W
Reserved	17h		
Luminance Processing Control 1	18h	40h	R/W
Luminance Processing Control 2	19h	00h	R/W
Power Control	1Ah	00h	R/W
Chrominance Processing Control 1	1Bh	00h	R/W
Chrominance Processing Control 2	1Ch	0Ch	R/W
Reserved	1Dh - 1Eh		
GPIO Input 2	1Fh		R

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REGISTER NAME	I2C SUBADDRESS	DEFAULT	R/W
AGC Gain Status 1	20h		R
AGC Gain Status 2	21h		R
Reserved	22h		
Back-End AGC Status	23h		R
Status Request	24h	00h	R/W
AFE Gain Control	25h	F5h	R/W
Luma ALC Freeze Upper Threshold	26h	00h	R/W
Chroma ALC Freeze Upper Threshold	27h	00h	R/W
Reserved	28h		
AGC Increment Speed	29h	06h	R/W
AGC Increment Delay	2Ah	1Eh	R/W
AGC Decrement Speed	2Bh	04h	R/W
AGC Decrement Delay	2Ch	00h	R/W
AGC White Peak Processing	2Dh	F2h	R/W
Back-End AGC Control	2Eh	08h	R/W
Reserved	2Fh - 31h		
Coarse Gain	32h	00h	R/W
Auto_Contrast_pixel_delay	33h	00h	R/W
AFE Fine Gain for G/Y/Luma/CVBS	34h - 35h	086Ah	R/W
Reserved	36h - 37h		
Auto_Contrast_Start_Pixel	38h - 39h	007Ah	R/W
Auto_Contrast_Pixel_Width	3Ah - 3Bh	02D0h	R/W
Auto_Contrast_Start_Line	3Ch - 3Dh	0019h	R/W
Auto_Contrast_Line_Length	3Eh - 3Fh	00F0h	R/W
HS Start Pixel	40h - 41h	0325h	R/W
HS Stop Pixel	42h - 43h	0040h	R/W
VS Start Line	44h - 45h	0004h/0001h	R/W
VS Stop Line	46h - 47h	0007h/0004h	R/W
AVID Start Pixel LSBs	48h	7Ah/84h	R/W
AVID Start Pixel MSBs	49h	00h/00h	R/W
AVID Pixel Width	4Ah - 4Bh	02D0h/02D0h	R/W
VBLK Start Line	4Ch - 4Dh	0001h/026Fh	R/W
VBLK Stop Line	4Eh - 4Fh	0015h/0018h	R/W
NR_Start_Avid_Pixel	50h - 51h	000Ah	R/W
NR_Avid_Pixel_Width	52h - 53h	0346h	R/W
NR_Start_Noiseest_Pixel	54h - 55h	0014h	R/W
NR_Noiseest_Pixel_Width	56h - 57h	0332h	R/W
NR_Start_Noiseest_Line	58h - 59h	000Ah	R/W
NR_Noiseest_Line_Length	5Ah - 5Bh	01F9h	R/W
NR_Max_Noise	5Ch	28h	R/W
NR_Control	5Dh	09h	R/W
NR_Noise_Filter	5Eh - 5Fh	0330h	R/W
Operation Mode Control	60h	00h	R/W
Color PLL Speed Control	61h	09h	R/W
Reserved	62h - 7Bh		
Sync Height Low Threshold	7Ch	02h	R/W
Sync Height High Threshold	7Dh	08h	R/W
Reserved	7Eh - 80h	03h	R/W
Clear Lost Lock Detect	81h	00h	R/W
Reserved	82h - 84h		
V-Sync Filter Shift	85h	03h	R/W
Reserved	86h		
656 Version/F Bit Control	87h	00h	R/W
F- and V-Bit Decode Control	88h	00h	R/W
F- and V-Bit Control	89h	16h	R/W
Reserved	8Ah - 8Bh		

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REGISTER NAME	I2C SUBADDRESS	DEFAULT	R/W
Output Timing Delay	8Ch	00h	R/W
Reserved	8Dh		
MaxGradient	8Eh	34h	R/W
MinGradient	8Fh	08h	R/W
“Blue” Screen Y Control	90h	10h	R/W
“Blue” Screen Cb Control	91h	80h	R/W
“Blue” Screen Cr Control	92h	80h	R/W
“Blue” Screen LSB Control	93h	00h	R/W
Noise Measurement LSB	94h		R
Noise Measurement MSB	95h		R
Weak Signal High Threshold	96h	60h	R/W
Weak Signal Low Threshold	97h	50h	R/W
Reserved	98h		
NR_Pix_Delay_Factor	99h	00h	R/W
NR_Line_Delay_Factor	9Ah	00h	R/W
NR_YNoise_Limit	9Bh	0Ah	R/W
NR_UNoise_Limit	9Ch	05h	R/W
NR_VNoise_Limit	9Dh	05h	R/W
NR_Y_T0	9Eh	0Ah	R/W
NR_U_T0	9Fh	BCh	R/W
NR_V_T0	A0h	BCh	R/W
NR_Status	A1h	0	R
Vertical Line Count Status	A2h - A3h		R
MidTone_Hi	A4h - A5H	0190h	R/W
MidTone_Lo	A6h - A7H	0078h	R/W
Output Formatter Control 1 (write to all 4 I2C pages)	A8h	44h	R/W
Output Formatter Control 2 (write to all 4 I2C pages)	A9h	40h	R/W
Output Formatter Control 3 (write to all 4 I2C pages)	AAh	03h	R/W
Reserved	ABh - ACh		
Sync Control (write to all 4 I2C pages)	ADh	00h	R/W
Embedded Sync Offset Control 1 (write to all 4 I2C pages)	AEh	00h	R/W
Embedded Sync Offset Control 2 (write to all 4 I2C pages)	AFh	00h	R/W
AVD output control 1	B0h	00h	R/W
AVD output control 2	B1h	10h	R/W
OFM mode control	B2h	00h	R/W
OFM channel select 1	B3h	E4h	R/W
OFM channel select 2	B4h	E4h	R/W
OFM channel select 3	B5h	00h	R/W
OFM super-frame size LSBs	B6h	1Bh	R/W
OFM super-frame size MSBs	B7h	04h	R/W
OFM h-blank duration LSBs	B8h	40h	R/W
OFM h-blank duration MSBs	B9h	00h	R/W
Misc OFM Control	BAh	00h	R/W
Reserved	BBh - BFh	00h	R/W
Audio sample rate control	C0h	00h	R/W
Analog audio gain control 1	C1h	88h	R/W
Analog audio gain control 2	C2h	88h	R/W
Audio Mode Control	C3h	C9h	R/W
Audio Mixer Select	C4h	01h	R/W
Audio Mute Control	C5h	00h	R/W
Audio mixing ratio control 1	C6h	00h	R/W
Audio mixing ratio control 2	C7h	00h	R/W
Audio Cascade Mode control	C8h	00h	R/W
Audio High Pass Filter Coefficient Byte One	C9h	A5h	R/W
Audio High Pass Filter Coefficient Byte Two	CAh	FFh	R/W
Audio High Pass Filter Coefficient Byte Three	CBh	7Eh	R/W

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REGISTER NAME	I2C SUBADDRESS	DEFAULT	R/W
Audio Test Control	CCh	01h	R/W
Reserved	CDh - CFh		
Reserved	D0h - DFh		
Reserved	F1h		
Interrupt Status 0	F2h		R
Reserved	F3h		
Interrupt Mask 0	F4h	00h	R/W
Reserved	F5h		
Interrupt Clear 0	F6h	00h	R/W
Reserved	F7h - FDh		
Decoder write enable	FEh	0Fh	R/W
Decoder read enable	FFh	01h	R/W

R = Read only

W = Write only

R/W = Read and write

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## 5. Electrical Specifications

### 5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)<sup>(1)</sup>

Supply voltage range: VDD_3_3 to VSS_3_3 .....	0.5V to +4.0V
VDD_1_1 to VSS_1_1 .....	-0.2V to +1.2V
VDDA_3_3 to VSSA_3_3 .....	-0.3V to +3.6V
VDDA_1_8 to VSSA_1_8 .....	-0.2V to +2.0V
VDDA_1_1 to VSSA_1_1 .....	-0.2V to +1.2V
Digital Input Voltage, V <sub>I</sub> to DGND .....	-0.5V to +4.5V
Digital Output Voltage, V <sub>O</sub> to DGND .....	-0.5V to +4.5V
Analog Input Voltage Range A <sub>IN</sub> to AGND .....	-0.2V to +2.0V
Operating Free-Air Temperature, T <sub>A</sub> : Commercial .....	0°C to +70°C
Industrial .....	-40°C to +85°C
Storage Temperature, T <sub>stg</sub> .....	-65°C to +150°C

- (1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.



## 5.2 Recommended Operating Conditions

VDD\_1\_1 = 1.0 to 1.2V, VDD\_3\_3 = 3.0V to 3.6V, VDDA\_1\_1 = 1.0 to 1.2V, VDDA\_1\_8 = 1.65 to 1.95V,  
 VDDA\_3\_3 = 3.0V to 3.6V

	PARAMETERS	TEST CONDITIONS	MIN	NOM	MAX	UNIT
VDD_3_3	Supply voltage, digital		3.13	3.3	3.6	V
VDD_1_1	Supply voltage, digital		1.0	1.1	1.2	V
VDDA_3_3	Supply voltage, analog		3.0	3.3	3.6	V
VDDA_1_8	Supply voltage, analog		1.65	1.8	1.95	V
VDDA_1_1	Supply voltage, analog		1.0	1.1	1.2	V
V <sub>I(PP)</sub>	Input voltage, analog (ac-coupling necessary)			1.2	1.4	V
V <sub>IH</sub>	Input voltage high, digital (1)		0.7• VDD_3_3			V
V <sub>IL</sub>	Input voltage low, digital (2)				0.3• VDD_3_3	V
I <sub>OH</sub>	Output current	Vout = 2.4V			TBD	mA
I <sub>OL</sub>	Output current	Vout = 0.4V			TBD	mA
	Video ADC conversion rate			27	30	MHz
	Audio ADC conversion rate			32.768	35	MHz
F <sub>s</sub>	Audio sampling frequency		8		16	kHz
T <sub>A</sub>	Operating free-air temperature - Commercial		0		70	°C
	Operating free-air temperature - Industrial		-40		85	°C

- (1) Exception: 0.7•VDDA\_1\_8 for XTAL\_IN terminal  
 (2) Exception: 0.3•VDDA\_1\_8 for XTAL\_IN terminal  
 (3) Currents out of a terminal are given as a negative number

### 5.2.1 Reference Clock Specifications

Reference Clock Specification	MIN	NOM	MAX	UNIT
Frequency		27		MHz
Frequency tolerance (1)	-50		+50	ppm

- (1) This number is the required specification for the external crystal/oscillator and is not tested.

## 5.3 Electrical Characteristics

For minimum/maximum values ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ): VDD\_1\_1 = 1.0 to 1.2V, VDD\_3\_3 = 3.0V to 3.6V, VDDA\_1\_1 = 1.0 to 1.2V, VDDA\_1\_8 = 1.65 to 1.95V, VDDA\_3\_3 = 3.0V to 3.6V

For typical values ( $T_A = 25^\circ\text{C}$ ): VDD\_1\_1 = 1.1V, VDD\_3\_3 = 3.3V, VDDA\_1\_1 = 1.1V, VDDA\_1\_8 = 1.8V, VDDA\_3\_3 = 3.3V

### 5.3.1 DC Electrical Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>DD(33D)</sub>	3.3-V I/O digital supply current			TBD		mA
I <sub>DD(11D)</sub>	1.1-V core digital supply current			TBD		mA
I <sub>DD(33A)</sub>	3.3-V analog supply current			TBD		mA
I <sub>DD(18A)</sub>	1.8-V analog supply current			TBD		mA
I <sub>DD(11A)</sub>	1.1-V analog supply current			TBD		mA
P <sub>TOT</sub>	Total power dissipation, normal operation			TBD		mW
P <sub>APWD</sub>	Power dissipation with audio powered down			TBD		mW
P <sub>DOWN</sub>	Total power dissipation with power down (Set I2C register 1Ah to 0xFFh)			TBD		mW
I <sub>Ikg</sub>	Input leakage current				10	μA
C <sub>I</sub>	Input capacitance	Specified by design			8	pF
V <sub>OH</sub>	Output voltage high	I <sub>OH</sub> = -4mA	0.8• VDD_3_3			V
V <sub>OL</sub>	Output voltage low	I <sub>OL</sub> = 4mA			0.2• VDD_3_3	V

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## 5.4 Analog Processing and A/D Converters

### 5.4.1 Video A/D Converters

ADC sample rate = 27MSPS (1) for video Ch 1, Ch 2, Ch 3, and Ch 4

	PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zi	Input impedance, analog video inputs	Specified by design (not tested)	200			kΩ
Ci	Input capacitance, analog video inputs	Specified by design (not tested)			10	pF
V <sub>i(PP)</sub>	Input voltage range	C <sub>coupling</sub> = 0.1 μF	1.35	1.4		V
G	Nominal analog video gain(2)			-2.9		dB
DNL	Absolute differential non-linearity (3)	AFE only		0.75	1.0	LSB
INL	Absolute integral non-linearity	AFE only		1	2.5	LSB
FR	Frequency response	Multiburst (60 IRE)		-0.9		dB
XTALK	Input crosstalk	Specified by design, 1 MHz			-50	dB
SNR	Signal-to-noise ratio (all channels)	Fin = 1 MHz, 1.0 Vpp		54		dB
NS	Noise spectrum	Luma ramp (100 kHz to full, tilt null)		-58		dB
DP	Differential phase	Modulated ramp		0.5		deg
DG	Differential gain	Modulated ramp		± 1.5		%

Notes:

- (1) Double-sampler uses both edges of clock (i.e. 54MHz).
- (2) Specified by design
- (3) No missing codes, guaranteed.

## 5.4.2 Audio A/D Converters

ADC sample rate = 32.768MSPS for audio Ch 1, Ch 2, Ch 3, and Ch 4

	PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_i$	Input impedance, analog audio inputs	Specified by design, at 0-dB PGA gain	20			k $\Omega$
$C_i$	Input capacitance, analog audio inputs	Specified by design			10	pF
$V_{i(PP)}$	Input voltage range	$C_{coupling} = 2.2 \mu F$ , at 0-dB PGA gain		1.414		V <sub>pp</sub>
DNL	Absolute differential non-linearity (1)	AFE only		0.75	1.0	LSB
INL	Absolute integral non-linearity	AFE only		1	2.5	LSB
XTALK	Crosstalk between any two channels			TBD		dB
SNR	Signal-to-noise ratio (all channels)	$f_s = 16 \text{ kHz}$ , $V_{in} = -60 \text{ dB}$ , 1kHz		TBD		dB
THD+N	Total harmonic distortion + noise	$f_s = 16 \text{ kHz}$ , $V_{in} = -1 \text{ dB}$ , 1kHz		60		dB
DR	Dynamic range	$f_s = 16 \text{ kHz}$ , $V_{in} = -60 \text{ dB}$ , 1kHz		TBD		dB
	System clock frequency per channel			512•fs		Hz

Notes:

(1) No missing codes, guaranteed.

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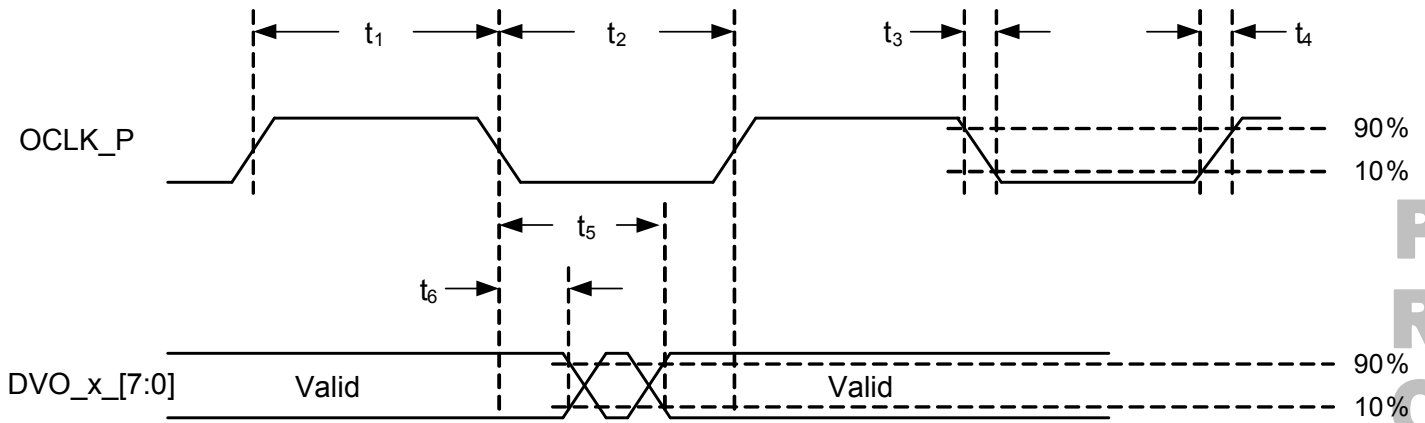
## 5.5 Timing

### 5.5.1 Video Output Clock and Data Timing

PARAMETER	TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
Duty cycle OCLK_P/OCLK_N		44	50	55	%
$t_1$ High time, OCLK_P/OCLK_N @ 13.5 MHz	$\geq 50\%$		37		ns
$t_1$ High time, OCLK_P/OCLK_N @ 27 MHz	$\geq 50\%$		18.5		
$t_1$ High time, OCLK_P/OCLK_N @ 54 MHz	$\geq 50\%$		9.25		
$t_1$ High time, OCLK_P/OCLK_N @ 81 MHz	$\geq 50\%$		6.17		
$t_1$ High time, OCLK_P/OCLK_N @ 108 MHz	$\geq 50\%$		4.63		
$t_2$ Low time, OCLK_P/OCLK_N @ 13.5 MHz	$\leq 50\%$		37		ns
$t_2$ Low time, OCLK_P/OCLK_N @ 27 MHz	$\leq 50\%$		18.5		
$t_2$ Low time, OCLK_P/OCLK_N @ 54 MHz	$\leq 50\%$		9.25		
$t_2$ Low time, OCLK_P/OCLK_N @ 81 MHz	$\leq 50\%$		6.17		
$t_2$ Low time, OCLK_P/OCLK_N @ 108 MHz	$\leq 50\%$		4.63		
$t_3$ Fall time, OCLK_P/OCLK_N	90% to 10%			1.08	ns
$t_4$ Rise time, OCLK_P/OCLK_N	10% to 90%			1.08	ns
$t_5$ Data valid time (propagation delay)	To 90%/10%			TBD(1)	ns
$t_6$ Data hold time	To 90%/10%	2.5			ns

(1) Measured with a load of 10pF for up 81MHz and 6pF for 108MHz. Specified by design.

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**Figure 5-1. Video Output Clock and Data Timing**

### 5.5.2 Video Input Clock and Data Timing

PARAMETER	TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
Duty cycle CLK_IN		44	50	55	%
$t_1$ Data setup time (video ports C and D)	To 90%/10%	TBD			ns
$t_2$ Data hold time (video ports C and D)	To 90%/10%	TBD			ns
$t_3$ Fall time, CLK_IN (pin 50)	90% to 10%			4.32	ns
$t_4$ Rise time, CLK_IN (pin 50)	10% to 90%			4.32	ns

(1) 8-Ch video cascade mode.

### 5.5.3 I<sup>2</sup>C Host Port Timing

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>1</sub> Bus free time between STOP and START		1.3			μs
t <sub>2</sub> Data Hold time		0		0.9	μs
t <sub>3</sub> Data Set up time		100			μs
t <sub>4</sub> Set up time for a (repeated) START condition		0.6			μs
t <sub>5</sub> Set up time for a STOP condition		0.6			ns
t <sub>6</sub> Hold time (repeated) START condition		0.6			μs
t <sub>7</sub> Rise time SDA and SCL signal	Specified by design			250	ns
t <sub>8</sub> Fall time SDA and SCL signal	Specified by design			250	ns
C <sub>b</sub> Capacitive load for each bus line	Specified by design			400	pF
f <sub>I2C</sub> I <sup>2</sup> C clock frequency (1)				400	kHz

Notes:

(1) All fast-mode (400kHz) I<sup>2</sup>C timing requirements are specified by design.

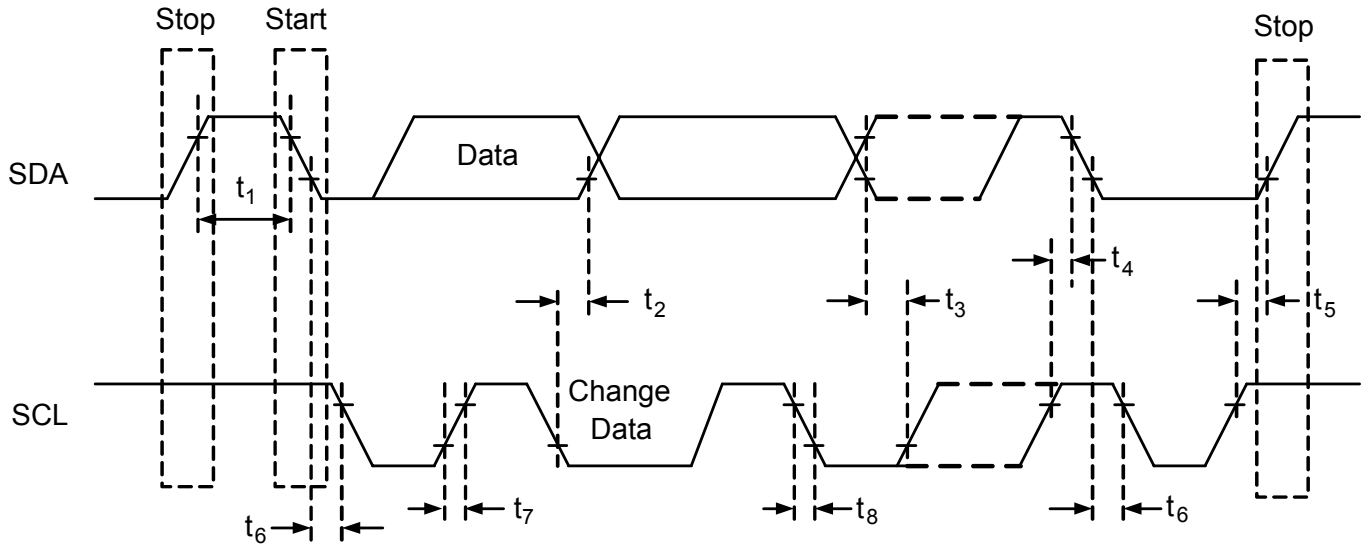


Figure 5-2. I<sup>2</sup>C Host Port Timing

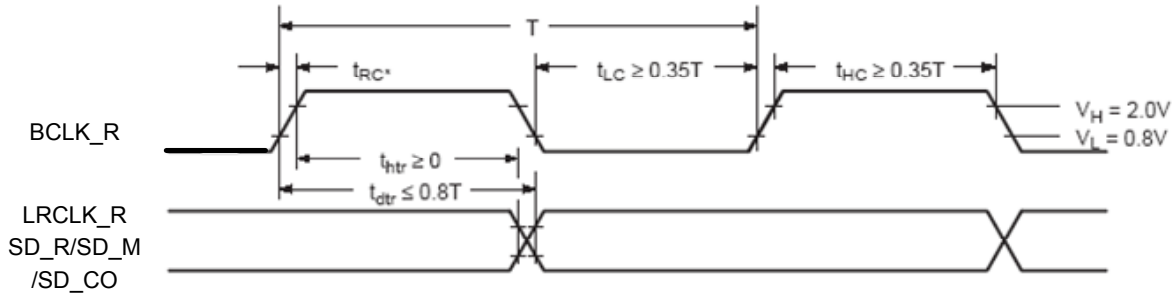
### 5.5.4 I<sup>2</sup>S Port Timings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
T <sub>tr</sub>	BCLK_R Clock Period (TX)	C <sub>L</sub> = 10pF	1.0			T <sub>tr</sub>	1,2
T <sub>HC</sub>	BCLK_R Clock HIGH Time	C <sub>L</sub> = 10pF	0.35			T <sub>tr</sub>	1,2
T <sub>LC</sub>	BCLK_R Clock LOW Time	C <sub>L</sub> = 10pF	0.35			T <sub>tr</sub>	1,2
T <sub>dtr</sub>	BCLK_R to SD_R and LRCLK_R	C <sub>L</sub> = 10pF			0.8	T <sub>tr</sub>	1,2
T <sub>htr</sub>	Hold Time BCLK_R to SD_R and LRCLK_R	C <sub>L</sub> = 10pF	0				1,2
T <sub>SCKDUTY</sub>	BCLK_R Duty Cycle	C <sub>L</sub> = 10pF	40%		60%	T <sub>tr</sub>	1,2
T <sub>SCK2SD</sub>	BCLK_R -to-SD_R Delay	C <sub>L</sub> = 10pF	-5		+5	ns	1,3
T <sub>AUDDLY</sub>	Audio Pipeline Delay			TBD	TBD	μs	1,4

**Notes:**

- (1) Specified by design.
- (2) Meets timings in Philips I<sup>2</sup>S specification.
- (3) Applies also to SD\_R -to-LRCLK\_R delay.



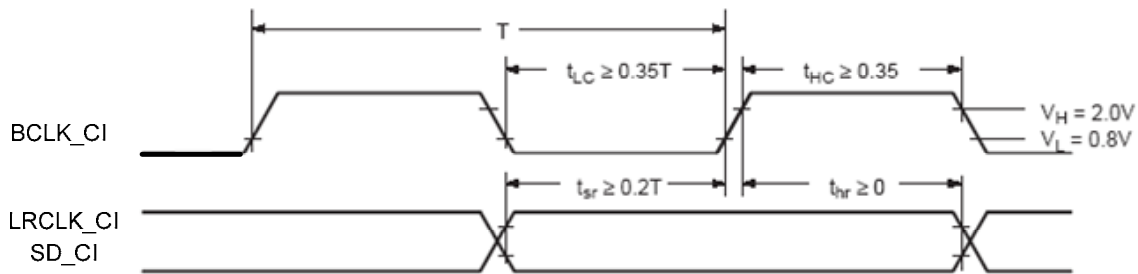


T = Clock Period

$T_{tr}$  = Minimum allowed clock period for transmitter

$T > T_{tr}$

\*  $t_{RC}$  is only relevant for transmitters in slave mode



T = Clock Period

$T_r$  = Minimum allowed clock period for transmitter

$T > T_r$

**Figure 5-3. I<sup>2</sup>S Port Timings**

### 5.5.5 Miscellaneous Timings

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
$T_{RESET}$	RESETB Signal Low Time for valid reset		200			ns	

## 6. Typical Applications

### 6.1 4-CH D1 Applications

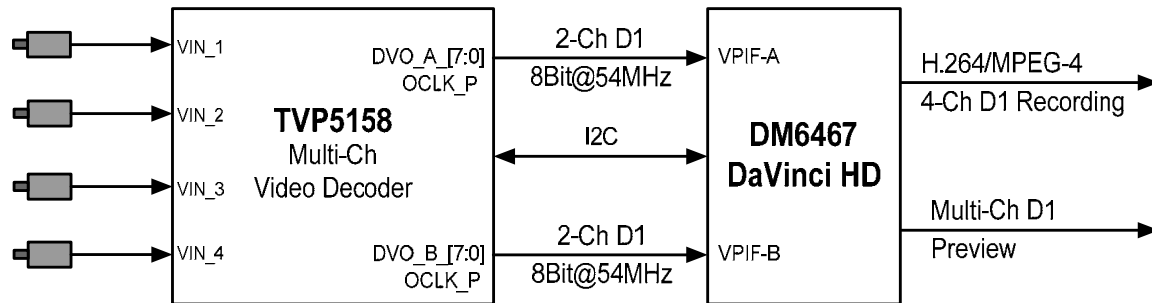


Figure 6-1. 4-CH D1 Application (Dual BT.656 I/F)

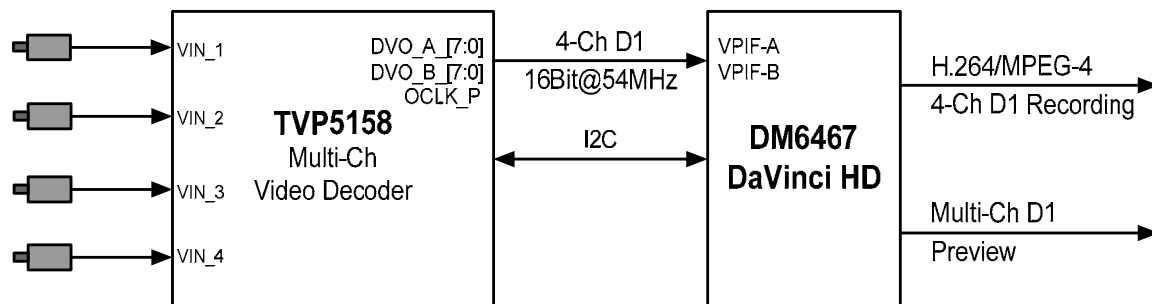
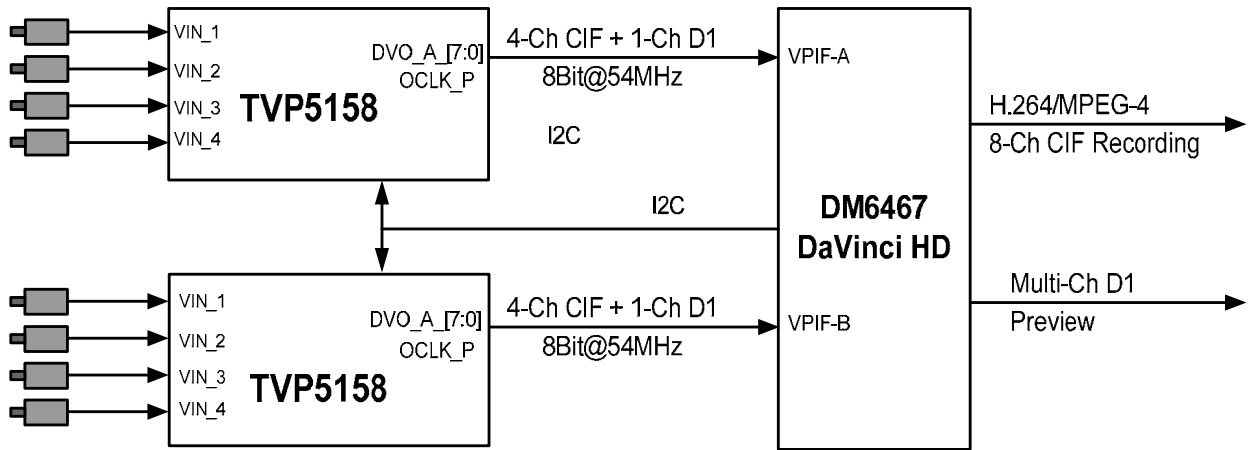
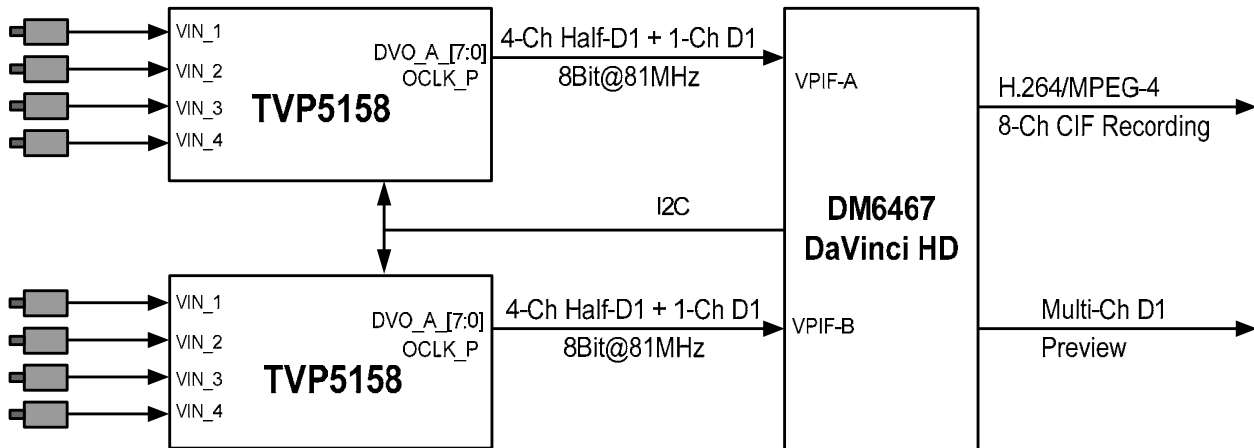


Figure 6-2. 4-CH D1 Application (16-Bit YUV 4:2:2 I/F)

## 6.2 8-CH CIF Applications



**Figure 6-3. 8-CH CIF Real Time Encoding and Multi-Ch D1 Preview Application**



**Figure 6-4. 8-CH CIF Real Time Encoding and Multi-Ch D1 Preview Application**

(The backend DSP drops one field of Half-D1 to get CIF format video)

## 6.3 16-CH CIF Applications

See section “3.8.3.3 Video Cascade mode” for the details of 16-CH CIF applications.

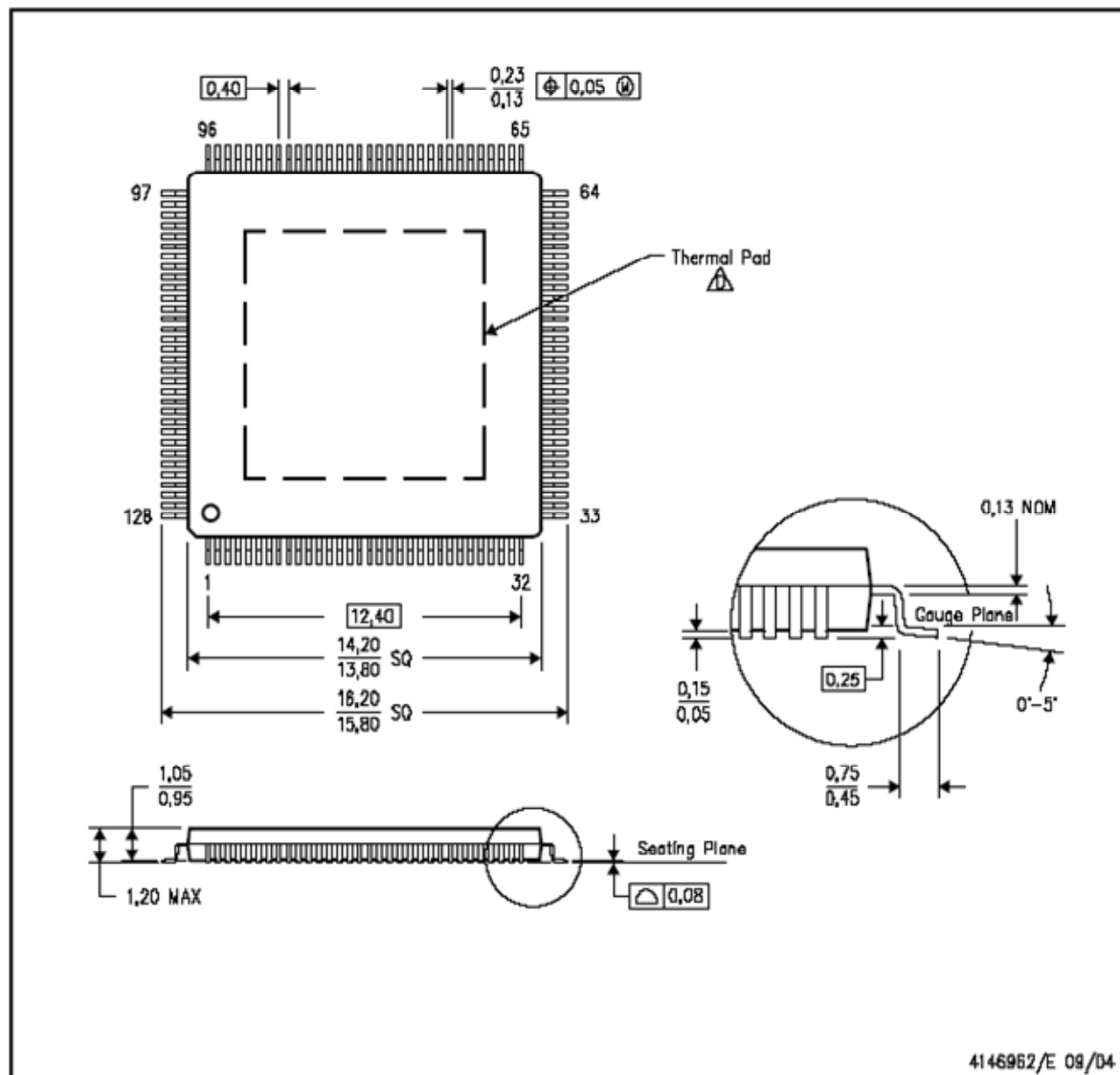
## 6.4 Application Circuit Example (TBD)

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## 7. Mechanical Data

PNP (S-PQFP-G128)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. See the product data sheet for details regarding the exposed thermal pad dimensions.

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