3.4.1 **SOC AIF2 connections**

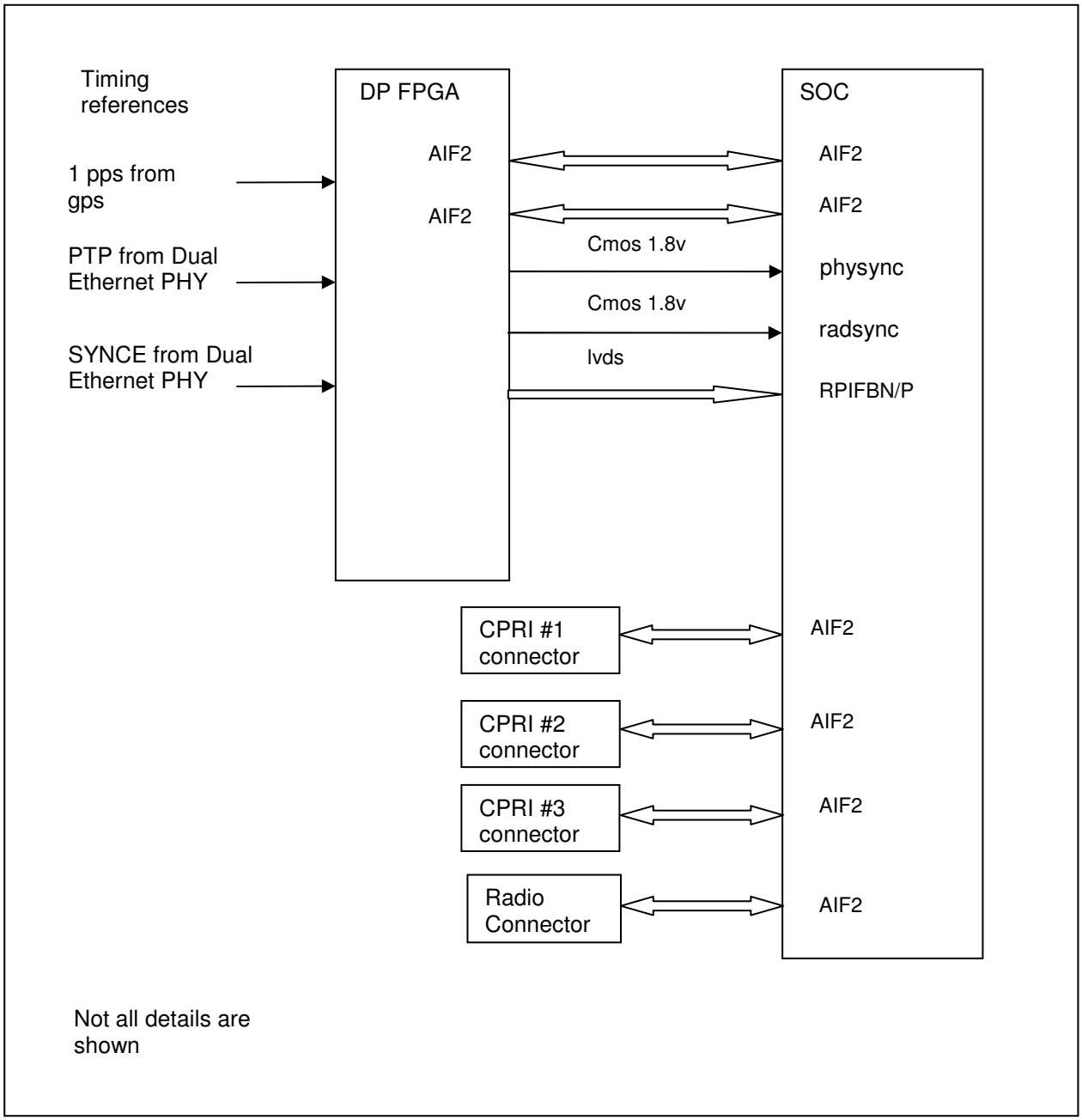

Figure 16 Digital Board – AIF2 connections

The AIF2 interfaces are used to connect the SOC to various elements in the design. The DP fpga is the timing reference to the SOC and sources the PHYSYNC, RADSYNC and RP1FBN/P signals to the SOC.