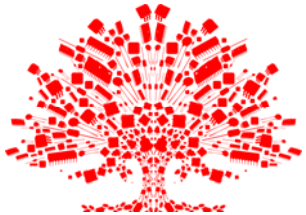

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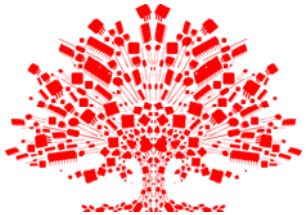
Inter-DM6467 Communications Using Direct GMII Connections

RandyP
SMTS FAE

Texas Instruments



Inter-DM6467 Communications

- **Hardware implementation**
  - **DM6467 EMAC**
  - **GMII direct connection for point-to-point network**
  - **Hardware issues**
- **Software implementation**
- **Performance**

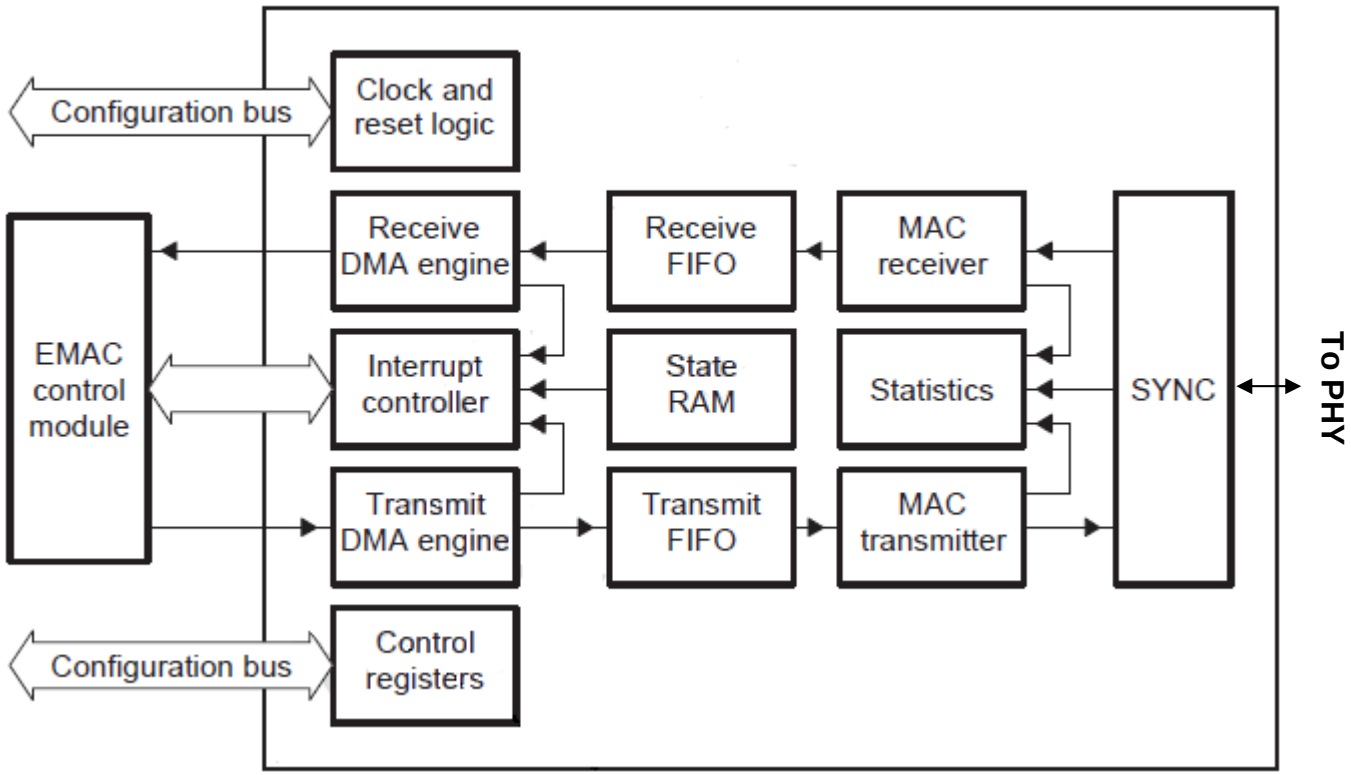
Inter-DM6467 Communications

- Hardware implementation
  - DM6467 EMAC
    - GMII direct connection for point-to-point network
    - Hardware issues
- Software implementation
- Performance

Ethernet Media Access Control

- Autonomous from CPU
- Monitors Ethernet for receive mac addresses
- Formats and transmits data

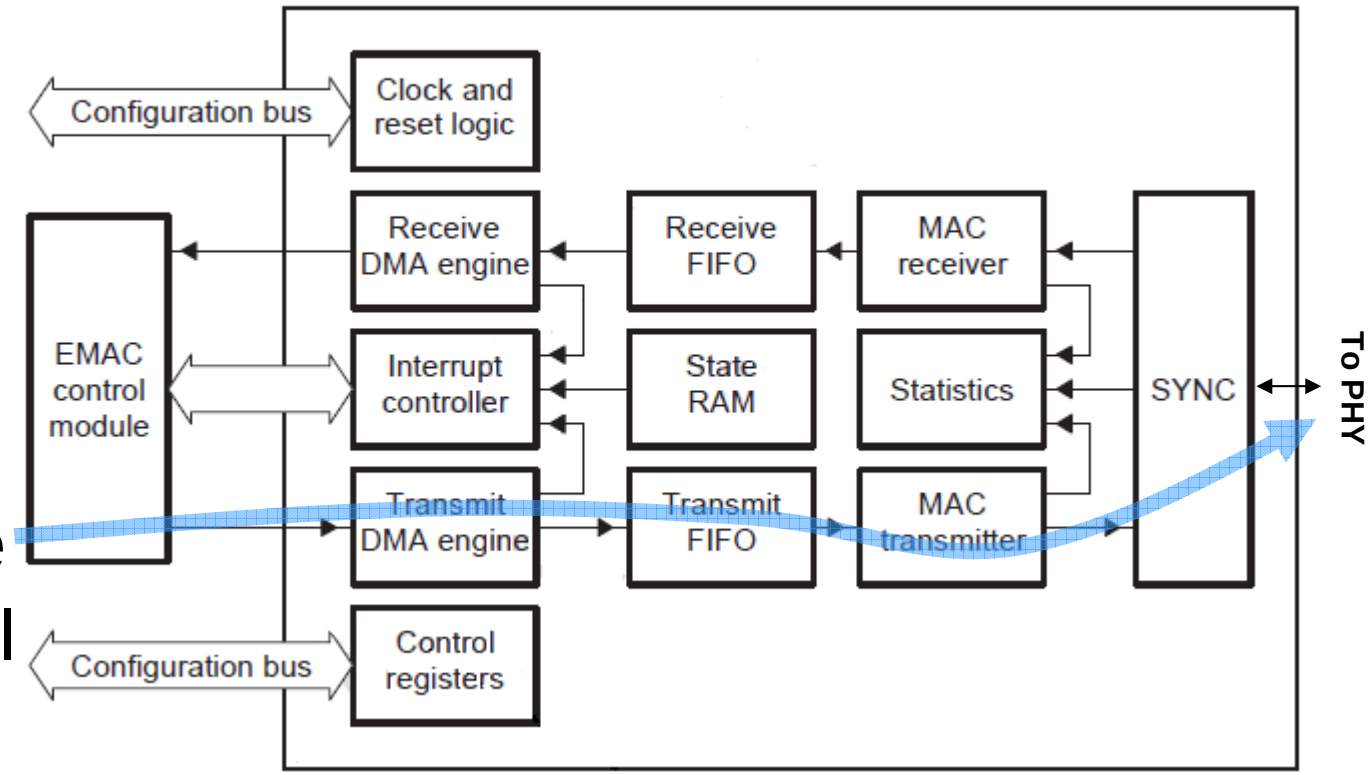
Figure 11. EMAC Module Block Diagram



Ethernet Media Access Control

- DMAs from memory to FIFO
- Builds Ethernet frame
- Sends frame thru MII/GMII to PHY

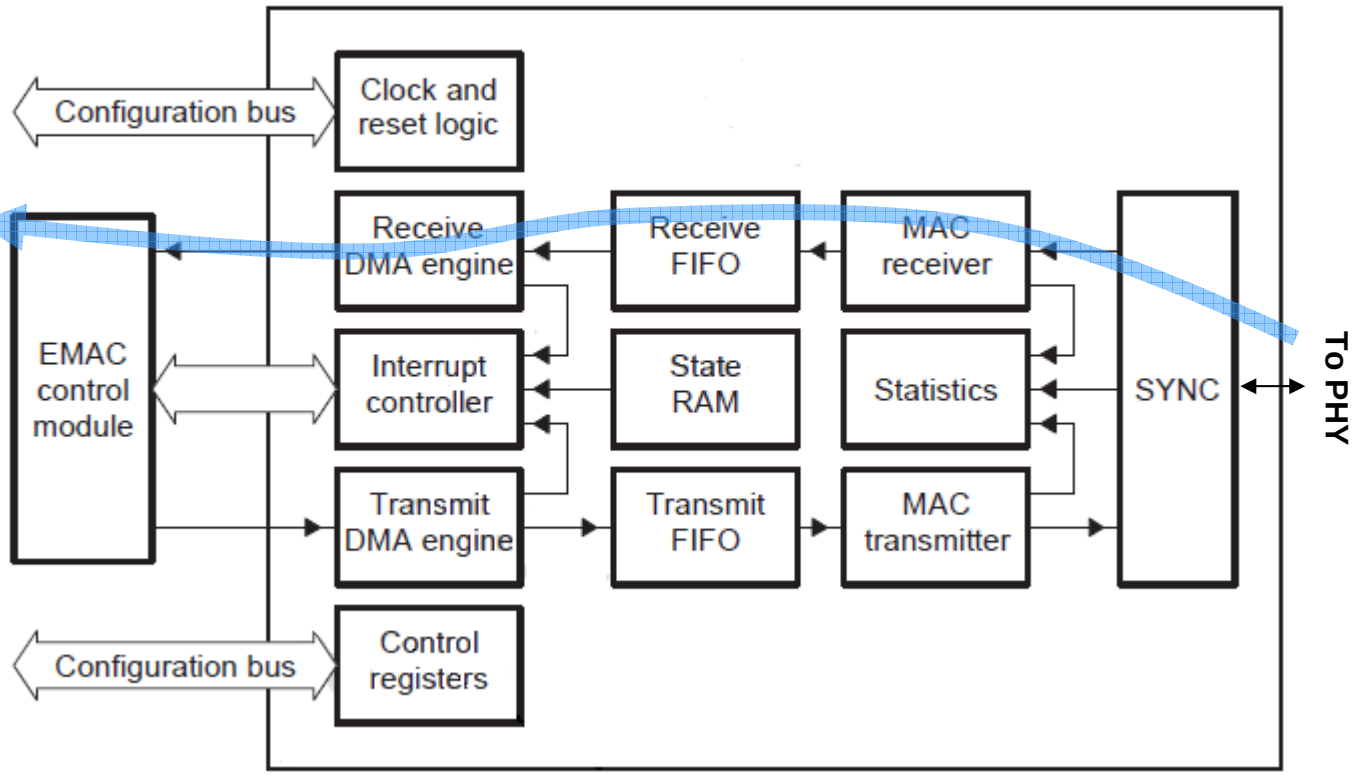
Figure 11. EMAC Module Block Diagram



Ethernet Media Access Control

- Looks for MAC addr match, picks rcvr channel
- Finds BD for this channel
- DMAs from FIFO to DDR

Figure 11. EMAC Module Block Diagram



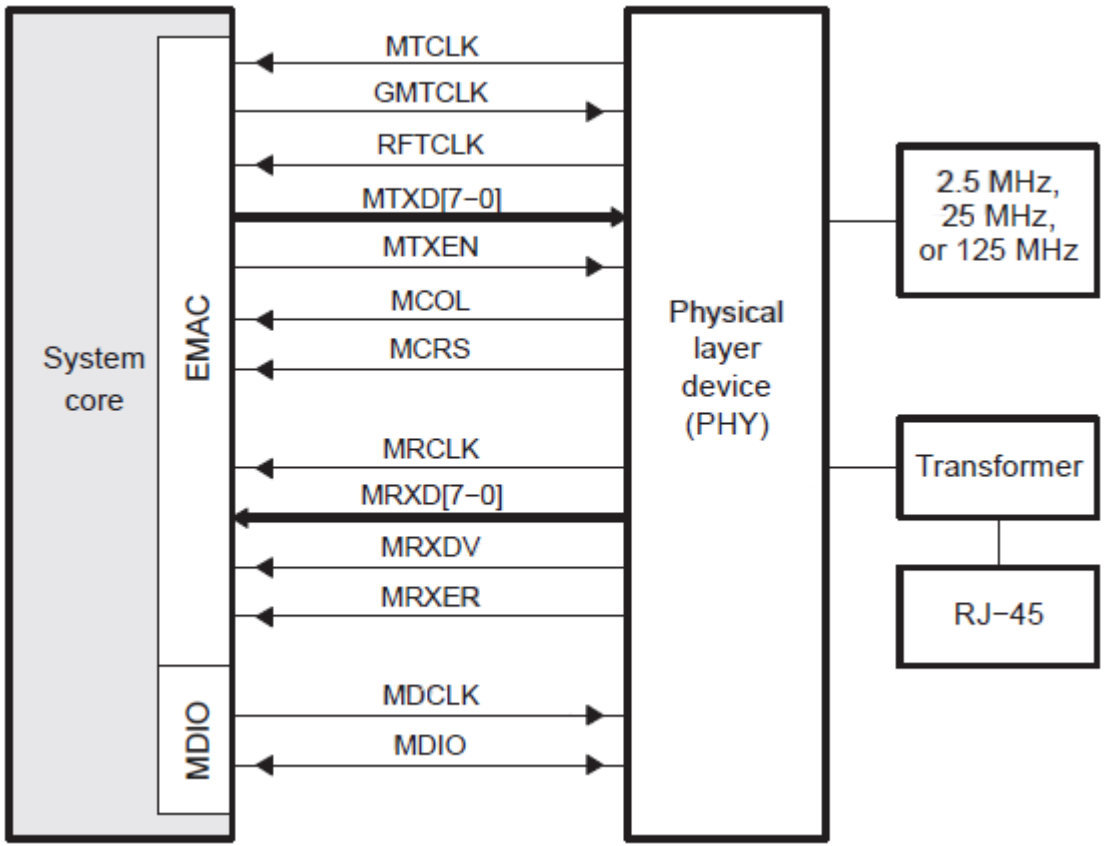
DM6467 EMAC DMA is limited

Table 6-55. EMAC DMA Master Memory Map

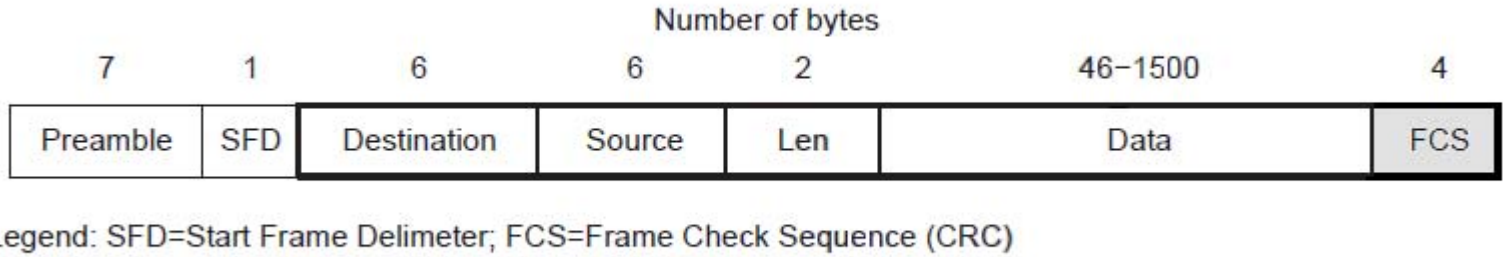
START ADDRESS	END ADDRESS	SIZE (BYTES)	EMAC DMA ACCESS
0x0000 0000	0x3FFF FFFF	1G	Reserved
0x4000 0000	0x4BFF FFFF	192M	Reserved
0x4C00 0000	0x4FFF FFFF	64M	VLYNQ (Remote Data)
0x5000 0000	0x7FFF FFFF	768M	Reserved
0x8000 0000	0x8FFF FFFF	256M	DDR2 Memory Controller
0x9000 0000	0x9FFF FFFF	256M	Reserved
0xA000 0000	0xBFFF FFFF	512M	Reserved
0xC000 0000	0xFFFF FFFF	1G	Reserved

- Limited to VLYNQ and DDR2 memory spaces
- Cannot access CFG space or ARM/DSP local SRAM

GMII Connections to PHY



Ethernet Frame



Legend: SFD=Start Frame Delimeter; FCS=Frame Check Sequence (CRC)

- EMAC adds fields to data buffer for transmit
  - Dest/src MAC addresses, length included in data
  - Preamble/SFD added
  - CRC/FCS can be generated automatically
- EMAC extracts data for receive
  - Matches Dest address for this device & channel
  - CRC/FCS can be removed or forwarded

Buffer Descriptor

Word Offset	Bit Fields 31 — 16	15 — 0
0	Next Descriptor Pointer	
1	Buffer Pointer	
2	Buffer Offset	Buffer Length
3	Flags	Packet Length

- Pointer to next Buffer Descriptor builds a singly-linked list
- Pointer to memory buffer for transmit or receive
- Offset is usually 0
- Length of this buffer
- Length of the whole packet
- Start, end, other flags

Flags:

Transmit:

31	30	29	28	27	26	25 — 16
SOP	EOP	OWNER	EOQ	TDOWNCMPLT	PASSCRC	Reserved

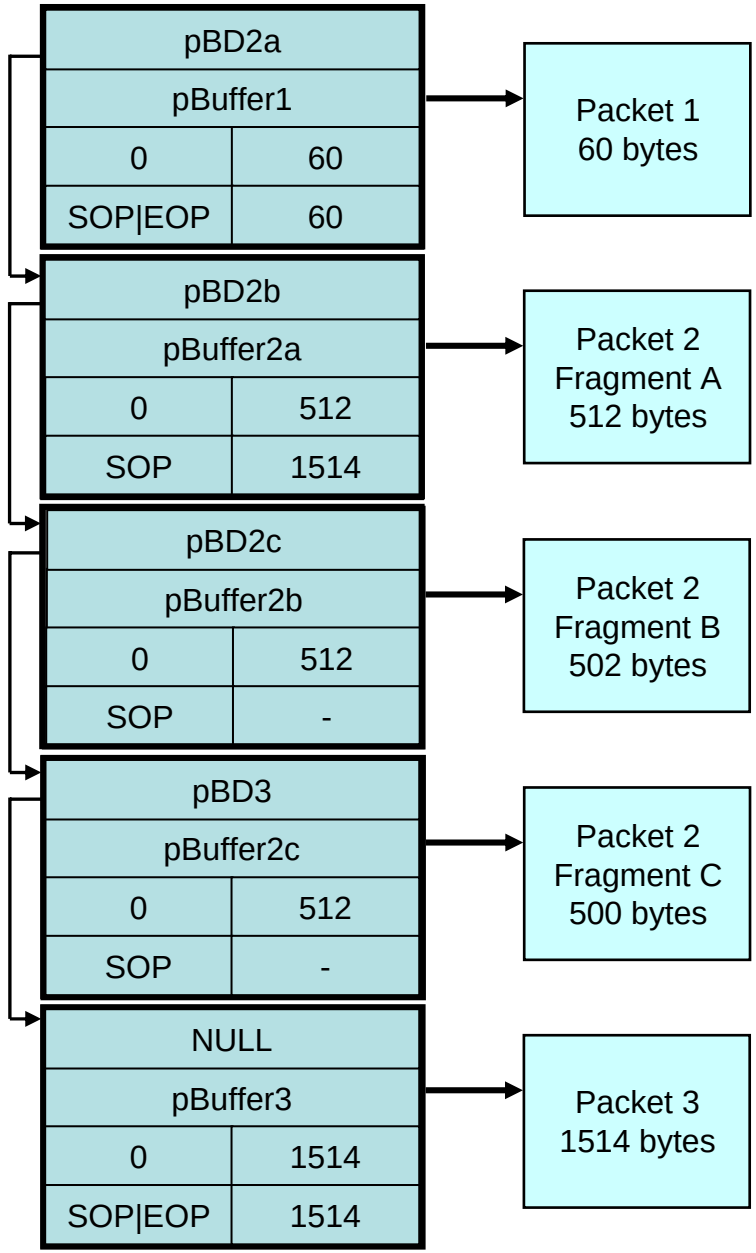
Receive:

31	30	29	28	27	26	25	24
SOP	EOP	OWNER	EOQ	TDOWNCMPLT	PASSCRC	JABBER	OVERSIZE

23	22	21	20	19	18	17	16
FRAGMENT	UNDERSIZED	CONTROL	OVERRUN	CODEERROR	ALIGNERROR	CRCERROR	NOMATCH

BD Linked List

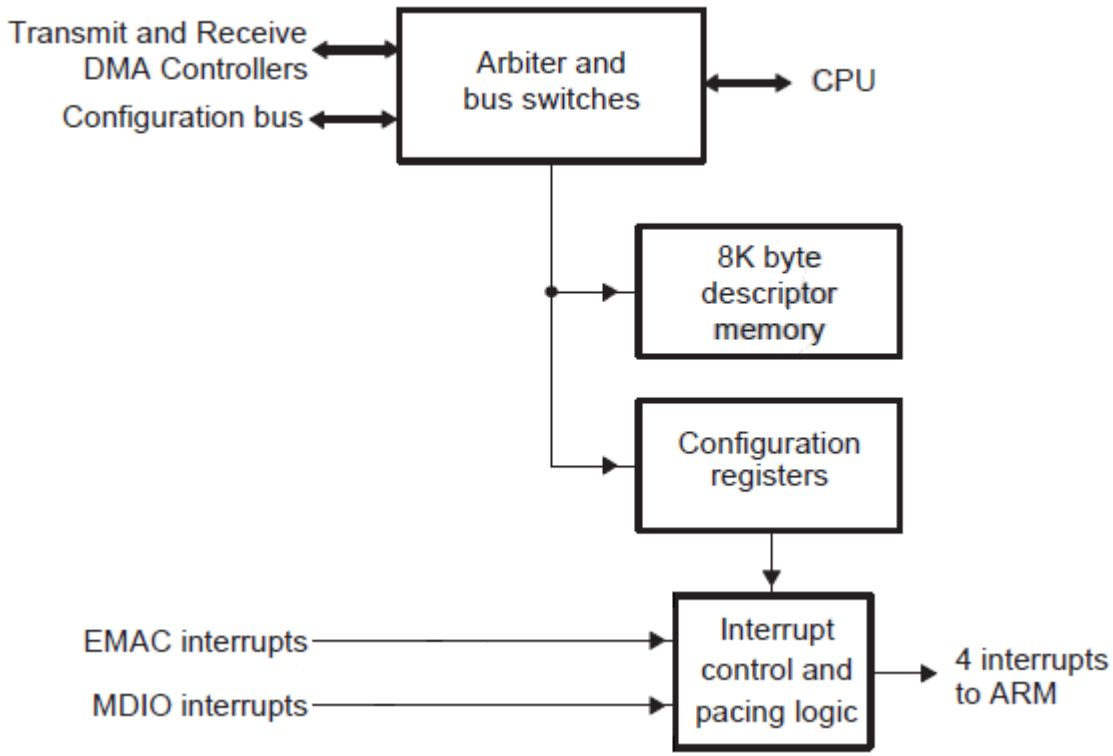
- Create all 3 packets
- Create all 5 Buf Descs
  1. 1 fragment of 60 bytes
  2. 3 fragments total 1514 bytes
  3. 1 fragment of 1514 bytes
- Once started, all 5 BDs will get used in order without further CPU interaction



EMAC Control Module

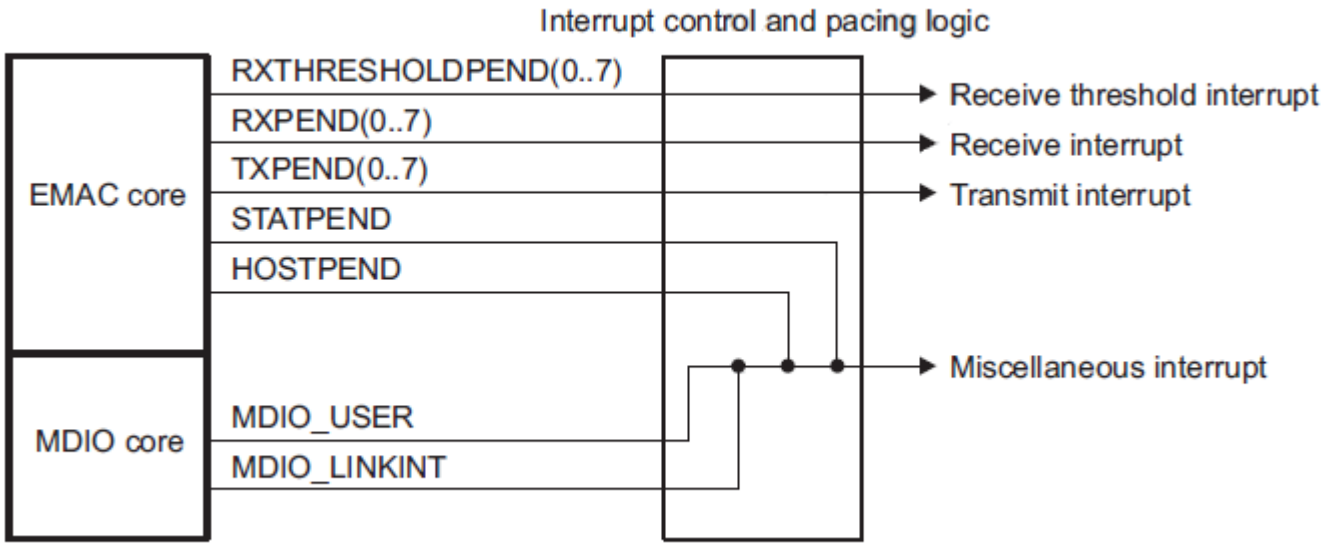
- System-level control functions
- DMA activity and arbitration
- Buffer Descriptor (BD) memory
- Interrupt muxing and status

Figure 9. EMAC Control Module Block Diagram



EMAC Interrupts

Figure 12. EMAC Control Module Interrupt Logic Diagram

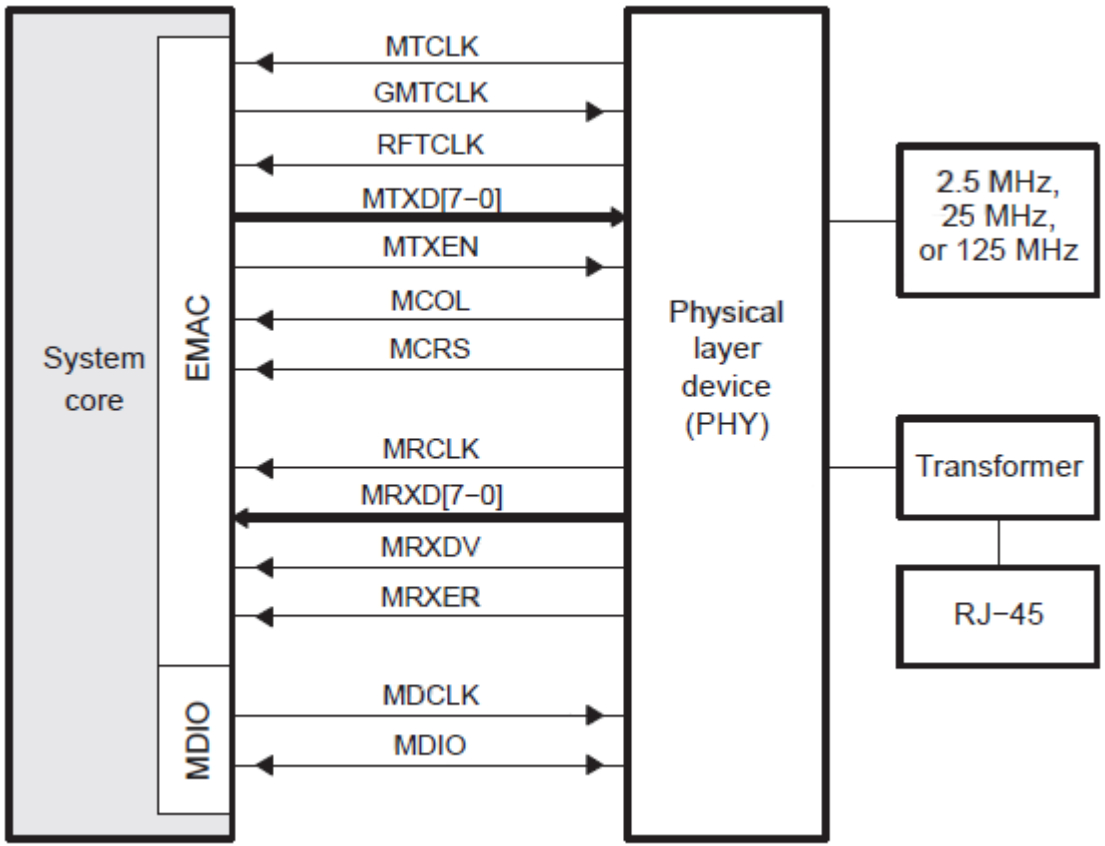


- All interrupts for all 8 channels combined into 4
- Pacing limits how often CPU gets interrupted
  - Fewer context switches
  - Potential for longer latency

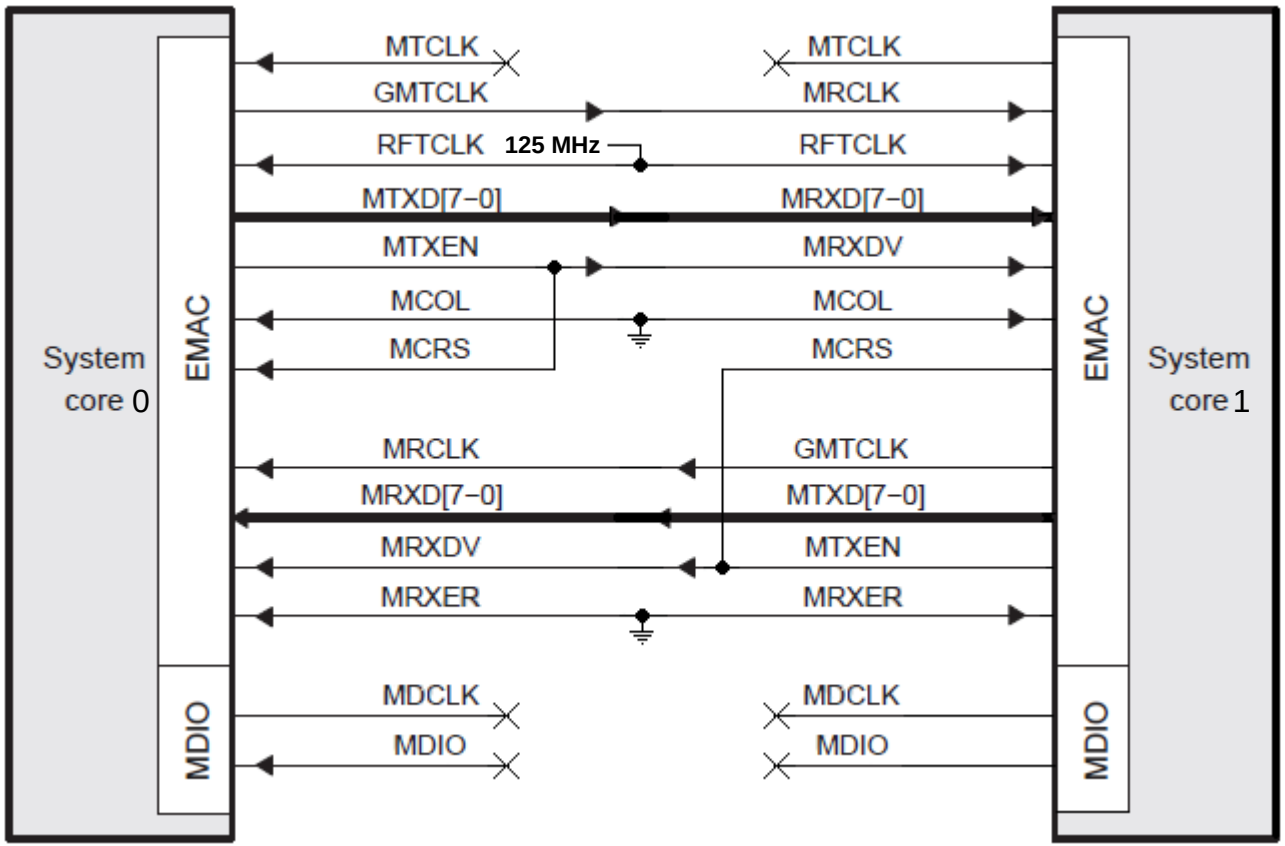
Inter-DM6467 Communications

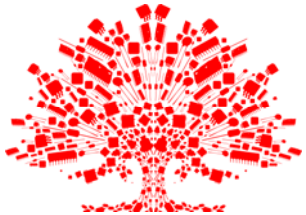
- Hardware implementation
  - DM6467 EMAC
  - GMII direct connection for point-to-point network
  - Hardware issues
- Software implementation
- Performance

GMII Connections to PHY



GMII-to-GMII Connections



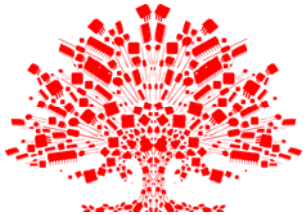


Inter-DM6467 Communications

- Hardware implementation
  - DM6467 EMAC
  - GMII direct connection for point-to-point network
  - Hardware issues
- Software implementation
- Performance

Hardware issues

- Power to the pins
  - Power ON both MII and GMII in VDD3P3V_PWDN
    - ON = clear bits to 0
    - On SVP, we do this in GEL in OnTargetConnect
    - *VDD3P3V_PWDN = 0x180000c0;
    - All on except USB, CLKOUT, and UART1
- Enable the EMAC module clocks in LPSC
  - Enable in Local Power and Sleep Controller (LPSC)
    - On SVP, we do this in GEL in OnTargetConnect
    - All modules enabled



Inter-DM6467 Communications

- Hardware implementation
- Software implementation
  - Initialize GMII
  - Send a packet
  - Receive a packet
- Performance

Inter-DM6467 Communications

- Hardware implementation
- Software implementation
  - Initialize GMII
  - Send a packet
  - Receive a packet
- Performance

Initialization

- There are a TON of registers
  - EMAC Control Module
  - EMAC Module
  - MDIO Module
- EMAC User's Guide has step-by-step procedures

Initialization

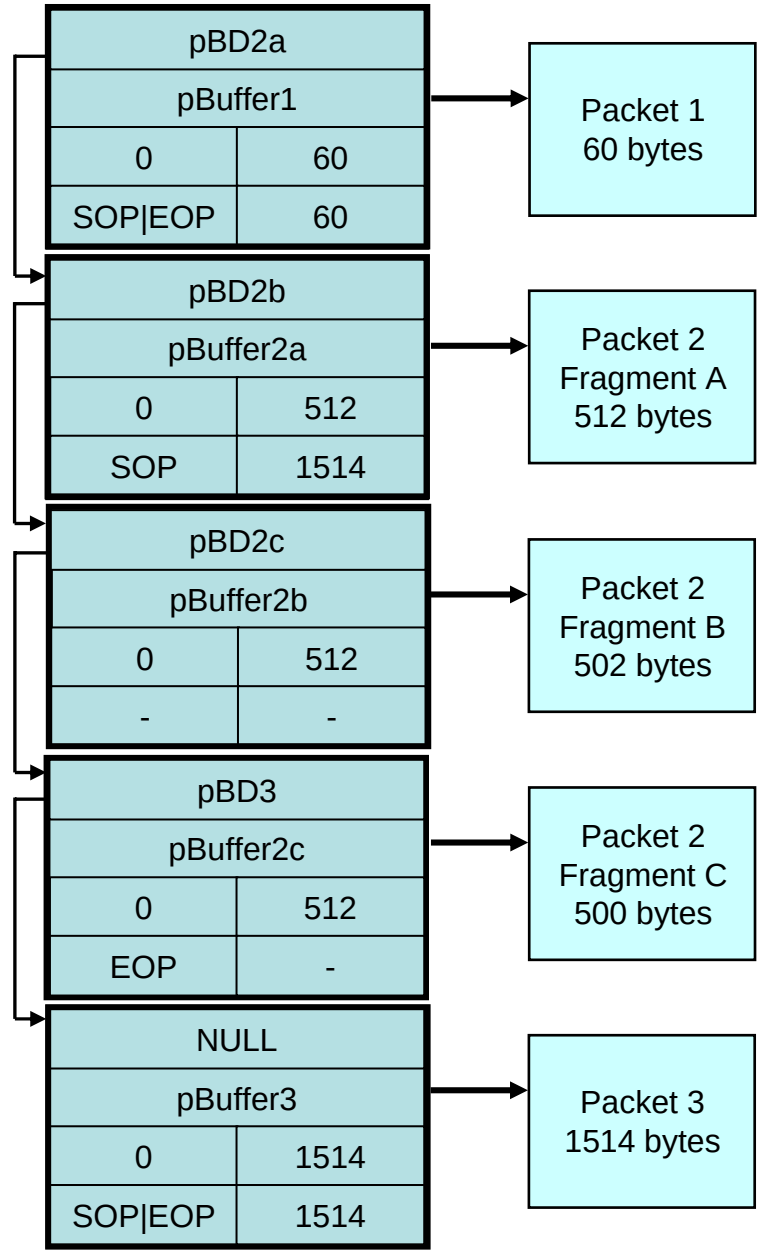
- ARM9 interrupts and hooks to EMAC ISRs
- 8 Receive channels
  - MAC address for each
  - Buffer Descriptor list for each
  - When you connect BD list to channel, it starts listening for MAC address match
- 8 Transmit channels
  - Buffer Descriptor list for each
  - When you connect BD list to channel, it starts transmitting

Inter-DM6467 Communications

- Hardware implementation
- Software implementation
  - Initialize GMII
  - Send a packet
  - Receive a packet
- Performance

Transmit BD list

- Data to send is in DDR
- Create all needed BDs
  - If space (512 total BDs)
  - Break large bufs into smaller
  - 60 bytes minimum size
  - 1514 bytes maximum size
- Write list head to TXnHDP
  - Starts transmitting after write
- All BDs go in order without further CPU interaction
  - Can get interrupts as needed

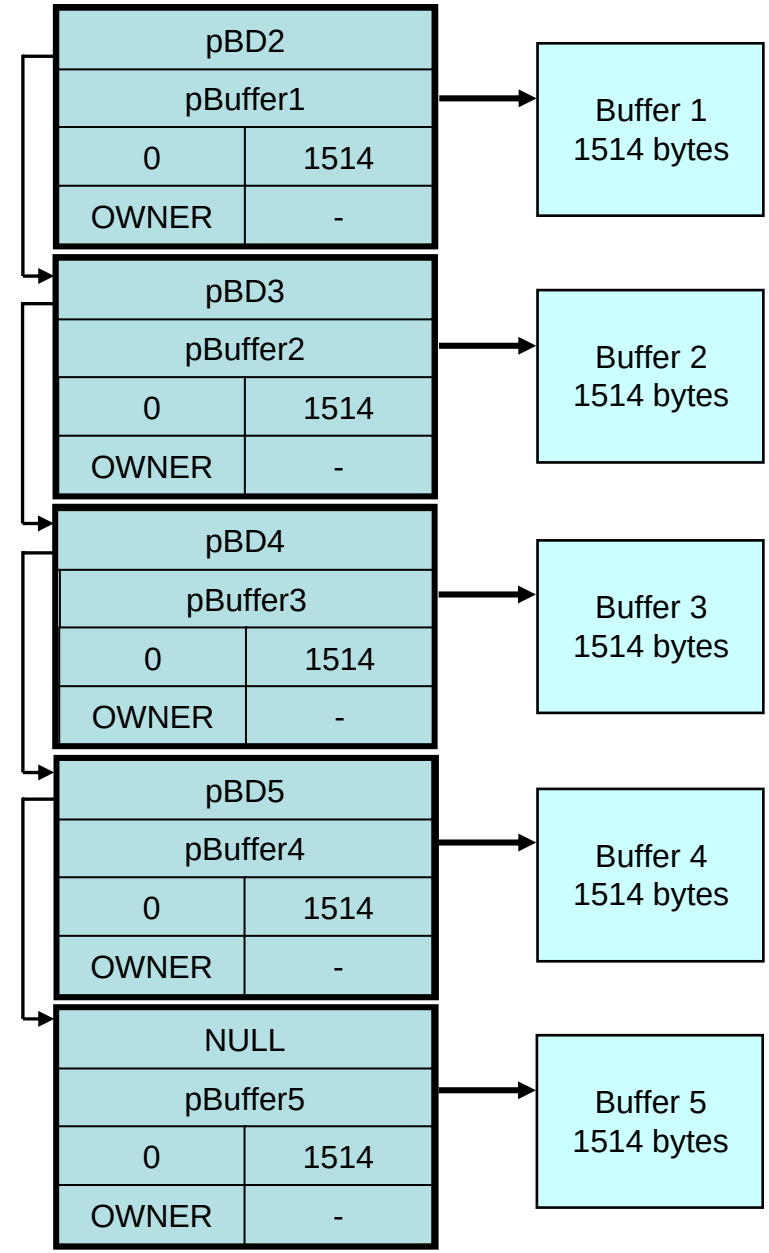


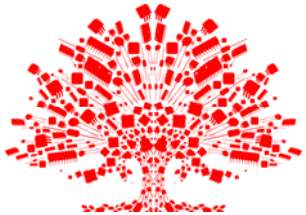
Inter-DM6467 Communications

- Hardware implementation
- Software implementation
  - Initialize GMII
  - Send a packet
  - Receive a packet
- Performance

Receive BD List

- Locate buffers in DDR
  - Should be 1514 B at least
  - Allow for any size packet
- Build list of BDs
  - Point to the buffers
  - Include size in BD
- Write list head to RXnHDP
  - Starts listening after write
- All BDs fill in order without further CPU interaction
  - Can get interrupts as needed





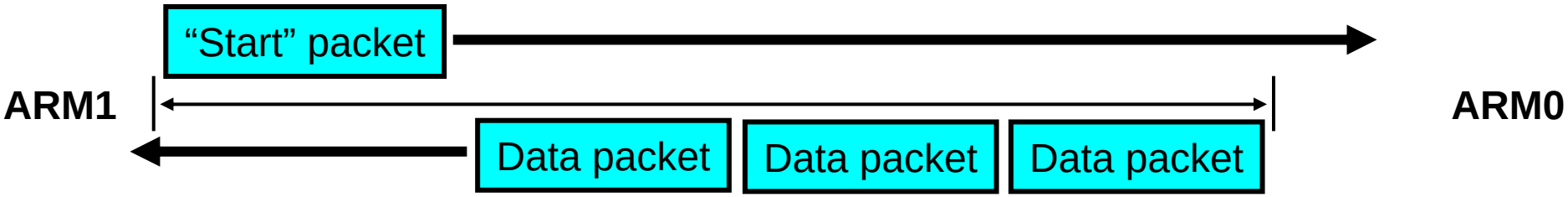
Inter-DM6467 Communications

- Hardware implementation
- Software implementation
- Performance

Loopback

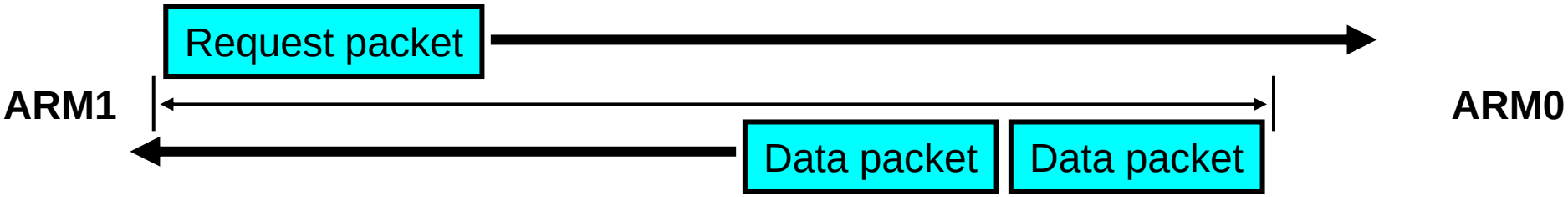
- Internal test mode
- Maximum ideal performance
- Easy to measure transmit-to-receive delay
  - All on one chip
- Measured 90% efficiency only measuring data
  - Packet overhead comes out of 10%
  - EMAC overhead comes out of 10%
  - Ideal maximum performance
- That's 900 Mbps

Packet Handshaking



- ARM-1 sends "Start" packet to ARM-0
- ARM-0 starts sending "real data" back to ARM-1
- ARM-1 measures from "Start" to "end"
  - Includes overhead of sending "Start" packet
  - Includes overhead of ARM-1 ISR
  - Divide received data by "Start" to "end"
  - 224 Mbps effective transfer rate for 15KB total rcv data
  - Will improve with larger total data transfered

Packet Request



- ARM-1 sends req packet with source addr, length
- ARM-0 builds BD list and starts sending data back
- ARM-1 measures from “Request” to “end”
  - Includes overhead of sending “Request” packet
  - Includes overhead of ARM-1 ISR
  - Includes overhead of ARM-1 BD list construction
- Implements a handy SRIO DirectIO scheme