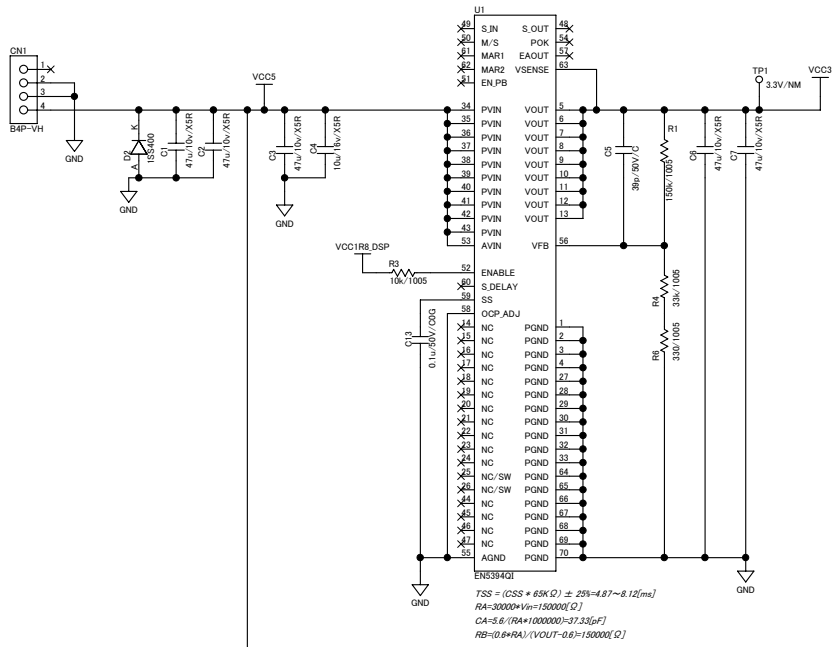
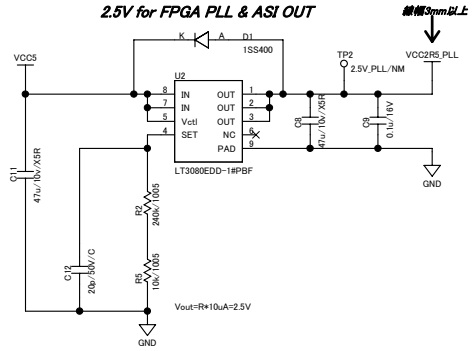
POWER1

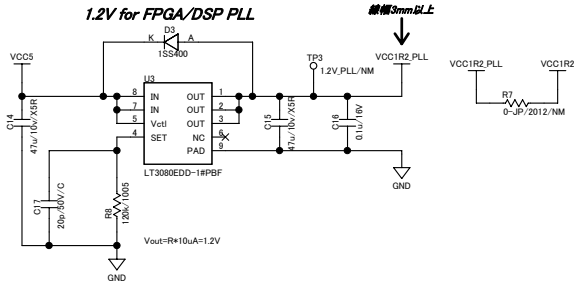
3.3V for ALL DEVICE



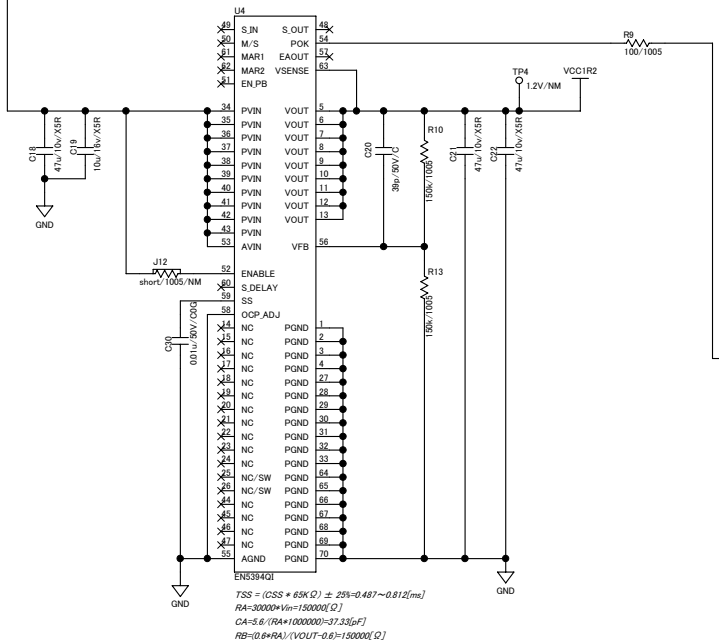
2.5V for FPGA PLL & ASI OUT



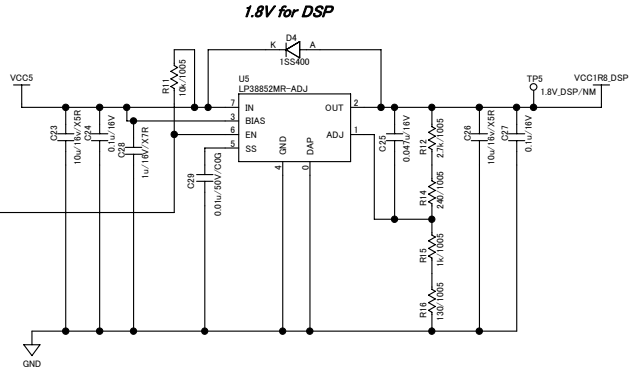
1.2V for FPGA/DSP PLL



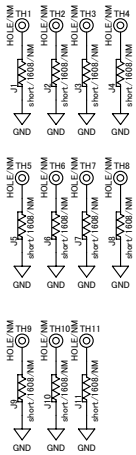
1.2V for FPGA DSP



1.8V for DSP



Mounting Holes



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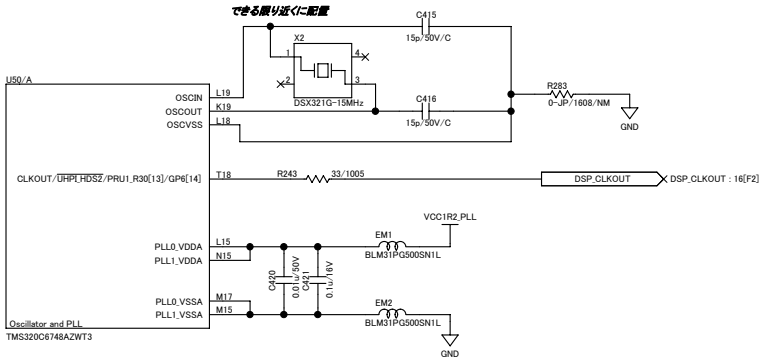

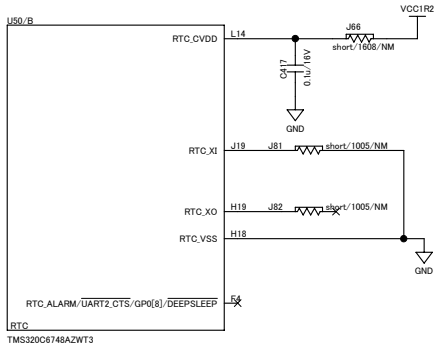

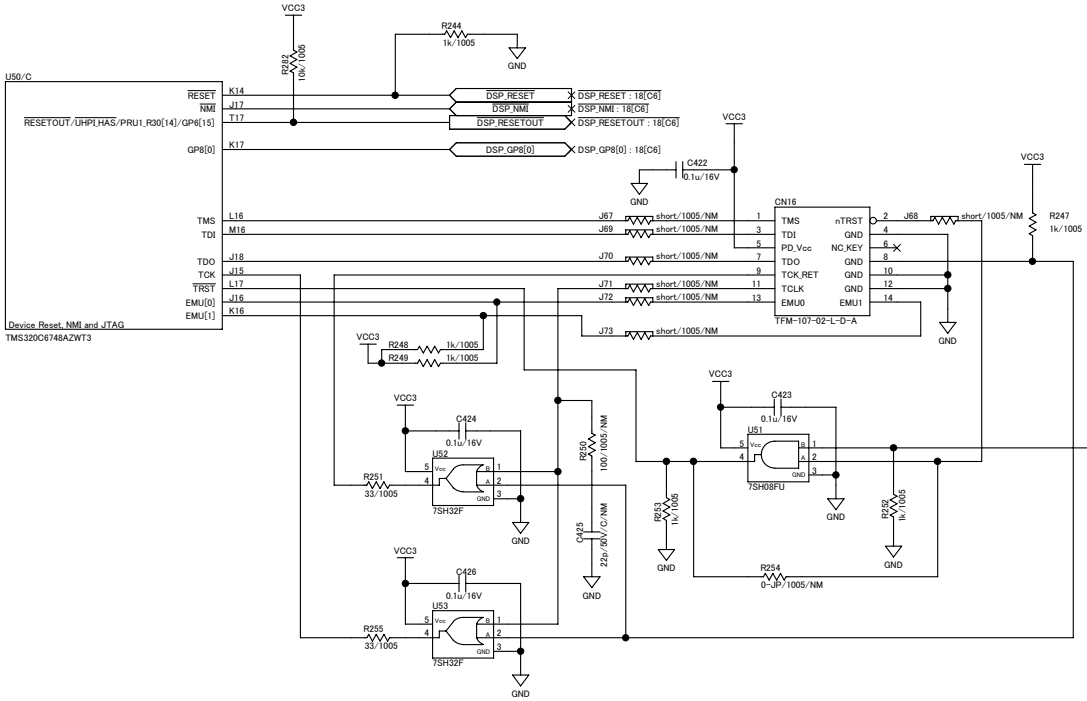

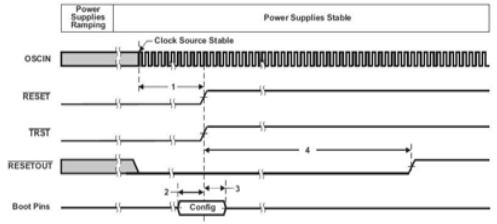

Figure 6-4. Power-On Reset (RESET and TRST active) Timing

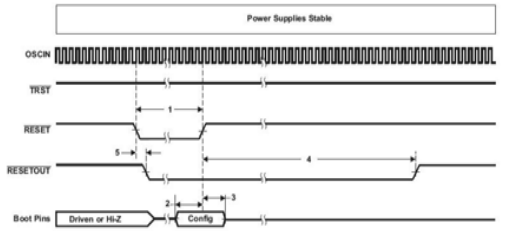

Figure 6-5. Warm Reset (RESET active, TRST high) Timing

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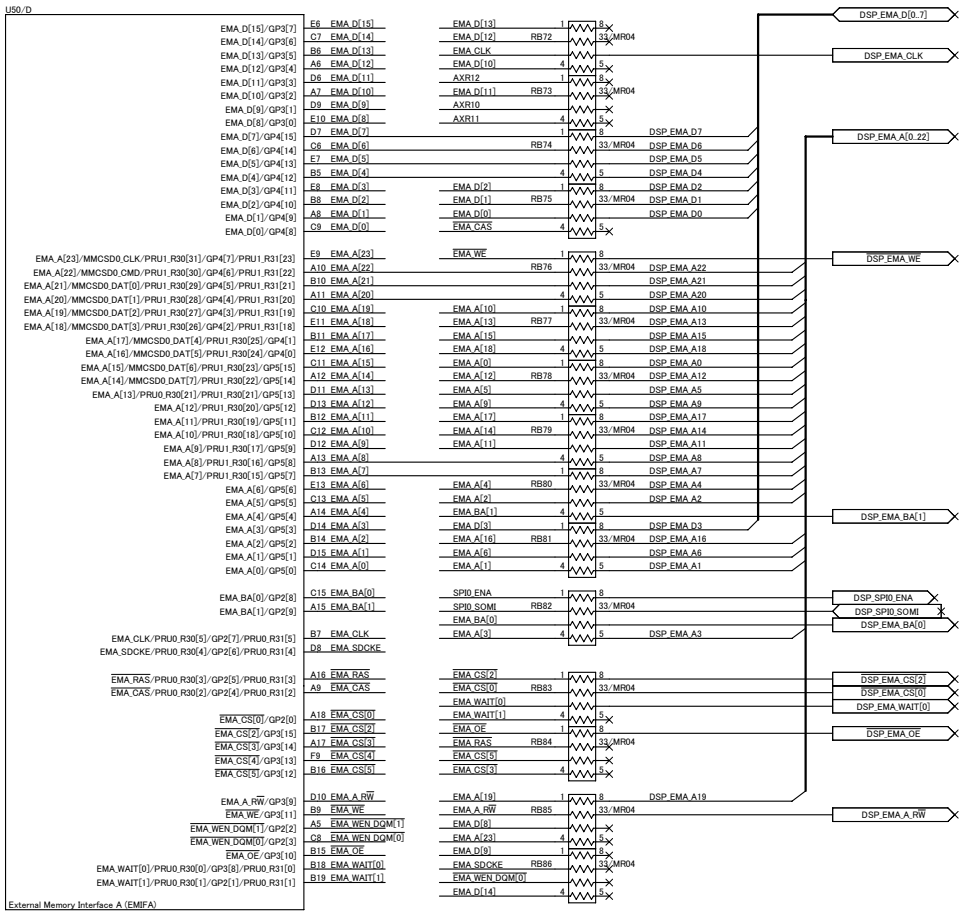


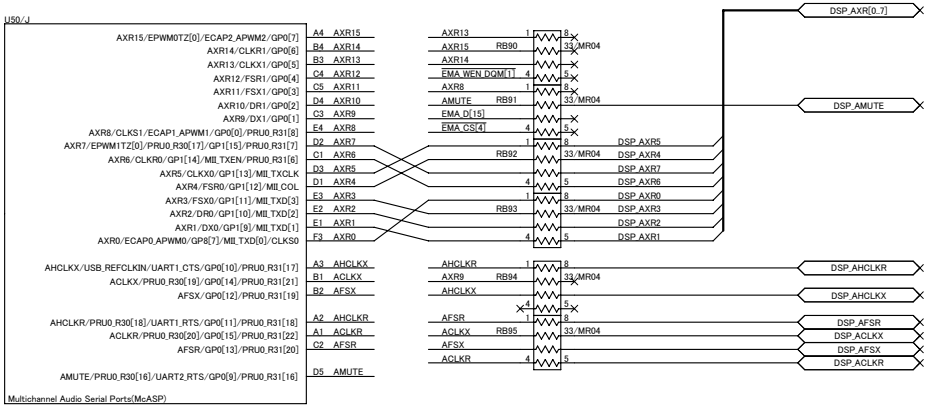
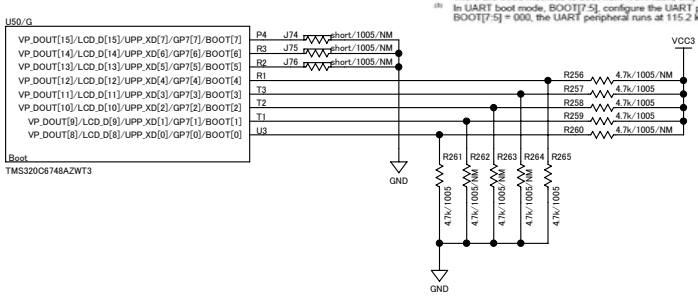
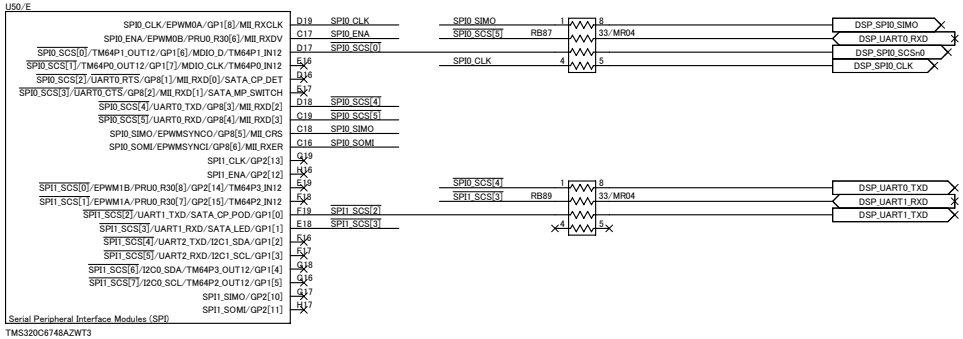


Table 8. Boot Mode Selection

BOOT[7:0] (1)	Boot Mode	AIS
0000 0010	NOR	Yes (2)
0000 1110	NAND 8	Yes
0001 0000	NAND16	Yes
0000 0000	I2C0 EEPROM	Yes
0000 0110	I2C1 EEPROM	Yes
0000 0001	I2C0 Slave	Yes
0000 0111	I2C1 Slave	Yes
0000 1000	SPI0 EEPROM	Yes
0000 1001	SPI1 EEPROM	Yes
0000 1010	SPI0 Flash	Yes
0000 1100	SPI1 Flash	Yes
0001 0010	SPI0 Slave	Yes
0001 0011	SPI1 Slave	Yes
xxx1 0110 (3)	UART0	Yes
xxx1 0111 (3)	UART1	Yes
xxx1 0100 (3)	UART2	Yes
0000 0100	HPI	No
0001 1110	Emulation Debug	No

(1) The boot pins, BOOT[7:0], are multiplexed with the following signals: VPIF_DOUT[15:8], LCD_DATA[15:8], UPP_XDATA[7:0], and GPIO_7[7:0].
(2) There are three methods to boot from NOR flash; only one of them uses AIS.
(3) In UART boot mode, BOOT[7:5], configure the UART peripheral to run at standard baud rates for different input clocks. For BOOT[7:5] = 000, the UART peripheral runs at 115.2 kbps with a 24 MHz input clock. For more information, see Section 9.





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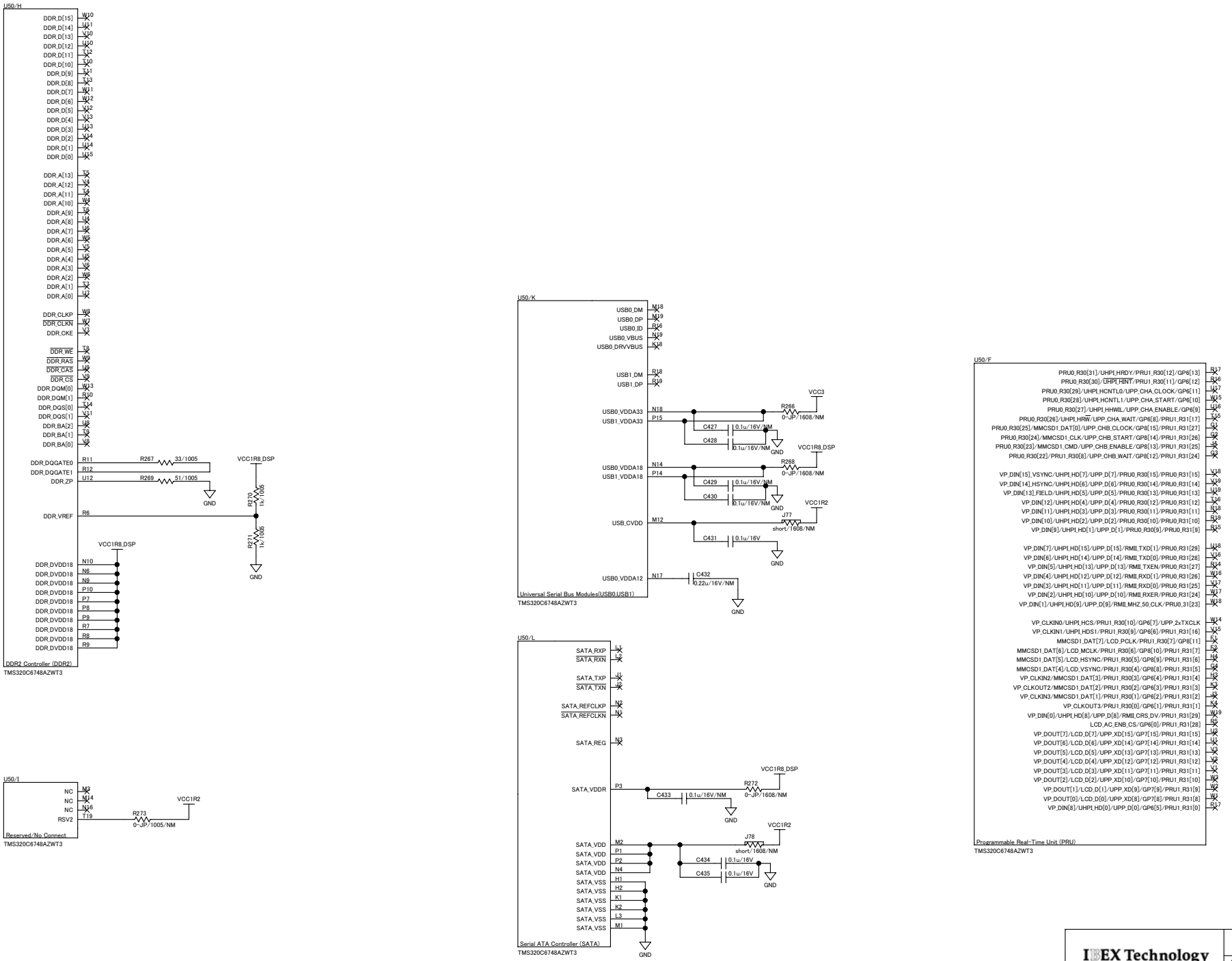
DSP3



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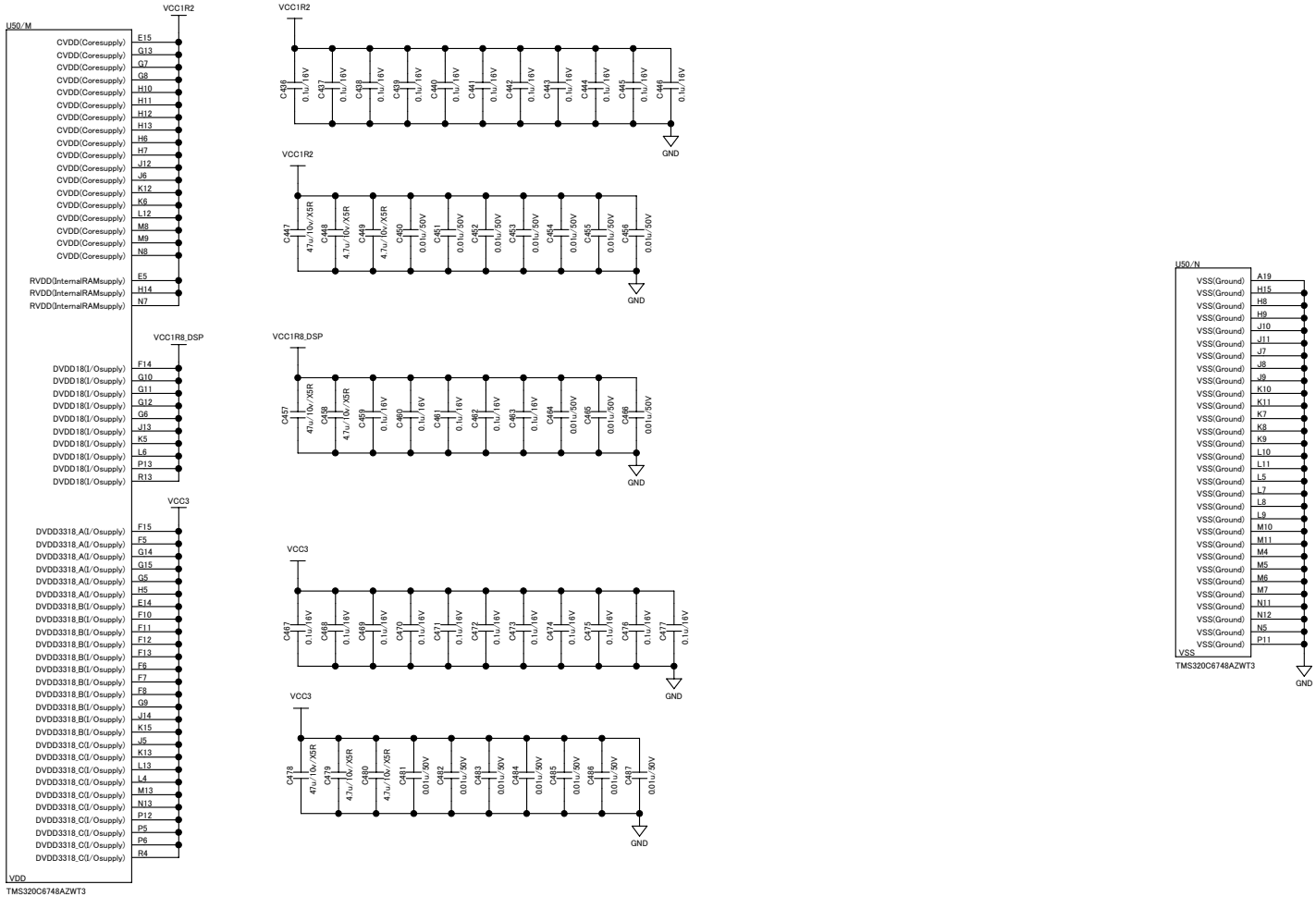
DSP_POWER



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