TMS320DM365 Video Stabilization Algorithm Datasheet

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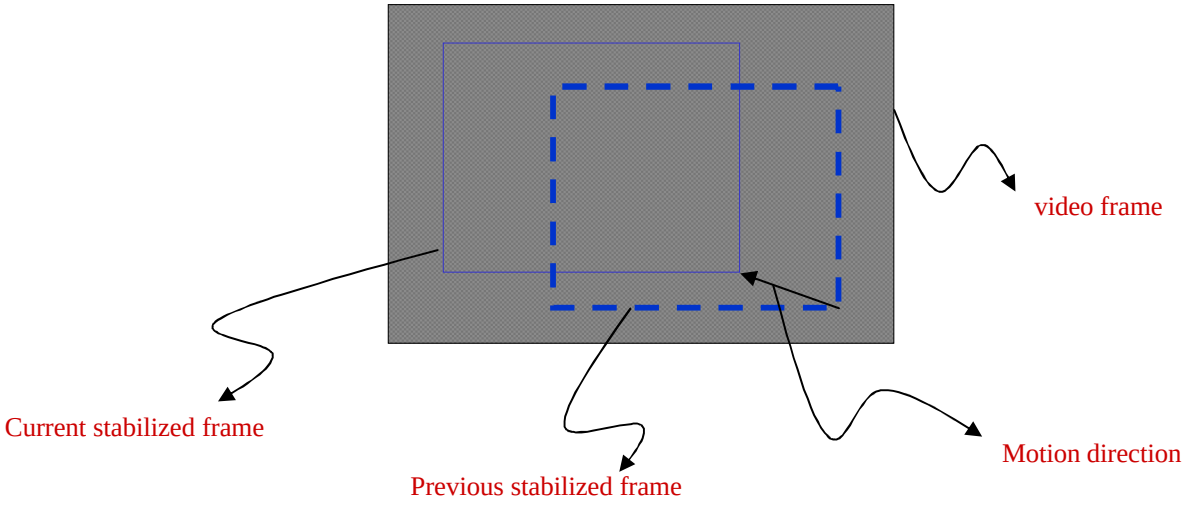
1.1 Description

The key features of Video Stabilization (VS) algorithm on TMS320DM365 are:

- VS is a video enhancement technique which reduces the jitter in video caused due to camera shake.
- VS is achieved by moving a sub-frame in the video frame in opposite direction to the camera movement.



- VS algorithm returns the co-ordinates of the upper left corner of the sub-frame and size of the sub-frame in the video frame.
- Boundary Signal Calculator (BSC) is a programmable hardware module which is a sub-module in IMAGE PIPE. It generates the vector sum of row and column pixels of the video frame which are called as Horizontal and Vertical BSC data respectively. BSC data of current and previous frame are input to VS algorithm.

  Pl. refer to sec. 4.5.21 of DM350_Spec_SOC_PRG_VPFE_B05.pdf for more details on BSC module.

- Since BSC is a sub-module in IMAGE PIPE, it always operates on the video frame input to IMAGE PIPE. In other words VS algorithm is always applied to the video frame which is input to IMAGE PIPE.
- Major part of VS algorithm (SAD computation of BSC data) is executed on iMX.

1.2 Performance

- VS algorithm compensates the camera movement which is up to +/- 10% of the sub-frame width in Horizontal direction and sub-frame height in vertical direction.

- VS algorithm (iMX version) takes ***1.85 milli sec*** for an IMAGE PIPE input of size ***1280 x 960***.
- VS algorithm (C version) takes ***8.5 milli sec*** for an IMAGE PIPE input of size ***1280 x 960***.

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1.3 Memory Requirement

- VS algorithm requires the following 4 buffers to hold BSC data:
  - Horizontal BSC data of current frame.
  - Vertical BSC data of current frame.
  - Horizontal BSC data of previous frame
  - Vertical BSC data of previous frame.

  Each BSC data is 16 bit in length.
  The size of each buffer is limited to 1920 x 2 = 3840 Bytes by BSC module.
  Total size of BSC data buffers = 4 x 3840 = 15360 Bytes = 15 KB

- VS algorithm needs around 5 KB of memory to be used as scratch memory.

Total memory requirement of VS algorithm = 15 + 5 = 20 KB.

1.4 Processor MIPS Requirement

Since Major part of the algorithm (SAD computation of BSC data) gets executed on Hardware accelerator (iMX), processor MIPS requirement is negligible.

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