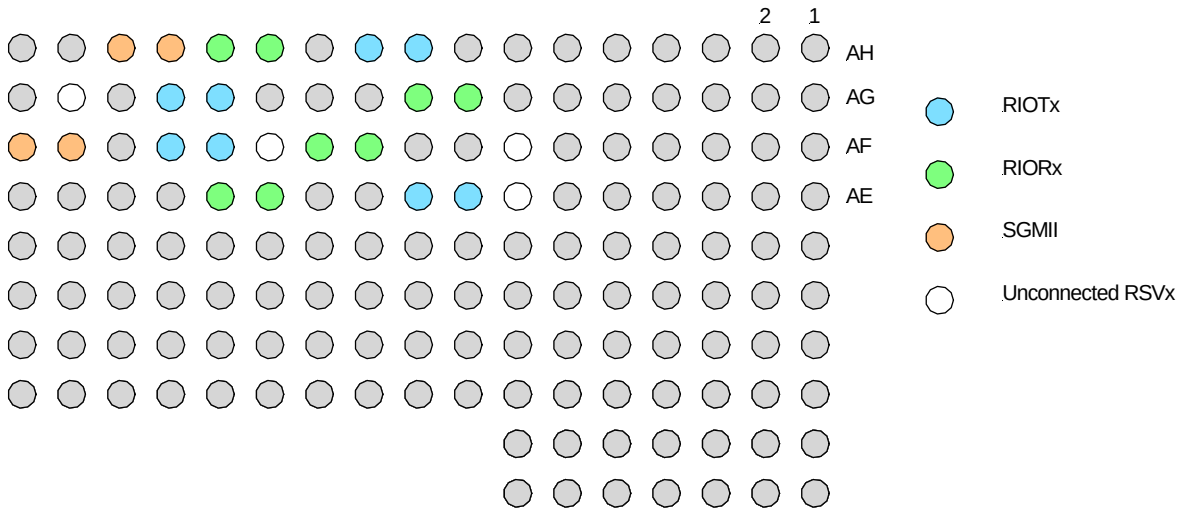
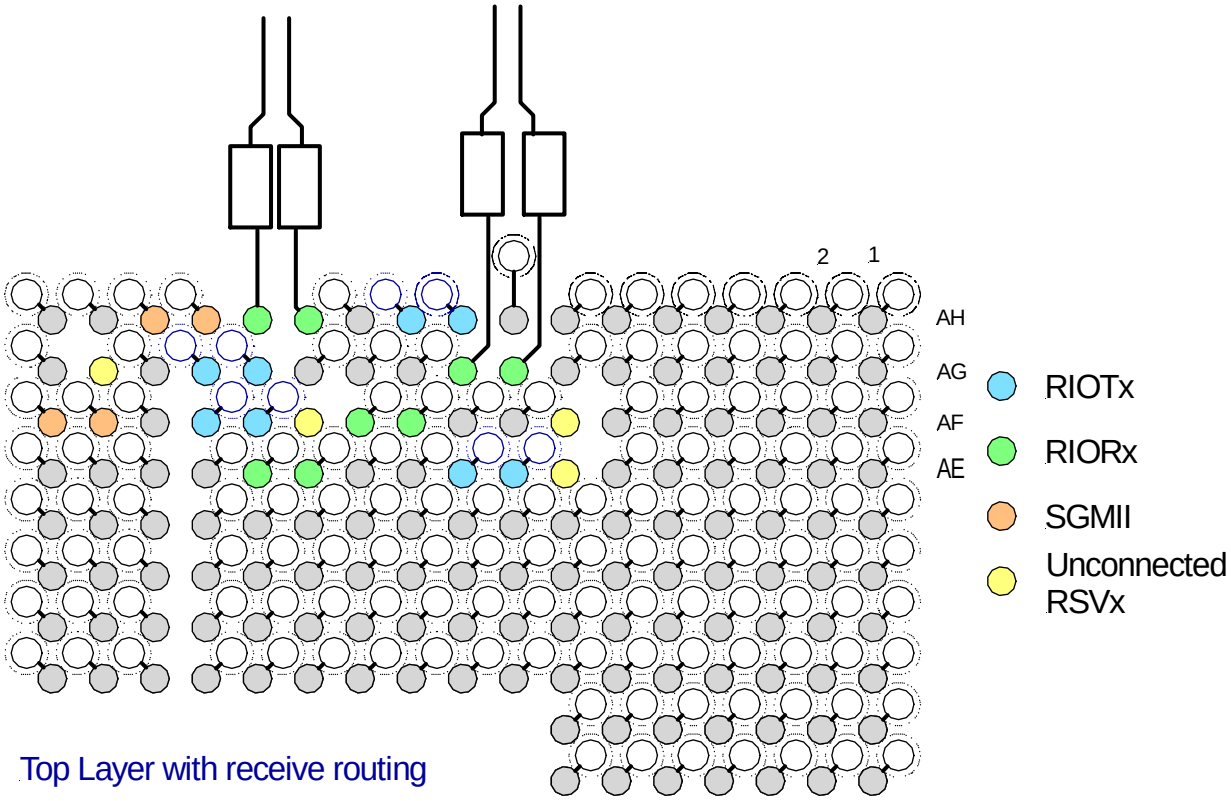
Serial RapidIO Routing for the TMS320C6457

The routing of high speed SERDES interfaces in crucial to achieving the full transfer rates supported by the interface. The routing requirements for the C6457 are described in section 2.3 of Application Report SPRAAY1A – TMS320TCI6484 and TMS320C6457 SerDes Implementation Guidelines. All guidelines should be followed where possible but the pinout for the C6457 provides some challenges. This document provides some clarification on the BGA escape for the transmit and receive signal pairs of the C6457.

The layout guidelines published for the C6457 state that it is strongly recommended to route the trace from the SerDes receive pad to the capacitor pad on the top layer assuming that both C6457 and the capacitor are mounted to the top layer of the board. Although this routing is ideal the placement of the RIOTx and RIORx pins make this difficult. Using 4mil traces only one trace may be routed between two pads. Once the space between the outer most ring of pads has been used for routing, any pads closer to the center of the part will require a via to carry the signal to an internal layer in order to escape from under the part. In general only the first two rings can be routed from under the part without vias. Consequently the pairs on row AF and AE will need to use a via next to the pad to escape from under the part.

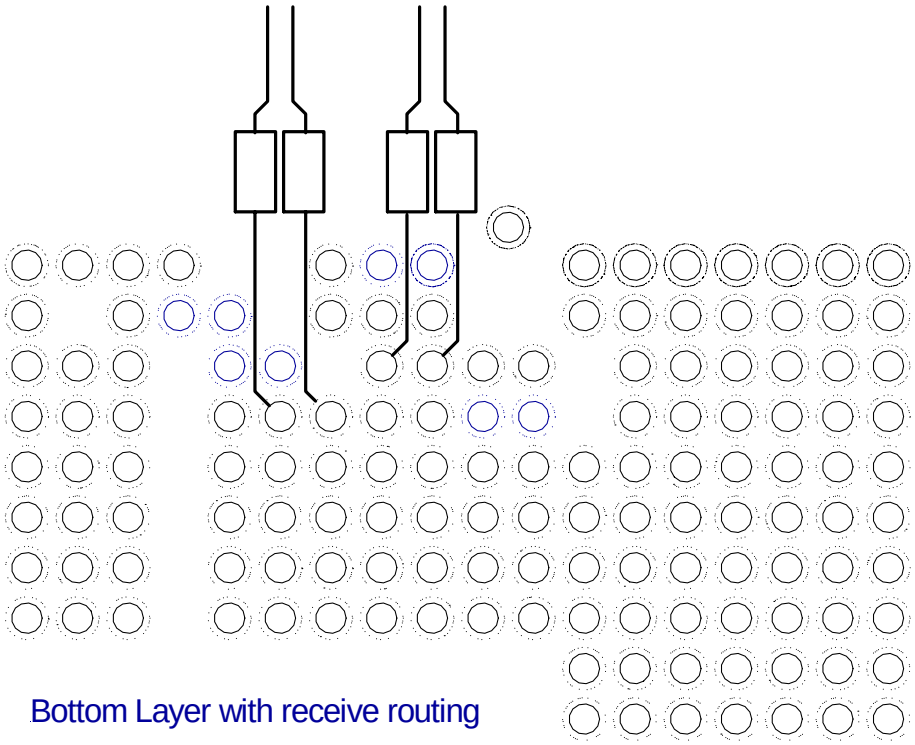


Routing the receive pairs on row AH and AG can be accomplished as recommended with the capacitors on the same layer as the C6457. Once the traces have escaped from the BGA the width and separation should be adjusted to achieve the 100ohm differential impedance. An example of the routing for the top of the board is shown below. Be sure to meet all length match requirements as well.



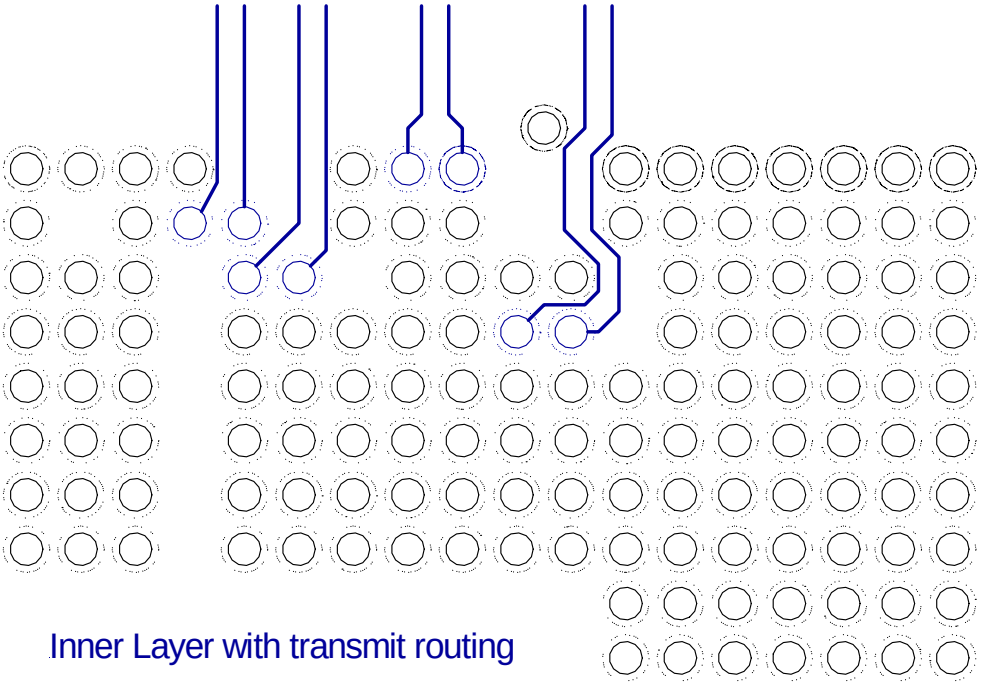
Top Layer with receive routing

It isn’t possible to route the receive pairs on rows AF and AE on the top layer therefore vias must be used to escape from the BGA. Since the number of vias should be minimized the remaining receive signal pairs should be routed to capacitors on the bottom layer. A top view example of this routing is shown below.



Bottom Layer with receive routing

Unfortunately routing the receive pairs on both the top and the bottom requires that the transmit pairs escape on an inner layer. Note that all four pairs are shown routed on the same layer but to achieve the best signal quality some of the pairs may be routed on a different inner layer depending an the connection at the other end of the trace. Whatever layer is used the signals must be routed on a layer adjacent to a solid plane.

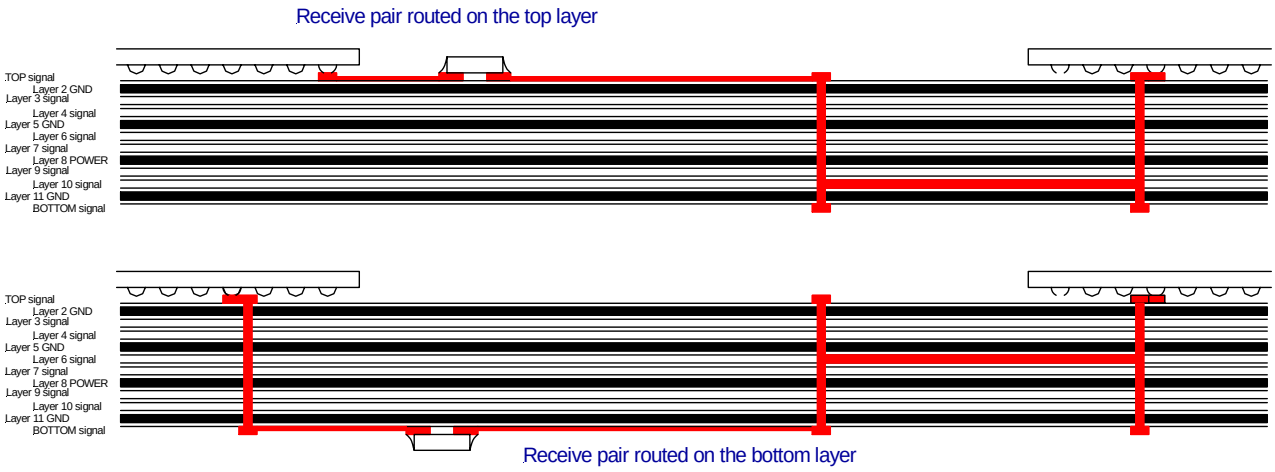


Inner Layer with transmit routing

It's clear that using an inner layer to escape the transmit pairs will ensure that there will be some via stub on the trace. The length of the stub portion of the via should be minimized where ever possible. Studies have shown that the stub will have an impact on signal quality and cause significant transmission loss at the resonance. In addition the frequency of the resonance is proportional to the length of the stub where the frequency of the interference will decrease as the stub length increases. Connecting two close layers with a plated thru-hole via will leave a stub that can effect the transmission frequencies of the serial rapidIO interface. This should be avoided.

Now that the signals have escaped from under the BGA care should be taken to connect them in the best manner possible. If serial rapidIO interfaces of two C6457 components are connected together at least one additional via is needed to connect the receive pairs on either the top or the bottom from one part with the transmit pairs of the second part on an inner layer. For receive signals routed on the top layer this can be accomplished with minimal via stubs. A via is added at some point between the capacitor and the second C6457 and the transmit portion of the trace is routed on the inner layer closest to the bottom while still adjacent to a plane. In the example below this is layer 10 which is adjacent to the ground plane on layer 11. This will allow the trace to be routed to the via under the second C6457 while minimizing the stub.

The receive signals routed on the bottom layer are more difficult to connect. In this case routing on layer 10 or layer 3 would minimize the stub on one end of the trace but leave a longer stub at the other end. To ensure that the interference due to the via stubs is present at the highest frequency possible the transmit trace should be routed close to the center of the board insuring that the two via stubs are as close to equal length as possible. This is shown in the figure below. In this example the transmit pairs would be routed on both layer 10 and layer 6. Routing the transmit traces on two layers may not be possible due to the long continuous stretches of trace creating a block for other signals. If it is desired that all of the transmit trace be routed on the same layer, a center layer should be used to minimize the length of the via stubs.



If the signals are routed to a surface mount component or connector that doesn't have the escape limitations the routing can be optimized to reduce the number of vias and the via stubs. The figure below illustrates the connection between a C6457 and a surface mount connector. In all three cases, receive routed on top, receive routed on the bottom and transmit routed internally, the connection is made with the smallest stub possible insuring the best possible performance.