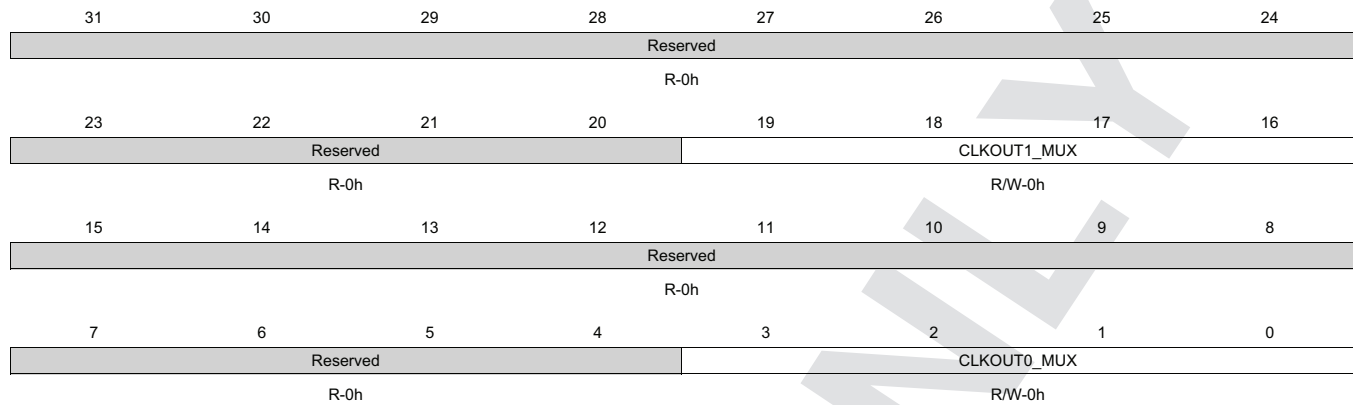


1.9.1.146 CLKOUT_MUX Register (offset = 2E4h) [reset = 0h]

CLKOUT_MUX is shown in Figure 1-173 and described in Table 1-186.

Figure 1-173. CLKOUT_MUX Register



LEGEND: R/W = Read/Write; R = Read only; W1toC1 = Write 1 to clear bit; -n = value after reset

Table 1-186. CLKOUT_MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	Reserved	R	0h	
19-16	CLKOUT1_MUX	R/W	0h	Select the source clock of the CLKOUT1 0 - 0000: Source is PRCM_SYSClk_OUT 1 - 0001: Source is SATA SERDES OBS CLK 10 - 1010: RCOSC32K OUT 11 - Reserved 2 - 0010: Source is PCIe SERDES OBS CLK 3 - 0011: Source is DSS_DPLL_OUT_DIV2 4 - 0100: Source is ISP_DPLL_OUT_DIV2 5 - 0101: Source is L3_DPLL 6 - 0110: Source is OSC0 OUT 7 - 0111: Source is OSC1 OUT 8 - 1000: Modena Func Clock OUT 9 - 1001: SGX_DPLL OUT
15-4	Reserved	R	0h	
3-0	CLKOUT0_MUX	R/W	0h	Select the source clock of the CLKOUT0 0 - 0000: Source is PRCM_SYSClk_OUT 1 - 0001: Source is SATA SERDES OBS CLK 10 - 1010: RCOSC32K OUT 11 - Reserved 2 - 0010: Source is PCIe SERDES OBS CLK 3 - 0011: Source is DSS_DPLL_OUT_DIV2 4 - 0100: Source is ISP_DPLL_OUT_DIV2 5 - 0101: Source is L3_DPLL 6 - 0110: Source is OSC0 OUT 7 - 0111: Source is OSC1 OUT 8 - 1000: Modena Func Clock OUT 9 - 1001: SGX_DPLL OUT