Table 4-11. PINCNTL1 – PINCNTL270 (PINCNTLx) Registers Bit Descriptions

Bit	Field	Description	Comments
31:20	RESERVED	Reserved. Read only, writes have no effect.	For PINCNTLx register reset value examples, see Table 4-12, *PNICNTLx Register Reset Value Examples*. For the full register reset values of all PINCNTLx registers, see Table 4-13, *PINCNTLx Registers MUXMODE Functions*.
19	RSV	Reserved. This bit ***must*** always be written with the reset (default) value. (See Table 4-13 for full register reset value)	
18	RSV	Reserved. This field ***must*** always be written as "1".	
17	PLLTYPSEL	Pullup/Pulldown Type Selection bit 0 = Pulldown (PD) selected 1 = Pullup (PU) selected	
16	PLLUDEN	Pullup/Pulldown Enable bit 0 = PU/PD enabled 1 = PU/PD disabled	
15:8	RESERVED	Reserved. Read only, writes have no effect.	
7:0	MUXMODE[7:0]	MUXMODE Selection bits These bits select the multiplexed mode pin function settings (seeTable 4-13, *PINCNTLx Registers MUXMODE Functions*). Values other than those shown inTable 4-13 are illegal.	

Table 4-12. PINCNTLx Register Reset Value Examples

HEX ADDRESS RANGE	PINCNTLx REGISTER NAME	Bits 31:24	Bits 23:20	Bit 19	Bit 18	Bit 17	Bit 16	Bits 15:8	Bits 7:0	Register Reset Value
		RESERVED	RESERVED	RSV	RSV	PLLTYPESEL	PLLUDEN	RESERVED	MUXMODE[7:0]	
0x4814 0800	PINCNTL1	00h	0h	0	1	1	0	00h	00h	0x0006 0000
0x4814 0804	PINCNTL2	00h	0h	1	1	1	0	00h	00h	0x000E 0000
0x4814 0808	PINCNTL3	00h	0h	1	1	1	0	00h	00h	0x000E 0000
…										
0x4814 0C34	PINCNTL270	00h	0h	1	1	0	0	00h	00h	0x000C 0000

(1) "(M0)" represents multimuxed option "0" for this pin function, "(M1)" represents multimuxed option "1" for this pin function, ... etc.

(2) Within this MUXMODE setting, EMAC[x] GMII or RGMII pin functions are selected via the RGMII0_EN and/or RGMII1_EN bits (8 and 9, respectively) in the GMII_SEL register [0x4814_0650] of the Control Module. "0" = GMII (default) and "1" = RGMII.

PRODUCT PREVIEW