EVM2812 Hardware Manual

REV1.0

Jumper Manual

JP1. MOTOR CONTROL BUS1

JP1 Motor Contor Bus 1
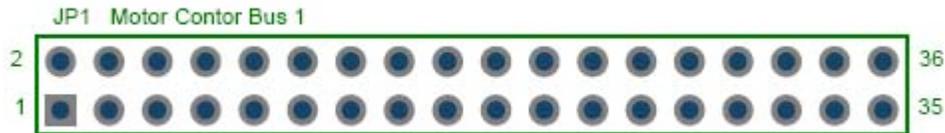
Pin #	Signal	Pin #	Signal
1	+3.3V	2	+3.3V
3	PWM1	4	PWM2
5	PWM3	6	PWM4
7	PWM5	8	PWM6
9	T1PWM	10	T2PWM
11	CAP1	12	CAP2
13	CAP3	14	TDIRA
15	TCKINA	16	/T1CTRIP
17	XINT2	18	/T2CTRIP
19	(Empty)	20	(Empty)
21	(Empty)	22	(Empty)
23	GND	24	GND
25	+5V	26	+5V
27	(Empty)	28	ADCLO
29	ADINA6	30	ADINA7
31	ADINA4	32	ADINA5

| 33 | ADINA2 | 34 | ADINA3 |
| 35 | ADINA0 | 36 | ADINA1 |

JP2. MOTOR CONTROL BUS2

JP2 Motor Contor Bus 2

Pin #	Signal	Pin #	Signal
1	+3.3V	2	+3.3V
3	PWM11	4	PWM12
5	PWM9	6	PWM10
7	PWM7	8	PWM8
9	T3PWM	10	T4PWM
11	CAP4	12	CAP5
13	CAP6	14	TDIRB
15	TCKINB	16	/T3CTRIP
17	XINT1	18	/T4CTRIP

19	SIMOA	20	SOMIA
21	CLKA	22	STEA
23	GND	24	GND
25	+5V	26	+5V
27	RST	28	ADCLO
29	ADINB6	30	ADINB7
31	ADINB4	32	ADINB5
33	ADINB2	34	ADINB3
35	ADINB0	36	ADINB1

JP3. Address Bus
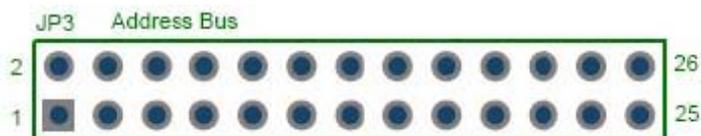
Pin #	Signal	Pin #	Signal
1	A0	2	A1
3	A17	4	A16
5	A15	6	A14
7	A13	8	A12
9	A2	10	A3
11	A6	12	A5
13	A4	14	A9
15	A8	16	A7
17	A10	18	A18
19	A11	20	/XHOLD
21	+5V	22	+3.3V
23	GND	24	(¿Õ)
25	XREADY	26	XCLKOUT

Note: Address buses are not in order because in design, there is no consideration for equal length of signal line and address line.

JP4. DATA Bus JP8. MCBSP

JP4 DATA BUS
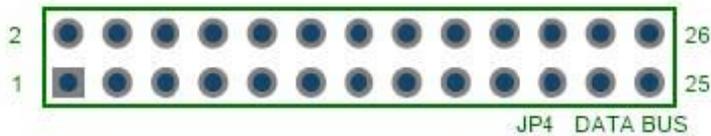
Pin #	Signal	Pin #	Signal
1	D0	2	D1
3	D2	4	D3
5	D4	6	D5
7	D6	8	D7
9	D8	10	D9
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15
17	CS01	18	RD
19	CS2	20	+3.3V
21	CS67	22	WR
23	XR/W	24	GND
25	MP/MC	26	/XHOLD

JP8
McBSP
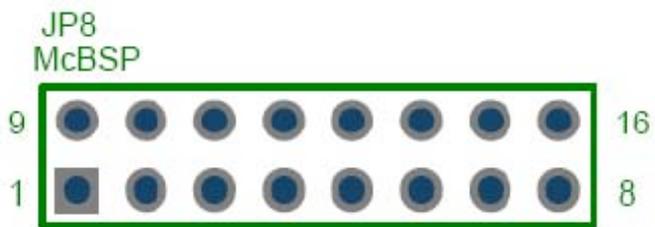
Pin #	Signal	Pin #	Signal
1	XF	2	XNMI
3	/C1TRIP	4	/C2TRIP
5	/C3TRIP	6	/C4TRIP
7	/C5TRIP	8	/C6TRIP
9	MDXA	10	MDRA

11	MFSXA	12	MCLRXA
13	MSXRA	14	MCLKXA
15	+3.3V	16	GND

JP9. DAC
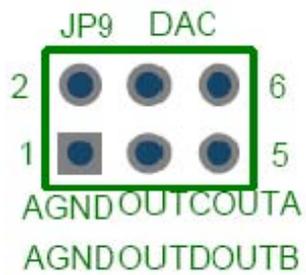
Pin #	Signal	Pin #	Signal
1	AGND	2	AGND
3	OUTD	4	OUTC
5	OUTB	6	OUTA

JP10. JTAG

Standard DSP JTAG, connected with DSP Emulator.

JP6. CAN
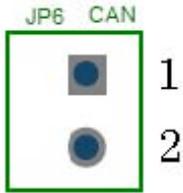
Pin #	Signal	Pin #	Signal
1	CANH	2	CANL

Note: R& is terminal end resistor. When connecting to CAN, this resistor needs to be soldered, as 120Ω.

JP11. POWER
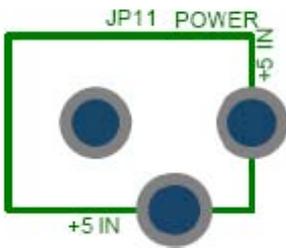
JP11 is power supply input port for 5V DC input.

JP5 MP/MC

MP/MC Jumper, when debugging, not in jumpering, JP5 is in MP mode. When

downloading Flash, JP5 is in jumpering, it's in MC mode.

JP12 SCS/CS
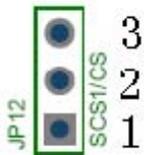
SCS/CS Jumper is for DA to choose signals. When 1-2 are in jumpering, it is SCS mode,

using DSP's IOF4 and IOF5 as IO port to produce chip-selection signals, and use 74

HC139 to produce SPI external device chip selection logic signal. SCS1 is DAC chip-

selection signal (DAC is TLV5614,SPI interface); SCS2 is X25650£¨EEPROM SPI

interface£©chip-selection signal£¬SCS3 is external SPI bus chip-selection signal. Real

values as following

IOF5	IOF4	SCS
0	1	SCS1

1	0	SCS2
1	1	SCS3

JP7 ADCLO

When ADCL0 Jumper is in jumpering, it is internal AGND input; when not in jupering, it

is JP1 or JP2 bus ADCL0 pin, input external AD sampling signal's ADC earth level

signal.