1.5-V to 7-V, ULTRA LOW DROPOUT REGULATOR

Check for Samples: TPS7H1101-SP, TPS7H1201-HT

FEATURES

- Current Share/Parallel Operation to Provide Higher Output Current
- Wide V_{IN} Range: 1.5 V - 7 V
- 5962R13202:
  - Radiation Hardness Assurance (RHA) up to TID 100 krad (Si)
  - Total Ionizing Dose 100 krad (Si)
  - ELDRS free 100 krad (Si)
  - Dose rate 10mRAD(si)/sec
  - Single Event Latchup (SEL) Immune to LET = 85MeV-cm2/mg
  - SEB and SEGR Immune to LET = 85MeV-cm2/mg
  - SET/SEFI Onset Threshold is = 40MeV-cm2/mg, See Radiation Report for details
  - SET/SEFI Cross-Section Plot, See Radiation Report for details
- Stable With Ceramic Output Capacitor
- ±2.0 % Accuracy over Line, Load and Temperature (TPS7H1101-SP)
- ±4.2 % Accuracy over Line, Load and Temperature (TPS7H1201-HT)
- Programmable SoftStart
- PowerGood Output
- Low Dropout Voltage
  - TPS7H1201-HT
    100 mV (MAX) at 0.5 A (210°C) , V_{OUT}= 6.8V
  - TPS7H1101-SP
    62 mV at 1 A (25°C), V_{OUT} = 1. 8V
    125 mV at 2 A (25°C), V_{OUT} = 1.8 V
    196 mV at 3 A (25°C), V_{OUT} = 1.8 V
    210 mV at 3 A (25°C), V_{OUT} = 1.3 V
    335 mV (MAX) at 3A (125°C) , V_{OUT} = 1.3 V
- Low Noise
  - TPS7H1201-HT
    20.26 µVRMS (V_{IN} = 2.1 V, V_{OUT} = 1.8 V at 0.5 A)
    31.0 µVRMS (V_{IN} = 7 V, V_{OUT} = 6.7 V at 0.5 A)
  - TPS7H1101-SP
    20.33 µVRMS (V_{IN} = 2 V, V_{OUT} = 1.8V at 3A)
    31.68 µVRMS (V_{IN} = 7 V V_{OUT} = 6.7V at 3A)
- PSRR: Over 45 dB at 1 kHz
- Load/Line Transient Response
- Fold-Back Current Limit (TPS7H1101-SP)
- 16-Pin Thermally Enhanced Ceramic Flatpack Package (HKS/HKR) and KGD (Bare Die) package

APPLICATIONS

- TPS7H1101-SP: Rad Tolerant Applications
- RF 5-V Components VCOs, Receivers, ADCs, Amplifiers
- Clock Distribution
- Clean Analog Supply Requirements
- Supports Harsh Environment Applications
- TPS7H1201-HT Available in Extreme (–55°C to 210°C) Temperature Range TPS7H1101-SP Available in Military (–55°C to 125°C) Temperature Range (1)
- TPS7H1201-HT: Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.
- Engineering Evaluation (/EM) Samples are Available (2)

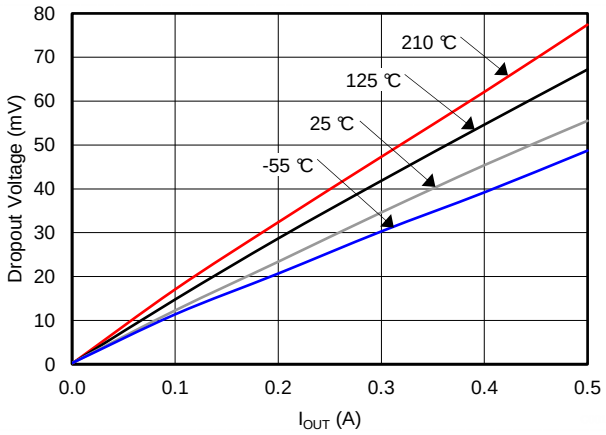
(1) Custom temperature ranges available
(2) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. No Burn-In, etc.) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of -55°C to 125°C or operating life.

DESCRIPTION

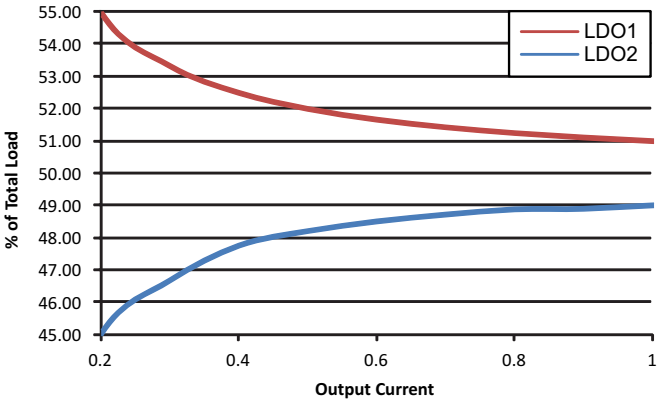
The TPS7H1x01 is a low dropout (LDO) linear regulator that uses a PMOS pass element configuration. It operates under wide range of input voltage, from 1.5 V to 7V while offering excellent PSRR. The TPS7H1x01 features a precise and programmable fold back current limit implementation with a very wide adjustment range. To support complex power requirements of FPGAs, DSPs, or Microcontrollers the TPS7H1x01 provides enable on/off functionality, programmable SoftStart, current sharing capability, and a PowerGood open drain output. The TPS7H1x01 is available in a thermally enhanced16-pin ceramic flatpack package (CFP) and KGD (Bare Die) package.

DESCRIPTION (CONTINUED)

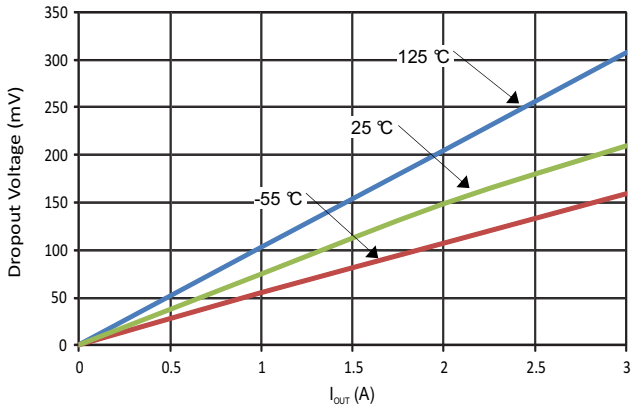
VDO vs. I_{OUT} (TPS7H1201-HT)



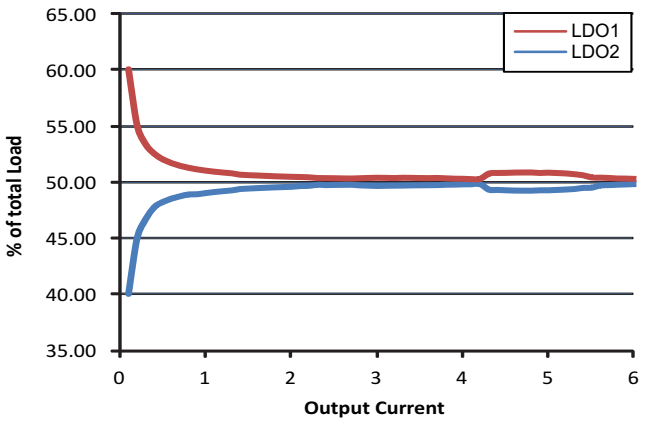
LDO Current Share (TPS7H1201-HT)



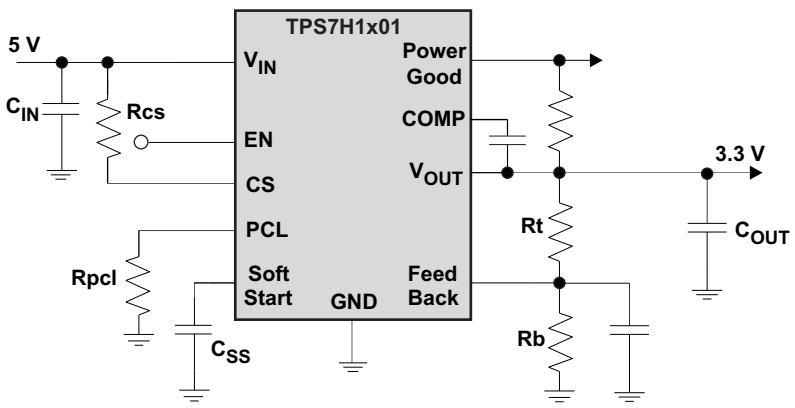
VDO vs. I_{OUT} (TPS7H1101-SP)



LDO Current Share (TPS7H1101-SP)



TYPICAL APPLICATION CIRCUIT



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)			
			UNIT
Input voltage range	V_{IN}, PG	-0.3 to 7.5	V
	FB, COMP, PCL, CS, EN	-0.3 to V_{IN} + 0.3	V
Output voltage range	V_{OUT} , SS	-0.3 to V_{IN}	V
Peak output current		Internally limited	A
PG pin sink current		5	mA
Electrostatic discharge rating (HBM)		2	kV
Electrostatic discharge rating (CDM)		1	kV
Maximum Operating junction temperature, T_J	TPS7H1201	-55 to 220	°C
	TPS7H1101	-55 to 150	
Storage temperature, T_J	TPS7H1201	-65 to 220	°C
	TPS7H1101	-65 to 150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION(1)(2)(3)

THERMAL METRIC(4)		TPS7H1x01			UNITS
		HKS (HeatSlug_up_no Underfill)(5)	HKR (HeatSlug_down Underfill)(6)(7)	HKR (HeatSlug_down_no Underfill)	
		16 PINS	16 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(8)	75.4	30.7	86.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(9)	0.4	N/A	N/A	
θ_{JB}	Junction-to-board thermal resistance(10)	4.8	69	59.3	
ψ_{JT}	Junction-to-top characterization parameter(11)	1.1	2.4	5	
ψ_{JB}	Junction-to-board characterization parameter(12)	53.5	12.3	63.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(13)	N/A	0.6	0.6	

(1) Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.
(2) Maximum power dissipation may be limited by overcurrent protection.
(3) Test board conditions:
  (a) 2.5 inches × 2.5 inches, 4 layers, thickness: 0.062 inch
  (b) 2 oz. copper traces located on the top of the PCB
  (c) 2 oz. copper ground planes on the 2 internal layers and bottom layer
  (d) 48 0.010 inch thermal vias located under the device package
(4) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(5) Power rating at a specific ambient temperature T_A should be determined with a junction temperature below 220°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 220°C for best performance and long-term reliability.
(6) Power rating at a specific ambient temperature T_A should be determined with a junction temperature below 135°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 230°C for best performance and long-term reliability.
(7) Values listed in the underfill column were derived using properties from a composite, generic silver filled epoxy underfill. They are not product specific.
(8) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(9) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(10) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(11) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(12) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(13) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

TPS7H1201 ELECTRICAL CHARACTERISTICS

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.3 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG pin pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = -55°C to 210°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.5		7	V
V_{FB}	Feedback pin voltage	1.5 V ≤ V_{IN} ≤ 7 V	T_J = 125°C	0.593	0.605	0.617	V
			T_J = 210°C	0.580	0.605	0.630	V
V_{OUT}	Output voltage range			0.8		V_{IN} - 0.2	V
	Output voltage accuracy	I_{OUT} ≤ 0.5 A, 1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 6.8 V(1)	T_J = 125°C	-2		2	%
			T_J = 210°C	-4.2		4.2	%
ΔV_{OUT}%/ ΔV_{IN}	Line regulation	1.5 V ≤ V_{IN} ≤ 7 V		-0.07	0.01	0.07	%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	0.8 V ≤ V_{OUT} ≤ 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A			0.0125		%/A
ΔV_O	DC input line regulation	1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = -55°C(2)			0.5	3	mV
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 25°C(2)			0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 125°C(2)			0.2	1	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 210°C(2)			0.84	3	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = -55°C(2)			0.5	3	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 25°C(2)			0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 125°C(2)			0.2	1	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 210°C(2)			0.84	3	
ΔV_O	DC output load regulation	V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = -55°C(2)			0.05		mV
		V_{OUT} = 0.8 V, 0 ≤I_{Load} ≤ 0.5 A, T_J = 25°C(2)			0.05		
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 125°C(2)			0.07		
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 210°C(2)			0.51		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = -55°C(2)			0.10		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 25°C(2)			0.04		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 125°C(2)			0.05		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 210°C(2)			0.47		
V_{DO}	Dropout voltage	I_{OUT} = 0.5 A, V_{OUT} = 6.8 V, V_{IN} = V_{OUT} + 0.1 V			55.5	100	mV
I_{CL}	Programmable output current limit range	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, PCL resistance = 47 kΩ		500		700	mA
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance varies		200		700	mA
V_{CS}	Operating voltage range at CS			0.3		V_{IN}	V
CSR	Current sense ratio	I_{LOAD} / I_{CS}, V_{IN} = 2.3 V, V_{OUT} = 1.9 V			47394		
I_{GND}	GND pin current	V_{IN} = 1.5V, V_{OUT} = 1.2 V, I_{OUT} = 0.5 A			13	20	mA
I_Q	Quiescent current (no load)	V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 0 A			12	17	mA
I_{SHDN}	Shutdown current	V_{EN} < 0.5 V, 0.8 V ≤ V_{IN} ≤ 7 V			15	4500	µA
I_{SNS}, I_{FB}	FB/SNS pin current	V_{IN} = 7 V, V_{OUT} = 6.8 V			1	10	nA
I_{EN}	EN pin input current	V_{IN} = 7 V, V_{EN} = 7 V			6.75	610	nA
V_{ILEN}	EN pin input low (disable)				0.30 x V_{IN}		V
V_{IHEN}	EN pin input high (enable)				0.75 x V_{IN}		V
Eprop Dly	Enable pin propagation delay	V_{IN} = 2.2 V, EN rise to I_{OUT} rise			650	1000	µs

(1) Based upon using 0.1% resistors.
(2) Line and load regulations done under pulse condition for T < 10 ms.

TPS7H1201 ELECTRICAL CHARACTERISTICS (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.3 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG pin pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = -55°C to 210°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{EN}	Enable pin turn-on delay	V_{IN} = 2.2 V, V_{OUT} = 1.8 V, I_{LOAD} = 0.5 A, C_{OUT} = 220 µF, C_{SS} = 2 nF			1.4	1.6	ms
V_{THPG}	PG threshold on	No load,V_{OUT} = 1.2 V and V_{OUT} = 6.8 V		84	90		%
$V_{THPGHYS}$	PG hysteresis	1.5 V ≤ V_{IN} ≤ 7 V			2		%
V_{OLPG}	PG pin output low	I_{PG} = 0 to -1 mA			73	300	mV
I_{LKGPG}	PG pin leakage current	V_{OUT} > V_{THPG}, V_{PG} = 7 V			0.02	20	µA
I_{SS}	SS pin current	V_{IN} = 1.5 V to 7 V			2.5	6.3	µA
I_{SSdisb}	SS pin disable current	V_{IN} = 1.5 V to 7 V			5	13	µA
V_{SS}	SS pin voltage (device enabled)(3)	V_{IN} = 1.5 V to 7 V				1.2	V
PSRR	Power-supply rejection ratio	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, C_{OUT} = 220 µF	1 kHz		45		dB
			100 kHz		20		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 500 mA, V_{IN} = 2 V, V_{OUT} = 1.8 V			20.26		μV_{RMS}
T_J	Operating junction temperature			-55		210	°C

(3) Any external pull up voltage should not exceed 1.2 V.

TPS7H1101 ELECTRICAL CHARACTERISTICS

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG pin pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = -55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.5		7	V
V_{FB}	Feedback pin voltage(1)(1)	0 A ≤ I_{OUT} ≤ 3 A, 1.5 V ≤ V_{IN} ≤ 7 V	0.594	0.605	0.616	V
V_{OUT}	Output voltage range		0.8		V_{IN} - 0.35	V
	Output voltage accuracy(1)	0 A ≤ I_{OUT} ≤ 3 A, 1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, 1.2 V, 1.8 V, 6.65 V(2)	-2		2	%
ΔV_{OUT}%/ ΔV_{IN}	Line regulation	1.5 V ≤ V_{IN} ≤ 7 V	-0.07	0.01	0.07	%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	0.8 V ≤ V_{OUT} ≤ 6.65 V, 0 ≤ I_{Load} ≤ 3 A		0.08		%/A
ΔV_I	DC input line regulation	1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = -55°C(3)		0.5	3	mV
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 25°C(3)		0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 125°C(3)		0.2	1.0	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = -55°C(3)		0.5	3.0	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 25°C(3)		0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 125°C(3)		0.2	1.0	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, T_J = -55°C(3)		0.5	3.0	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, T_J = 25°C(3)		0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, T_J = 125°C(3)		0.2	1.0	

(1) The output voltage accuracy of condition at I_{OUT} = 2 A and I_{OUT} = 3 A is specified by characterization , but not production tested.
(2) Based upon using 0.1% resistors.
(3) Line and load regulations done under pulse condition for T < 10 ms.

TPS7H1101 ELECTRICAL CHARACTERISTICS (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG pin pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = -55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_O	DC output load regulation(4)	V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = -55°C(5)		0.4	1.0	mV
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(5)		0.6	1.1	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(5)		0.8	1.3	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = -55°C(5)		0.8	1.8	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(5)		1.3	1.8	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(5)		1.6	2.4	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = -55°C(5)		1.1	1.9	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(5)		1.9	2.6	
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(5)		2.5	3.4	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = -55°C(5)		0.3	1.2	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(5)		0.5	1.3	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(5)		0.6	1.3	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = -55°C(5)		0.8	1.6	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(5)		1.1	2.1	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(5)		1.5	2.1	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = -55°C(5)		1.0	1.7	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(5)		1.1	2.4	
		V_{OUT} = 1.2 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(5)		2.2	3.5	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = -55°C(5)		0.1	0.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(5)		0.3	0.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(5)		0.4	1.2	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = -55°C(5)		1.4	2.4	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(5)		0.7	1.4	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(5)		0.6	1.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = -55°C(5)		2.5	3.9	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(5)		1.2	2.1	
		V_{OUT} = 1.8 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(5)		1.2	2.5	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = -55°C(5)		1.5	2.9	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 25°C(5)		0.4	2.6	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 1 A, T_J = 125°C(5)		2.8	3.5	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = -55°C(5)		3.5	5.9	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 25°C(5)		1.1	4.7	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 2 A, T_J = 125°C(5)		5.8	8.0	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = -55°C(5)		5.6	9.3	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 25°C(5)		3.7	8.0	
		V_{OUT} = 6.65 V, 0 ≤ I_{Load} ≤ 3 A, T_J = 125°C(5)		13.0	25	
V_{DO}	Worst case dropout voltage(4)	I_{OUT} = 3 A, V_{OUT} = 1.3 V, V_{IN} = V_{OUT} + V_{DO}		210	335	mV
	Dropout voltage(4)	I_{OUT} = 3 A, V_{OUT} = 1.8 V, V_{IN} = V_{OUT} + V_{DO}		196		
I_{CL}	Programmable output current limit range	V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance = 47 kΩ	500		750	mA
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance varies	200		3500(6)	mA
V_{CS}	Operating voltage range at CS		0.3		V_{IN}	V

(4) The parameter is guaranteed to the limit specified by characterization, but not production tested.
(5) Line and load regulations done under pulse condition for T < 10 ms.
(6) The maximum limit of the I_{CL}parameter is guaranteed to the limit specified by characterization, but not production tested.

TPS7H1101 ELECTRICAL CHARACTERISTICS (continued)

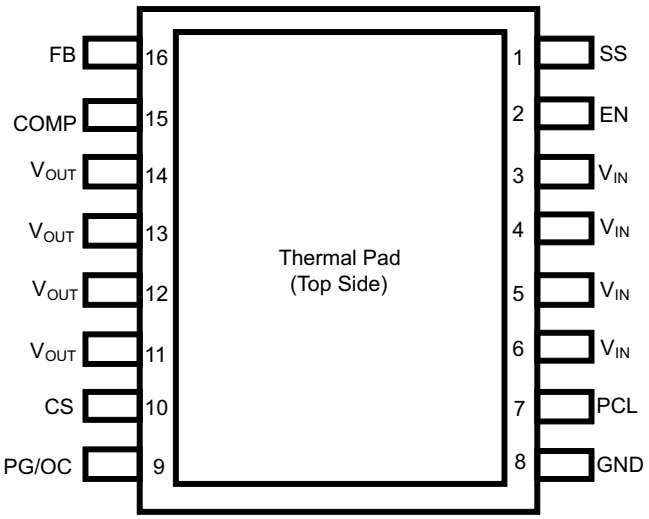
1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.35 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG pin pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = -55°C to 125°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CSR	Current sense ratio	I_{LOAD} / I_{CS}, V_{IN} = 2.3 V, V_{OUT} = 1.9 V			47394		
I_{GND}	GND pin current	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, I_{OUT} = 2 A			10	16	mA
I_Q	Quiescent current (no load)	V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 0 A			7	10	mA
I_{SHDN}	Shutdown current	1.5 V ≤ V_{IN} ≤ 7 V			26	230	µA
		1.5 V ≤ V_{IN} ≤ 7 V, Post 100kRads (si), T_J = 25°C(7)				1400	µA
I_{SNS}, I_{FB}	FB/SNS pin current	V_{IN} = 7 V, V_{OUT} = 6.65 V			1	5	nA
I_{EN}	EN pin input current	V_{IN} = 7 V, V_{EN} = 7 V, V_{OUT} = 6.65 V			20	150	nA
V_{ILEN}	EN pin input low (disable)	3.5 V < V_{IN} < 7 V			0.30 x V_{IN}		V
V_{IHEN}	EN pin input high (enable)	3.5 V < V_{IN} < 7 V			0.75 x V_{IN}		V
Eprop Dly	Enable pin propagation delay	V_{IN} = 2.2 V, EN rise to I_{OUT}rise			650	1000	µs
T_{EN}	Enable pin turn-on delay	V_{IN} = 2.2 V, V_{OUT} = 1.8 V, I_{LOAD} = 1 A, C_{OUT} = 220 µF, C_{SS} = 2 nF			1.4	1.6	ms
V_{THPG}	PG threshold	No load, 0.8 V ≤ V_{OUT} ≤ 6.65 V		86	90		%
$V_{THPGHYS}$	PG hysteresis	1.5 V ≤ V_{IN} ≤ 7 V			2		%
V_{OLPG}	PG pin output low	I_{PG} = 0 to -1 mA			120	300	mV
I_{LKGPG}	PG pin leakage current	V_{OUT} > V_{THPG}, V_{PG} = 7 V			0.5	2.5	µA
I_{SS}	SS pin charge current	V_{IN} = 1.5 V to 7 V			2.5	3.5	µA
I_{SSdisb}	SS pin disable current	V_{IN} = 1.5 V to 7 V			5	10	µA
V_{SS}	SS pin voltage (device enabled)(8)	V_{IN} = 1.5 V to 7 V				1.2	V
V_{SSdisb}	SS pin low level input voltage to disable device	V_{IN} = 1.5 V to 7 V				0.4	V
PSRR	Power-supply rejection ratio	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, C_{OUT} = 220 µF	1 kHz		48		dB
			100 kHz		25		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 3 A, V_{IN} = 2 V, V_{OUT} = 1.8 V			20.33		$µV_{RMS}$
TSD	Thermal shutdown temperature				185		°C
T_J	Operating junction temperature			-55		125	°C

(7) This maximum limit applies to SMD 5962R13202 post 100kRads (Si) test at 25°C.
(8) Any external pull up voltage should not exceed 1.2 V.

PIN ASSIGNMENTS

HKS PACKAGE
(TOP VIEW)



HKR PACKAGE
(TOP VIEW)

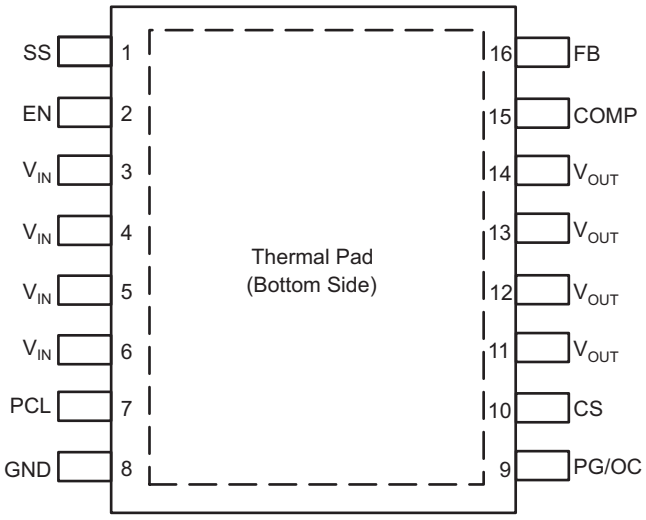


Table 1. PIN FUNCTIONS

PIN		DESCRIPTION
NAME	No.	
V_{IN}	3, 4, 5, 6	Unregulated supply voltage. It's recommended to connect an input capacitor as a good analog circuit practice.
V_{OUT}	11, 12, 13, 14	Regulated output.
FB	16	The output voltage feedback input through voltage dividers. See Feedback Circuit section.
GND	8	Ground/Thermal Pad(1)
EN	2	Enable pin. Driving this pin to logic high enables the device; driving the pin to logic low disable the device; V_{IN} voltage must be greater than 3.5 V. For V_{IN} less than 3.5 V, enable pin cannot be used to disable the device. It is recommended to connect the enable pin to V_{IN}.
CS	10	Current sense pin. Resistor connected from CS to V_{IN}. CS pin indicates voltage proportional to output current. CS pin low: Foldback current limit disabled (Apply for TPS7H1101-SP only) CS pin high: Foldback current limit enabled (Apply for TPS7H1101-SP only)
SS	1	SoftStart pin. Connecting an external capacitor slows down the output voltage ramp rate after enable event. The SoftStart pin can be used to disable the device as described in SoftStart section.
PG/OC	9	PowerGood pin. PG is open drain output to indicate the output voltage reaches to 90% of target. PG pin is also used as indicator when over current condition is activated.
PCL	7	Programmable current limit. A resistor to GND sets the over current limit activation point. The range of resistor that can be used on the PCL pin to GND is 47kΩ to 160 kΩ (TPS7H1201-HT). The range of resistor that can be used on the PCL pin to GND is 8.2 kΩ to 160 kΩ (TPS7H1101-SP).
COMP	15	Output of error amplifier

(1) Thermal Pad must be connected to GND

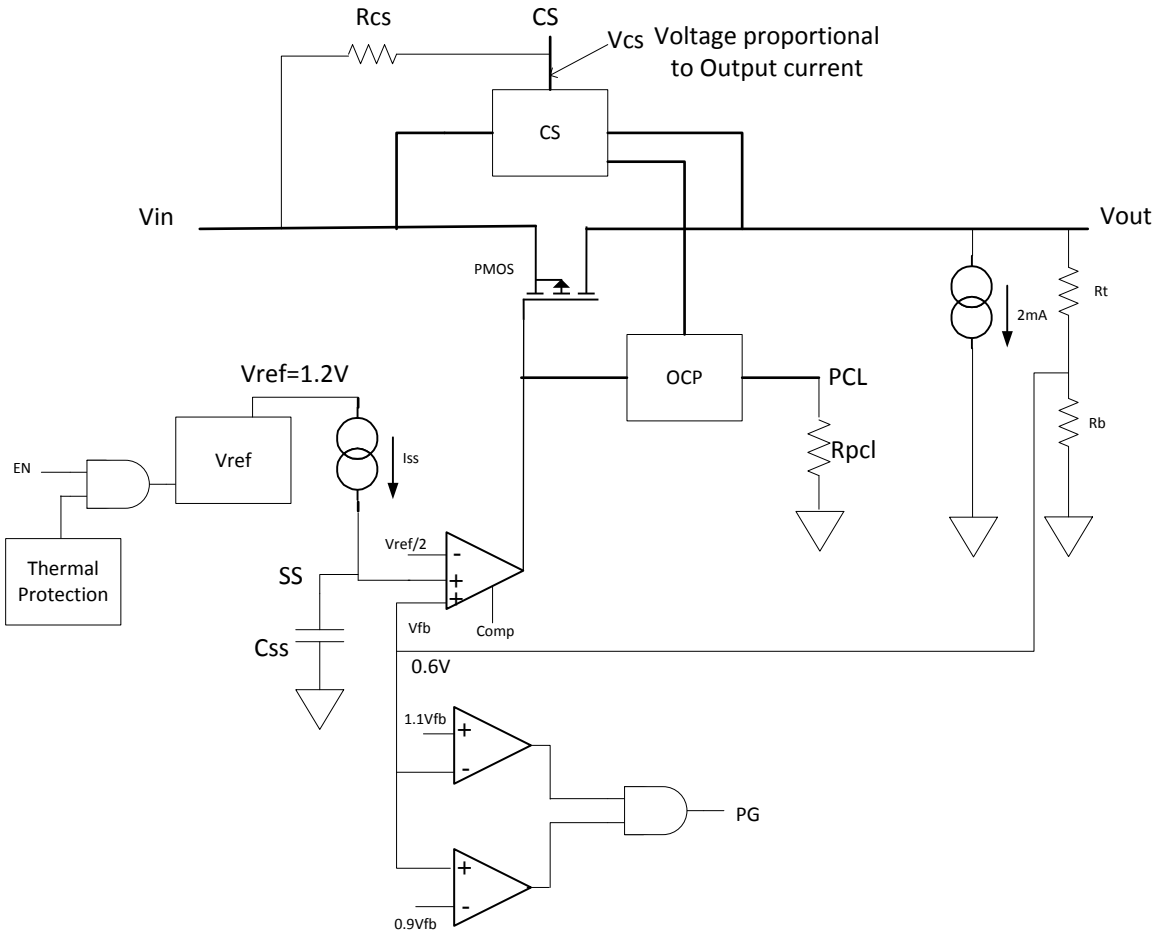
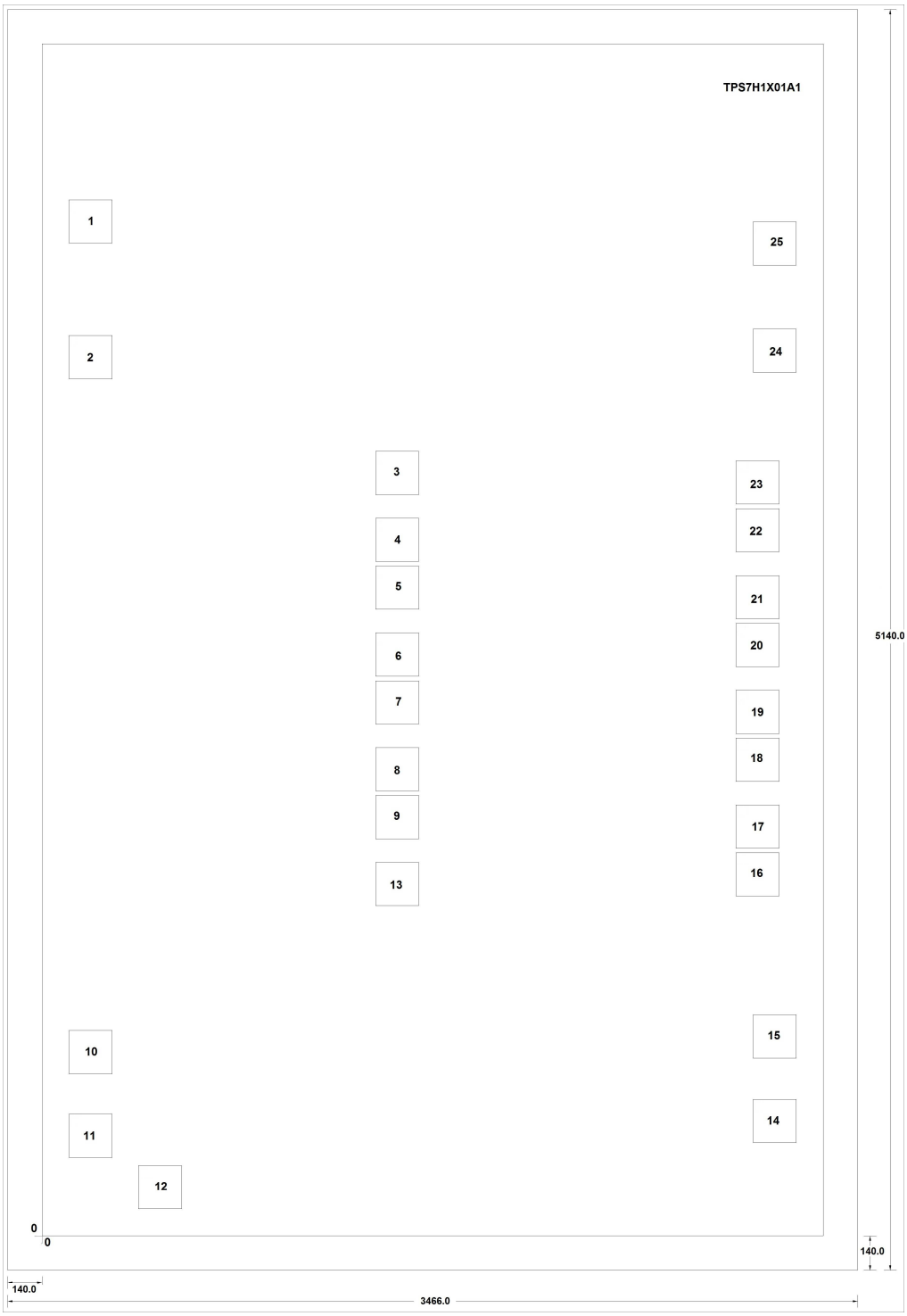


Figure 1. Functional Block Diagram

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	Ground	AlCu	30kA



A. All dimensions are in microns

Table 2. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
SS	1	109.89	4046.805	287.19	4224.105
EN	2	109.89	3493.35	287.19	3670.65
VIN	3	1359.99	3021.345	1537.29	3198.645
VIN	4	1359.99	2749.005	1537.29	2926.305
VIN	5	1359.99	2553.705	1537.29	2731.005
VIN	6	1359.99	2281.365	1537.29	2458.665
VIN	7	1359.99	2086.065	1537.29	2263.365
VIN	8	1359.99	1813.725	1537.29	1991.025
VIN	9	1359.99	1618.425	1537.29	1795.725
PCL	10	109.89	660.285	287.19	837.585
GND	11	109.89	319.455	287.19	496.755
N/C	12	392.58	109.935	569.88	287.235
VIN	13	1359.99	1346.085	1537.29	1523.385
PG/OC	14	2898.945	379.62	3076.245	556.92
CS	15	2898.945	724.32	3076.245	901.62
VOUT	16	2829.105	1384.695	3006.405	1561.995
VOUT	17	2829.105	1579.815	3006.405	1757.115
VOUT	18	2829.105	1852.335	3006.405	2029.635
VOUT	19	2829.105	2047.455	3006.405	2224.755
VOUT	20	2829.105	2319.975	3006.405	2497.275
VOUT	21	2829.105	2515.095	3006.405	2692.395
VOUT	22	2829.105	2787.615	3006.405	2964.915
VOUT	23	2829.105	2982.735	3006.405	3160.035
COMP	24	2898.945	3519.72	3076.245	3697.02
FB	25	2898.945	3956.535	3076.245	4133.835

TPS7H1X01 DETAILED DESCRIPTION

TPS7H1101 Overview

The TPS7H1101 is 3A, 1.5-V to 7-V low dropout (LDO) linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high thermal performance in a 16-pin ceramic flatpack package (HKR).

A number of features are incorporated in the design to provide high reliability and system flexibility. Current foldback, overload, current limit and thermal protection are incorporated in the design to make it viable for harsh environments.

A resistor connected from the CS (current sense) pin to V_{IN} indicates voltage proportional to the output current. When CS is held high, foldback current limit is enabled. Shorting CS low will disable the foldback current limit.

A resistor connected from programmable current limit (PCL) pin to ground sets the over current limit activation point. When over current limit activation point is reached, it results in LDO going into current foldback mode. Output current is reduced to approximately 50% of the current limit set point.

TPS7H1101 incorporates thermal protection which disables the output when the junction temperature rises approximately 185°C, allowing the device to cool. Depending on the power dissipation, thermal resistance and ambient temperature, the thermal protection wil turn on. Cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The device also has a current sense monitoring feature. A resistor connected from the CS (current sense) pin to VIN indicates voltage proportional to the output load current. A detailed description of this feature is provided in Programmable Current Limit (PCL) section.

In order to provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in Figure 33. Detailed parallel operation is provided in the Current Sharing section.

An enable feature is incorporated in the design allowing one to enable or disable the LDO. Power Good, an open drain connection, indicates the status of the output voltage. These provide the customers system flexibility in monitoring and controlling the LDO operation. When using Enable function, V_{IN} voltage must be greater than 3.5 V. For V_{IN} from 1.5 V to 7 V, TPS7H1101 can be disabled using SoftStart (SS) pin as described in Enable/Disable section.

TPS7H1201 Overview

The TPS7H1201 is a 0.5A , 1.5-V to 7-V low dropout (LDO) linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high thermal performance in a 16-pin ceramic flatpack package (HKS) or KGD (Bare Die) package.

A number of features are incorporated in the design to provide high reliability and system flexibility. Overload protection is incorporated in the design to make it viable for harsh environments.

A resistor connected from programmable current limit (PCL) pin to ground sets the current limit activation point. When current limit activation point is reached, output voltage drops while output load current is maintained at current limit point.

The device also has a current sense monitoring feature. A resistor connected from the CS (current sense) pin to VIN indicates voltage proportional to the output load current. A detailed description of this feature is provided in Programmable Current Limit (PCL) section.

In order to provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in Figure 33. Detaled parallel operation is provided in the Current Sharing section.

An enable feature is incorporated in the design allowing one to enable or disable the LDO. Power Good, an open drain connection, indicates the status of the output voltage. These provide the customers system flexibility in monitoring and controlling the LDO operation. When using Enable function, V_{IN} voltage must be greater than 3.5 V. For V_{IN} from 1.5 V to 7 V, TPS7H1201 can be disabled using SoftStart (SS) pin as described in Enable/Disable section.

TYPICAL CHARACTERISTICS (TPS7H1201-HT)

Feedback Voltage vs. Temperature

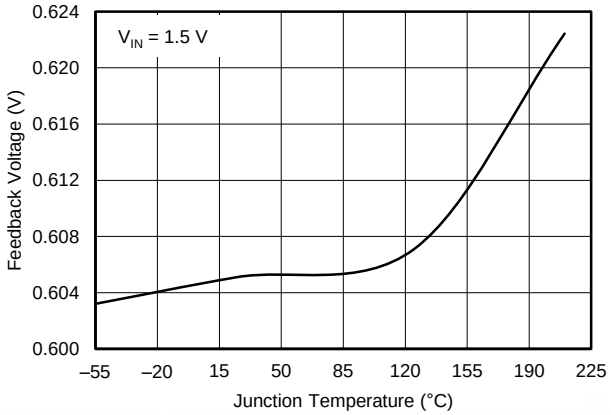


Figure 2.

Quiescent Current vs. Temperature

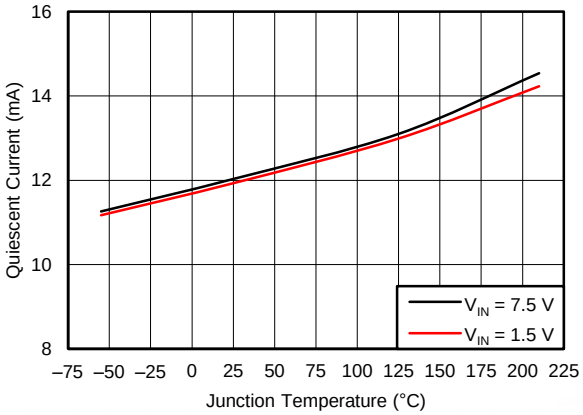


Figure 3.

Ground Current vs. Temperature

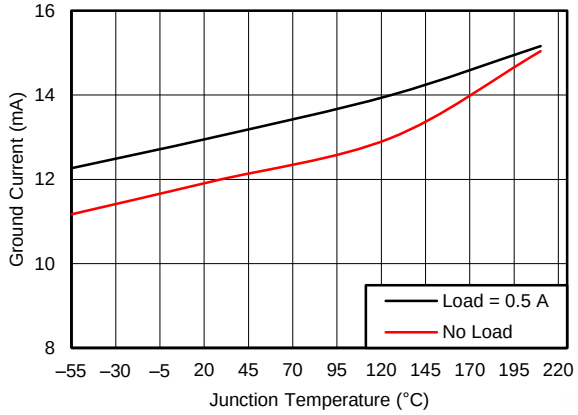


Figure 4.

Dropout Voltage vs. Temperature

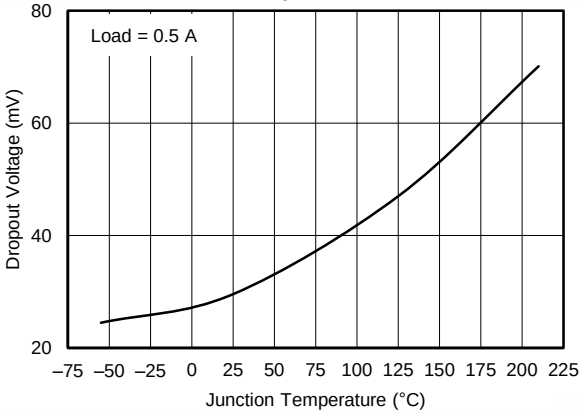


Figure 5.

Shutdown Current vs. Temperature

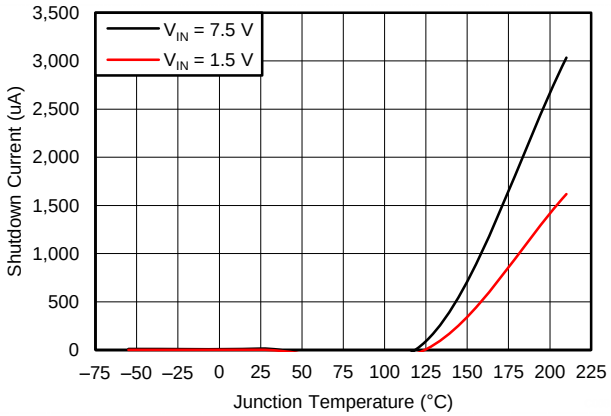


Figure 6.

PG Threshold vs. Temperature

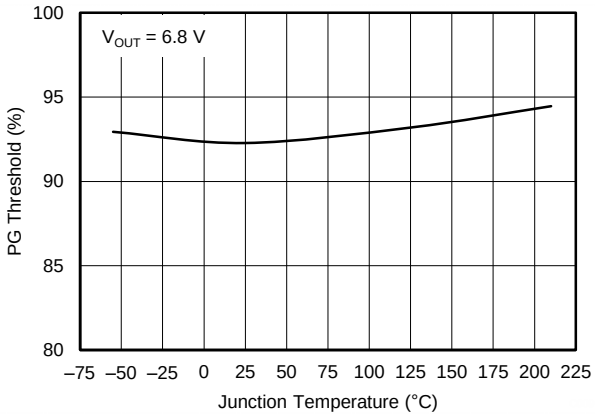


Figure 7.

TYPICAL CHARACTERISTICS (TPS7H1201-HT) (continued)

Power Supply Ripple Rejection vs. Frequency I_{OUT} = 250 mA

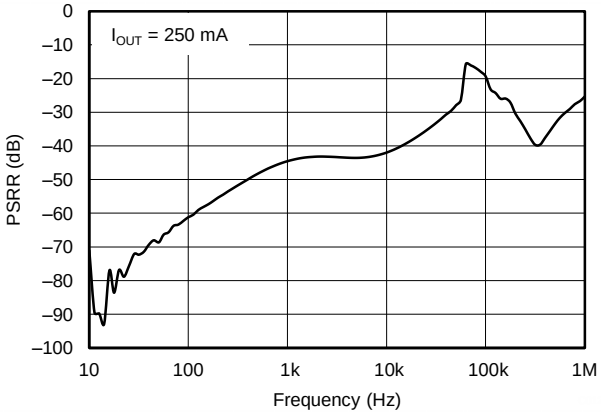


Figure 8.

Power Supply Ripple Rejection vs. Frequency I_{OUT} = No Load

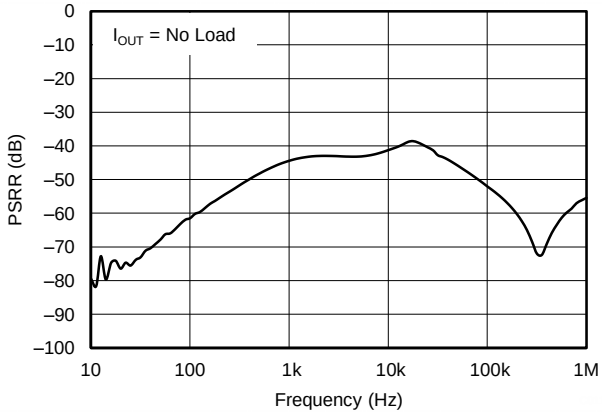


Figure 9.

Load Regulation vs. Temperature

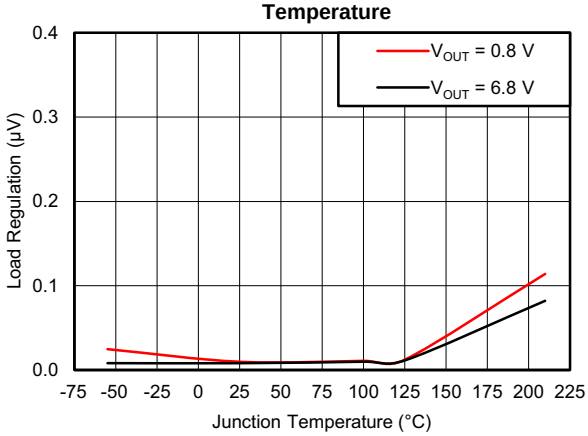


Figure 10.

TYPICAL CHARACTERISTICS (TPS7H1101-SP)

Feedback Voltage vs. Temperature

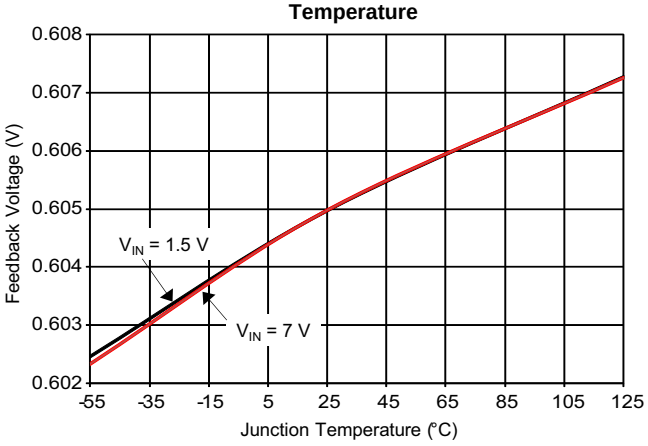


Figure 11.

Quiescent Current vs. Temperature

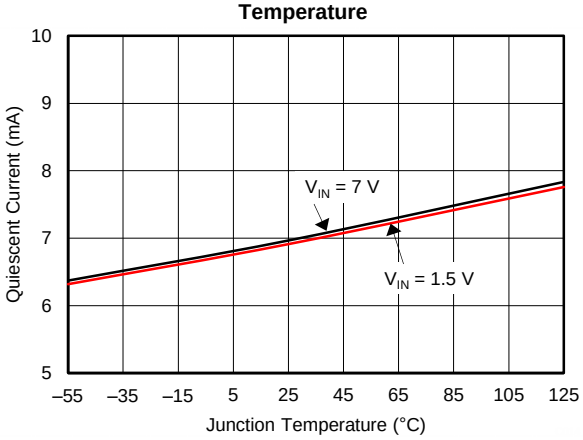


Figure 12.

Ground Current vs. Temperature

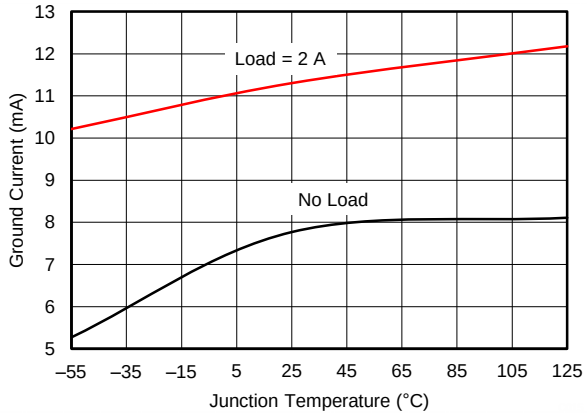


Figure 13.

Dropout Voltage vs. Temperature

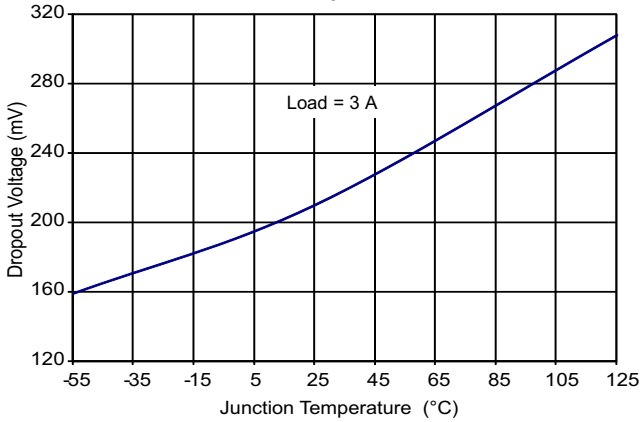


Figure 14.

Shutdown Current vs. Temperature

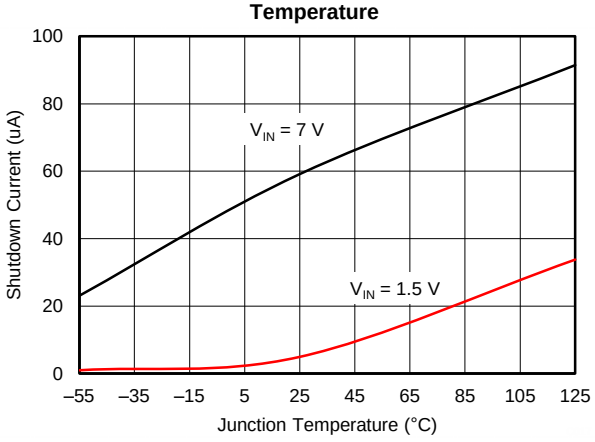


Figure 15.

PG Threshold vs. Temperature

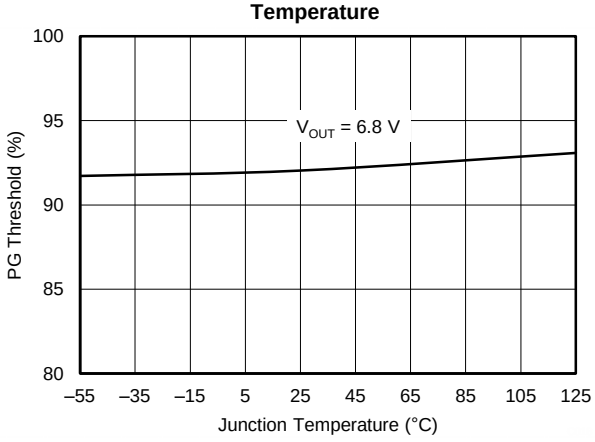


Figure 16.

APPLICATION INFORMATION

Adjustable Output Voltage (Feedback Circuit)

The Output voltage of the TPS7H1101-SP can be set to user programmable level between 0.8 V and 6.65 V. The Output voltage of the TPS7H1201-HT can be set to user programmable level between 0.8 V and 6.8 V. This can be achieved by using a resistor divider connected between V_{OUT}, FB and GND pins. R_{TOP} connected between V_{OUT} and V_{FB} and R_{BOTTOM} being connected between V_{FB} and GND.

V_{OUT} can be determined by using Equation 1.

$$V_{OUT} = \frac{(R_{TOP} + R_{BOTTOM}) \bullet V_{FB}}{R_{BOTTOM}} \quad (1)$$

Where V_{FB} = 0.605 V.

Table 3. Resistor Values for Typical Voltages

V_{OUT}	R_{TOP}	R_{BOTTOM}
0.8 V	10 kΩ	30.1 kΩ
1 V	10 kΩ	15 kΩ
1.2 V	10 kΩ	10 kΩ
1.5 V	15 kΩ	10 kΩ
1.8 V	20 kΩ	10 kΩ
2.5 V	32 kΩ	10.1 kΩ
3.3 V	45.9 kΩ	10.2 kΩ
4 V	59 kΩ	10.4 kΩ
5 V	77.7 kΩ	10.6 kΩ
5.5 V	78.7 kΩ	9.65 kΩ
6 V	78.7 kΩ	8.75 kΩ
6.5 V	78.7 kΩ	7.96 kΩ
6.6 V	79.6 kΩ	7.96 kΩ
6.7 V	78.7 kΩ	7.77 kΩ

Programmable Current Limit (PCL)

Programmable current limit resistor, R_{pcl}, sets the over current limit activation point and can be calculated per

R_{pcl} = (CSR * V_{ref})/ (I_{CL} - 0.0403),

Where V_{ref} = 0.605 V, I_{CL} = programmable current limit (A) and Current Sense Ratio (CSR) is the ratio of Output Load Current to I_{CS}.The typical value of the CSR is 47394.

Figure 17 shows the the Output Load Current (I_{OUT}) versus PCL pin current (I_{CL})

A suitable resistor R_{pcl} must be chosen to ensure the CS pin is within its operating range of 0.3 V to VIN.

For TPS7H1201-HT, the maximum programmable current limit is 700 mA. The range of resistor that can be used on the PCL pin to GND is 47 kΩ to 160 kΩ.

For TPS7H1101-SP, the maximum programmable current limit is 3.5 A. The range of resistor that can be used on the PCL pin to GND is 8.2 kΩ to 160 kΩ.

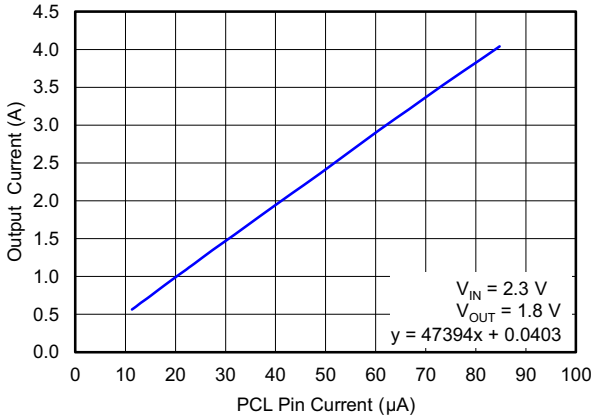


Figure 17. I_{OUT} (A) vs I_{PCL} (µA)

High Side Current Sense

Figure 18 shows the Cascode NMOS current mirror. V_{cs} must be in the range as specified in the Electrical Characteristics table. The example below shows typical calculation of R_{cs}.

$$I_{CS} = \frac{I_{LOAD} + V_{offset}}{CSR} \quad (2)$$

$$R_{CS} = \frac{V_{IN} - V_{CS}}{I_{CS}} \quad (3)$$

I_{LOAD} is the output load current

CSR is the current sense ratio

When V_{in} = 2.3 V, select V_{CS} = 2.05 V, I_{LOAD} = 3 A, CSR = 47394, and V_{offset} = 0.1899 A, then I_{CS} = 67.306 µA and R_{CS} = 3.714 kΩ.

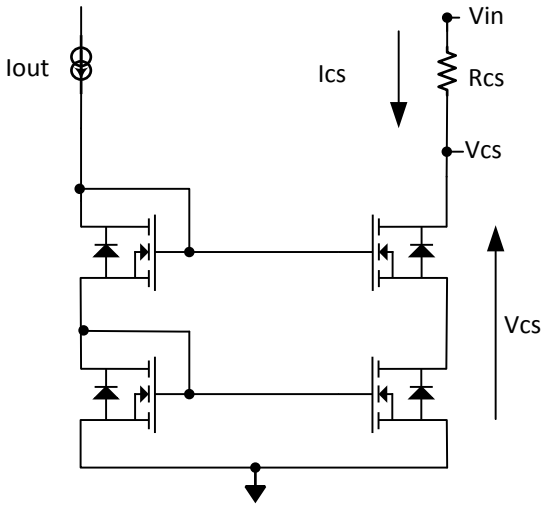


Figure 18. Cascode NMOS Current Mirror

For TPS7H1101-SP, Figure 21 shows typical curve V_{CS} vs I_{OUT} for Vin = 2.28 V and R_{CS} = 3.65 kΩ. A resistor connected from current sense (CS) pin to V_{IN} indicates voltage proportional to the output current.

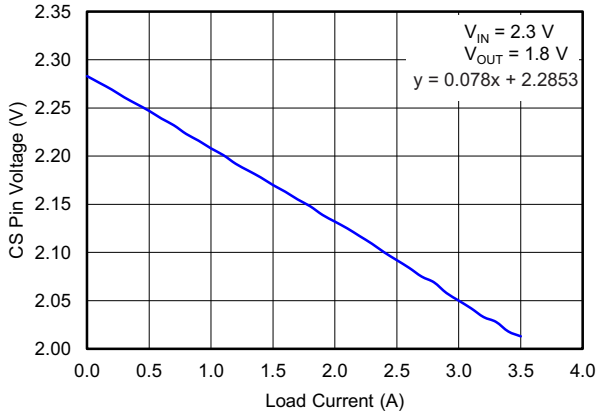


Figure 19. V_{CS} (V) vs I_{OUT} (A) (TPS7H1101-SP)

Monitoring current in CS pin (I_{CS} vs I_{OUT}) indicates the current sense ratio (CSR) between the main PMOSFET and the current sense MOSFET as shown in Figure 22.

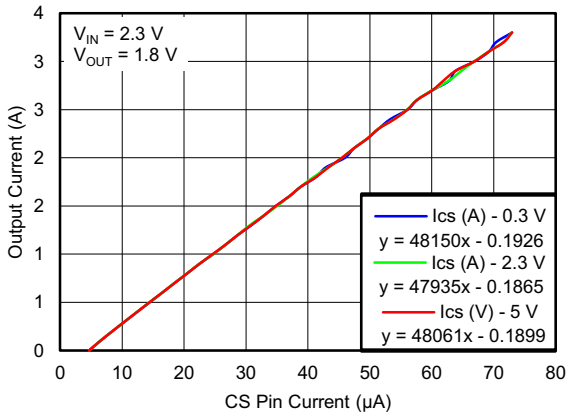


Figure 20. I_{OUT} (A) vs I_{CS} (A) (TPS7H1101-SP)

For TPS7H1201-HT, monitoring the voltage at the CS pin will indicate voltage proportional to the output current. Figure 21 shows typical curve V_{CS} vs I_{OUT} for V_{IN} = 2.28 V and R_{CS} = 3.65 kΩ.

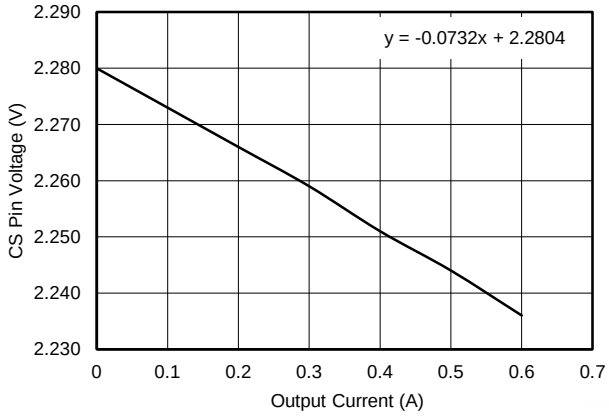


Figure 21. V_{CS} (V) vs I_{OUT} (A) (TPS7H1201-HT)

Monitoring current in CS pin (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMOSFET and the current sense MOSFET as shown in Figure 22.

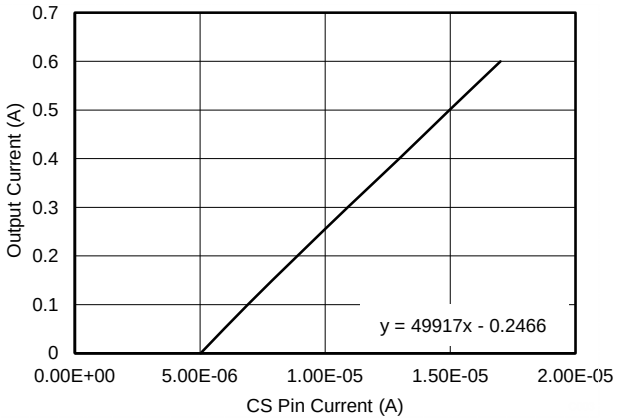


Figure 22. I_{OUT} (A) vs I_{CS} (A)

Figure 23 shows I_{OUT} vs I_{CS} when the voltage on CS pin is varied from 0.3 V to 7 V.

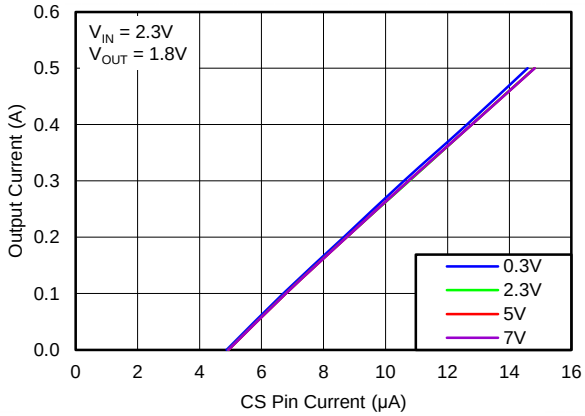


Figure 23. I_{OUT} (A) vs I_{CS} (A) (TPS7H1201-HT)

Current Foldback

1. The TPS7H1101-SP has Current Foldback feature which can be enabled when Current Sense (CS) pin is held high, Shorting CS low will disable the foldback current limit.
2. With foldback current limit enabled, when current limit trip point is activated,

   (a) Output voltage will drop low
   (b) output current will fold back to approx. 50% of the current limit trip point.
   This results in minimizing the power loss under fault conditions. Monitoring the voltage at the CS pin will indicate voltage proportional to the output current.

Power Good (PG)

Power Good pin (9) is an open drain connection and can be used to sequence multiple LDOs. Figure 24 shows typical connection. As shown, maximum voltage at PG pin must be limited to less than 1.2 V in order not to forward bias the internal MOSFET diode of PMOS current mirror circuitry.

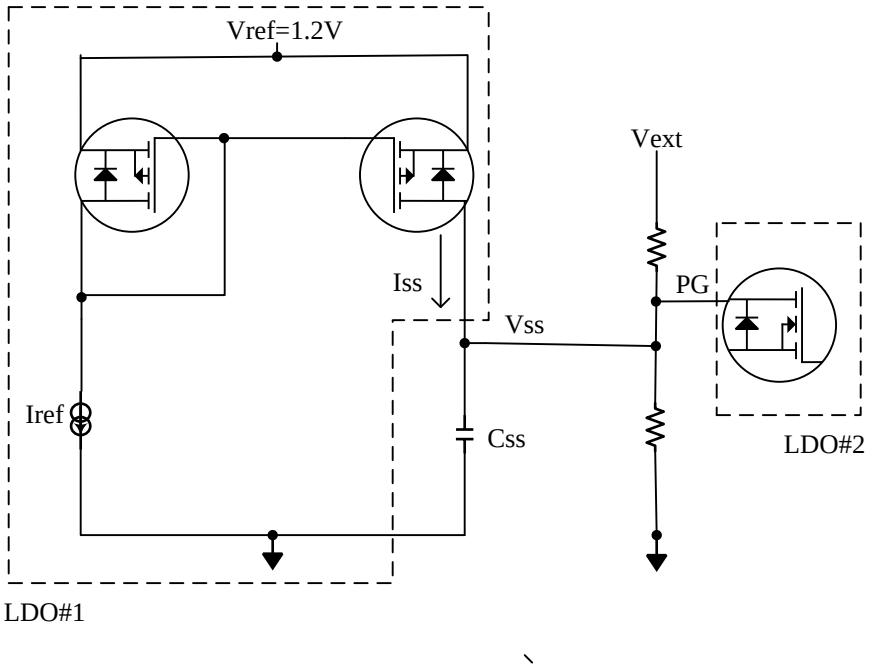


Figure 24. Sequencing LDO#1 by Power Good signal of LDO#2

Transient Response

For TPS7H1101-SP, waveforms below indicate the transient response behavior of the LDO for 50% step load change.

Channel 1: Output voltage overshoot / undershoot

Channel 2: Step load in current

Channel 3: Input voltage

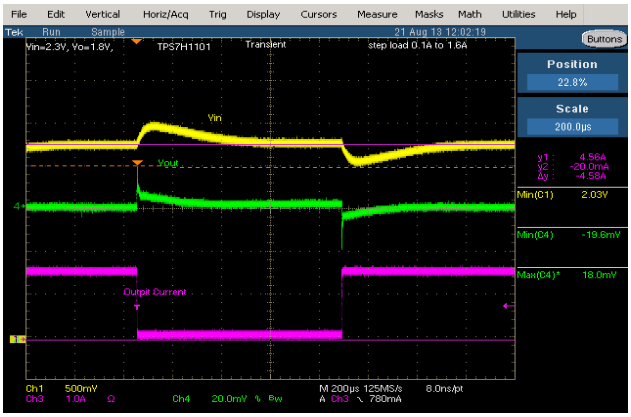


Figure 25. Load Transient Response:
Step Load 0.1 A to 1.6 A, V_{IN} = 2.3 V, V_{OUT} = 1.8 V (TPS7H1101-SP)

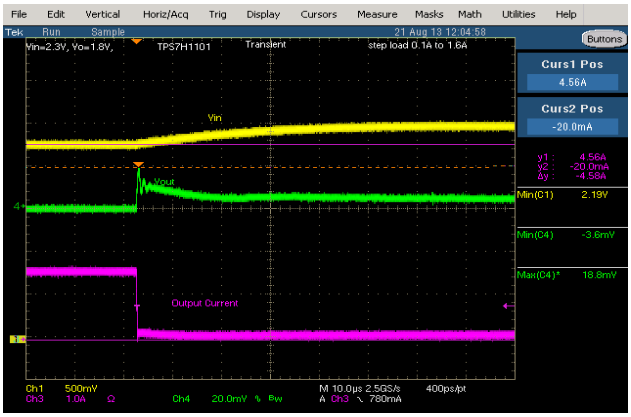


Figure 26. Expanded View Overshoot

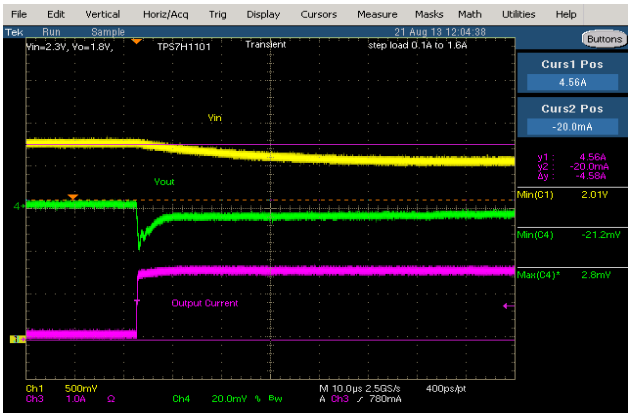


Figure 27. Expanded View Undershoot

Waveforms below indicate the transient response behavior of the TPS7H1201-HT.

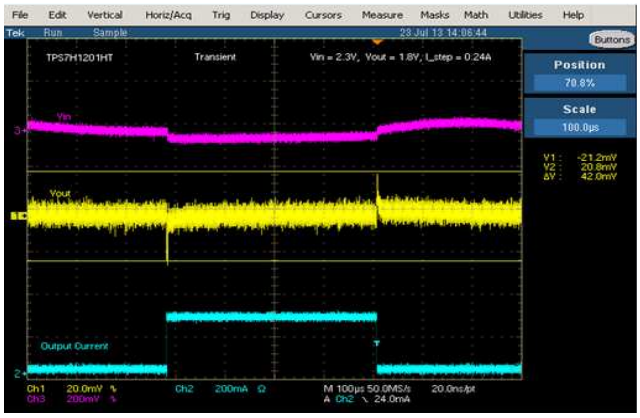


Figure 28. Load Transient Response: Step Load 0 A to 250 mA, V_{IN} = 2.3 V, V_{OUT} = 1.8 V (TPS7H1101-SP)

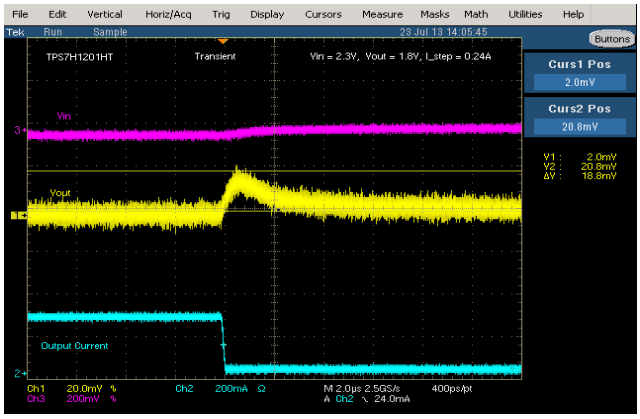


Figure 29. Expanded View Overshoot

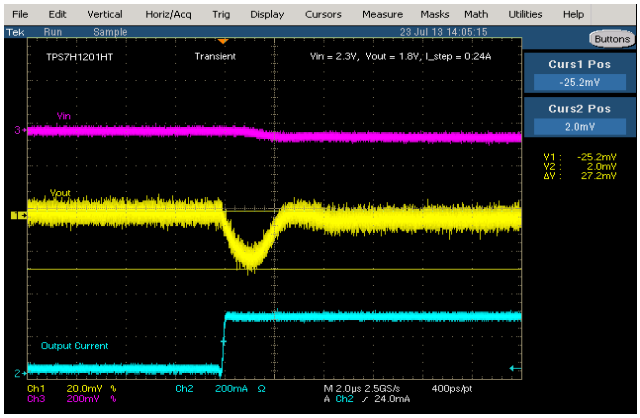


Figure 30. Expanded View Undershoot

Current Sharing

For demanding load requirements, multiple LDOs can be paralleled as indicated in Figure 33 below. In parallel mode CS pin of LDO#1 must be connected to PCL pin of LDO#2 via a series resistor R_{CL} and CS pin of LDO#2 must be connected to PCL pin of LDO#1 via series resistor R_{CL}. Typical value of R_{CL} in parallel operation is 3.75Kohm for current limit > 6A. In parallel configuration, R_{CL} (resistor from PCL to GND) and R_{CS} (resistor from CS pin to V_{IN}) must be left open (unpopulated). The R_{CL} value needs to be selected so that the operating condition of CS pin is maintained, as specified in the electrical characteristics table. The current from PCL through RCL of LDO1 is determined by the output load current of LDO2 divided by the Current Sense Ratio (CSR). Hence, the voltage at CS pin of the LDO1 is 0.605 V – ((output load current of LDO2 + 0.2458) / CSR * R_{CL}). Typical Value of R_{CL} is 3.65 Kohm. This parallel configuration will provide higher reliability (MTBF) for system needs due to reduced stress on the components, as the load current will be shared between the two LDOs.

Alternately, it can also provide twice the output current to meet system needs. When using two LDOs in parallel operation for higher output load current, use POL TPS50x01 as an input source.

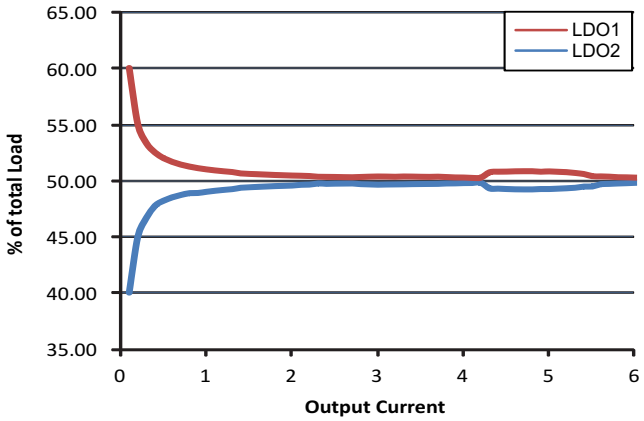


Figure 31. LDO Current Share (TPS7H1101-SP)

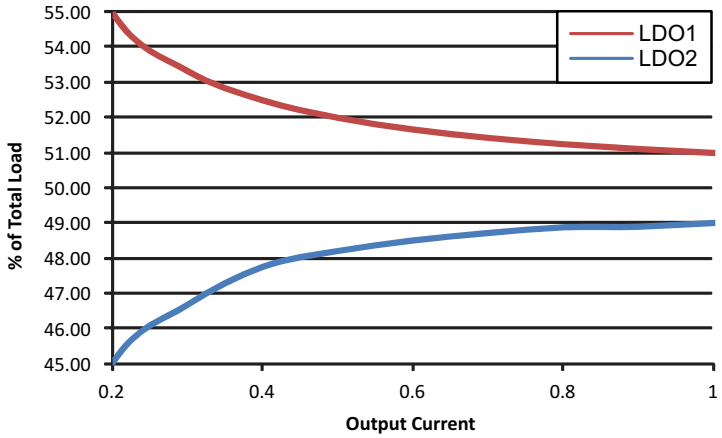


Figure 32. LDO Current Share (TPS7H1201-HT)

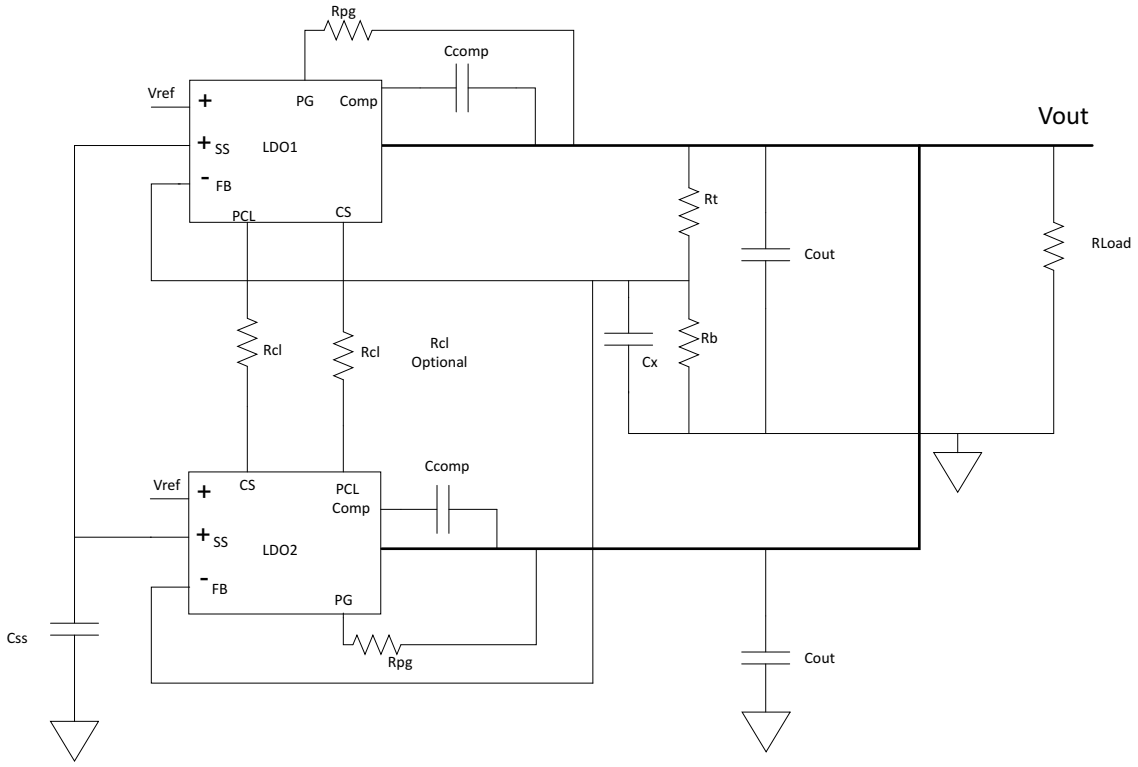


Figure 33. Functional Block Diagram (Parallel Operation)

Soft-Start

Connecting a capacitor on CS pin to GND (C_{SS}) slows down the output voltage ramp rate. The soft-start capacitor will charge up to 1.2 V.

$$C_{SS} = \frac{t_{SS} \bullet I_{SS}}{V_{FB}} \tag{4}$$

Where:

t_{ss} = Soft-start time

I_{ss} = 2.5 µA

$V_{FB} = V_{REF} / 2 = 0.605$ V

Enable/Disable

For Vin from 1.5 V to 7 V, TPS7H1x01 can be disabled using SoftStart (SS) pin. The minimum Soft-start pull down current is 10 µA, with soft-start to ground voltage of 400 mV or lower. External voltage applied to SoftStart (SS) pin must be limited to 1.2 V maximum. Removing the logic low condition on Soft-tart shall enable the device allowing the Soft-start capacitor to get charged by the internal current source. Alternatively, for V_{IN} greater than 3.5 V, the device can be disabled by pulling the enable pin to logic low. In all other cases, the enable pin should be connected to V_{IN}.

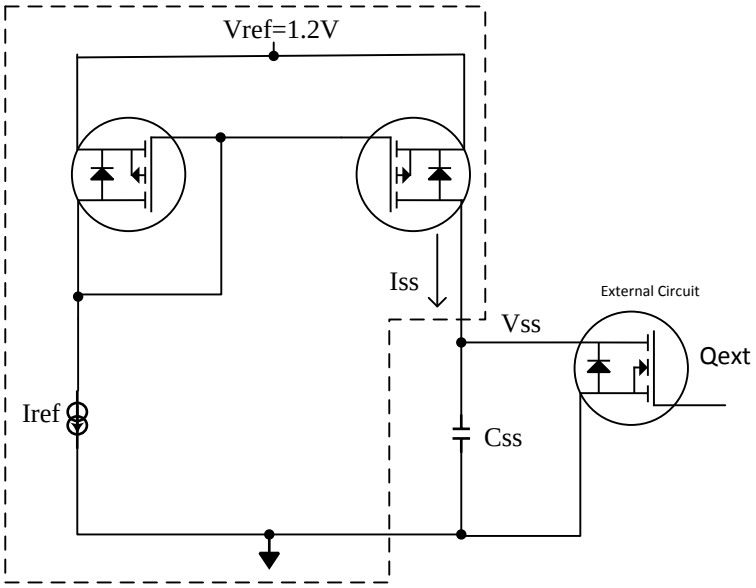


Figure 34. Enable/Disable

Circuit shown in Figure 34 highlights the Soft-start (SS) pin 1 along with block diagram of internal circuitry. Circuitry in dashed outline is internal to the IC composed of PMOSFET current mirror. PMOS current mirror sources current from the positive supply and external circuitry composed of Q_{ext} is used to sink current from SS pin 1. As highlighted in Electrical Characteristic table – typical I_{SS} = 2.5 µA and max I_{SS} = 3.5 µA for TPS7H1101-SP. If I_{SS} current is exceeded, such as sinking higher current in excess of max I_{SS}, this will disable the LDO.

External sink current from SS pin to guarantee disabling the IC is as indicated in the Electrical Characteristic table. Exceeding maximum external sink current will not damage the device.

Compensation

Generic block diagram for TPS7H1101-SP LDO with external compensation components is highlighted below in Figure 35. LDO incorporates nested loops, thus providing high gain necessary to meet design performance.

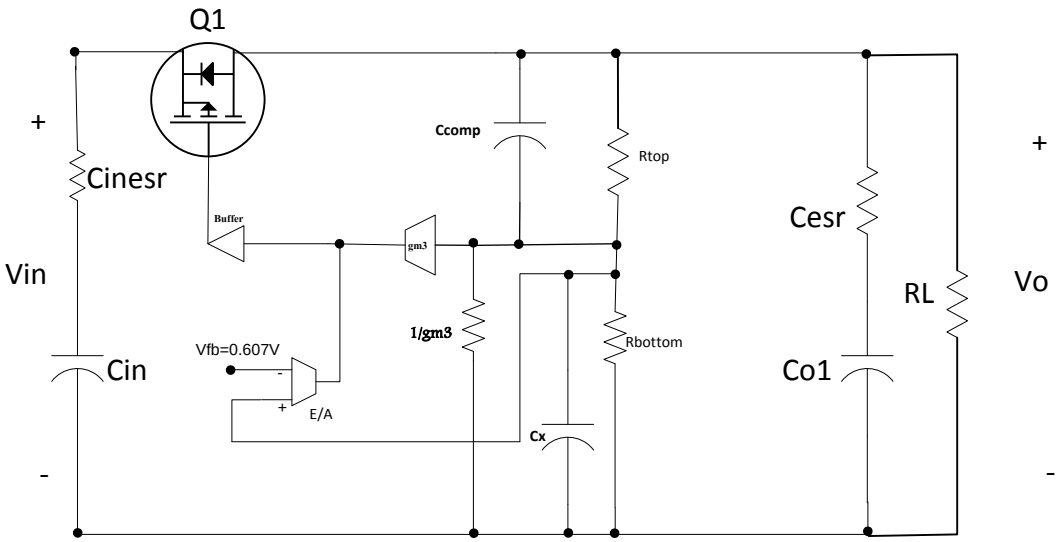


Figure 35. TPS7H1101-SP Compensation

Resistor divider composed of R_{top} and R_{bottom} will determine the output voltage set points as indicated by Equation 1.

Output capacitor C_{OUT} introduces a pole and a zero as shown below.

$$F_{p\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet R_L} \quad (5)$$

$$F_{z\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet C_{esr}} \quad (6)$$

C_x introduces a pole to the feedback loop and should be selected to compensate for the output capacitor zero, F_{z_co}.

$$F_p = \frac{1}{2 \bullet \pi \bullet C_x \bullet R_{bottom}} \quad (7)$$

C_x is calculated to be 1000 pF for C_o = 220 µF, C_{esr} = 45 mΩ.

Internal compensation in the LDO cancels the output capacitor pole introduced by C_{OUT} and R_L.

C_{comp} introduces a dominant pole at low frequency. It is recommended that a C_{comp} value of 10 nF be selected that will be valid for all line and load conditions.

Output Noise

Output noise is measured using HP3495A. Plots below shows noise of the TPS7H1101-SP and TPS7H1201-HT in µV/√Hz vs Frequency

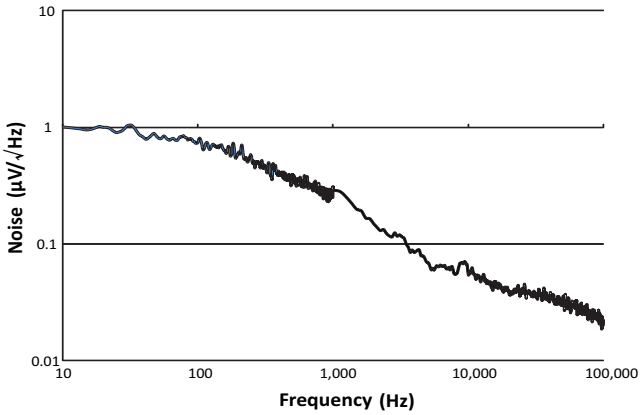


Figure 36. TPS7H1101-SP - RMS Noise (10 Hz - 100 kHz) = 20.33 µVrms, V_{IN} = 2 V, V_{OUT} = 1.8 V at 3 A, , C_{IN} = 220uF, C_{LOAD} = 220uF

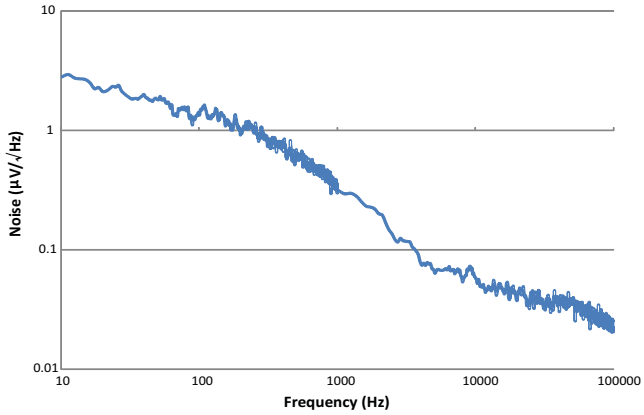


Figure 37. TPS7H1101-SP - RMS Noise (10 Hz - 100 kHz) = 31.68 µVrms, V_{IN} = 7 V, V_{OUT} = 6.7 V at I_{load} = 3 A, C_{IN} = 220 uF, C_{LOAD} = 220 uF

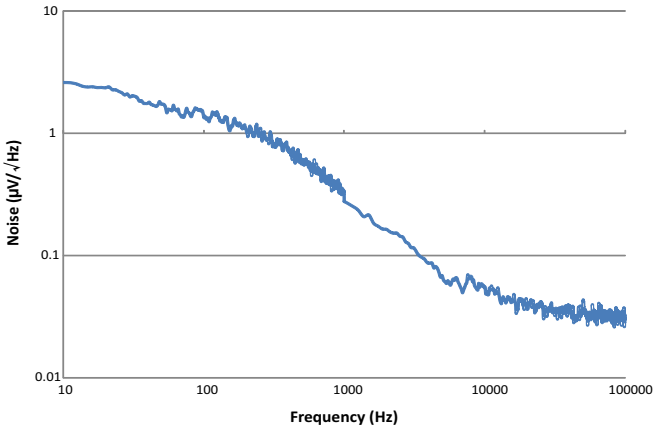


Figure 38. TPS7H1201-HT - RMS Noise (10 Hz - 100 kHz) = 20.26 µVrms, V_{IN} = 2.1 V, V_{OUT} = 1.8 V at I_{load} = 0.5 A, C_{IN} = 220 uF, C_{LOAD} = 220 uF

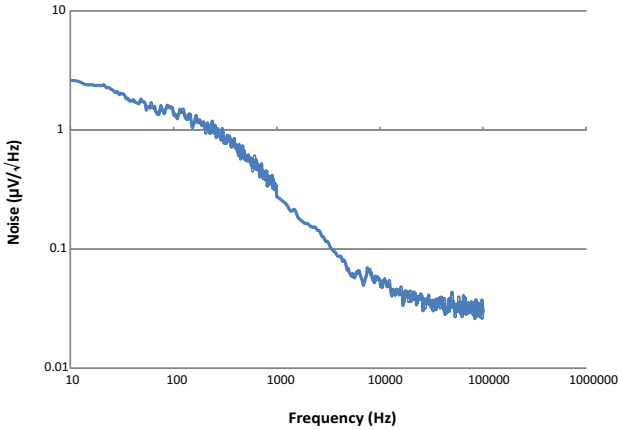


Figure 39. TPS7H1201-HT - RMS Noise (10 Hz - 100 kHz) = 31 µVrms, V_{IN} = 7 V, V_{OUT} = 6.7 V at I_{load} = 0.5 A, C_{IN} = 220 uF, C_{LOAD} = 220 uF

Capacitors

TPS7H1X01 requires the use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. Table 4 highlights some of the capacitors used in the device. It is recommended that proper derating guidelines as recommended by capacitor manufacturer be followed based upon output voltage and operating temperature.

Note polymer based tantalum capacitors must be derated to at least 60% of rated voltage, whereas manganese oxide (MnO2) based tantalum capacitors should be derated to 33% of rated voltage depending upon the operating temperature.

It is recommended to use a tantalum capacitor along with a 0.1µF ceramic capacitor for improved performance. The device is stable for input and output tantalum capacitor values of 10 µF to 220 µF with the ESR range of 10 mΩ to 2 Ω. However the dynamic performance of the device will vary based on load conditions and the capacitor values used.

It is important to ensure that good design layout practice be followed to ensure that the traces connecting V_{IN} to GND pins of LDO and V_{OUT} to GND pins of LDO should be kept short to reduce inductance. Trace length should be no longer than 5 cm.

Table 4. TPS7H1x01 Capacitors

Capacitor Part Number	Capacitor Details (Capacitor, Voltage, ESR)	Type	Vendor
T493X107K016CH612A(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
T493X226M025AH6x20(1)	22 µF, 25 V, 35 mΩ	Tantalum - MnO2	Kemet
T525D476M016ATE035(1)	47 µF, 10 V, 35 mΩ	Tantalum - Polymer	Kemet
T540D476M016AH6520(1)	47 µF, 16 V, 20 mΩ	Tantalum - Polymer	Kemet
T525D107M010ATE025(1)	100 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T541X337M010AH6720(1)	330 µF, 10 V, 6 mΩ	Tantalum - Polymer	Kemet
T525D227M010ATE025(1)	220 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T495X107K016ATE100(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
CWR29FK227JTHC(1)	220 µF, 10 V, 180 mΩ	Tantalum - MnO2	AVX
THJE107K016AJH	100 µF, 16 V, 58 mΩ	Tantalum	AVX
THJE227K010AJH	220 µF, 10 V, 40 mΩ	Tantalum	AVX
SMX33C336KAN360	33 µF, 25 V	Stacked ceramic	AVX
SR2225X7R335K1P5#M123	3.3 µF, 25 V, 10 mΩ	Ceramic	Presidio Components Inc.

(1) Operating temperature is -55°C to 125°C.

REVISION HISTORY

Changes from Revision F (October 2013) to Revision G **Page**

- Added BARE DIE INFORMATION 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1320201VXC	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 125	5962-1320201VXC TPS7H1101-SP	Samples
5962R1320201VXC	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 125	5962R1320201VXC TPS7H1101-RHA	Samples
TPS7H1101HKR/EM	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	25 Only	TPS7H1101HKREM	Samples
TPS7H1201SHKS	ACTIVE	CFP	HKS	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 210	TPS7H1201SHKS	Samples
TPS7H1201SKGD1	ACTIVE	XCEPT	KGD	0	70	TBD	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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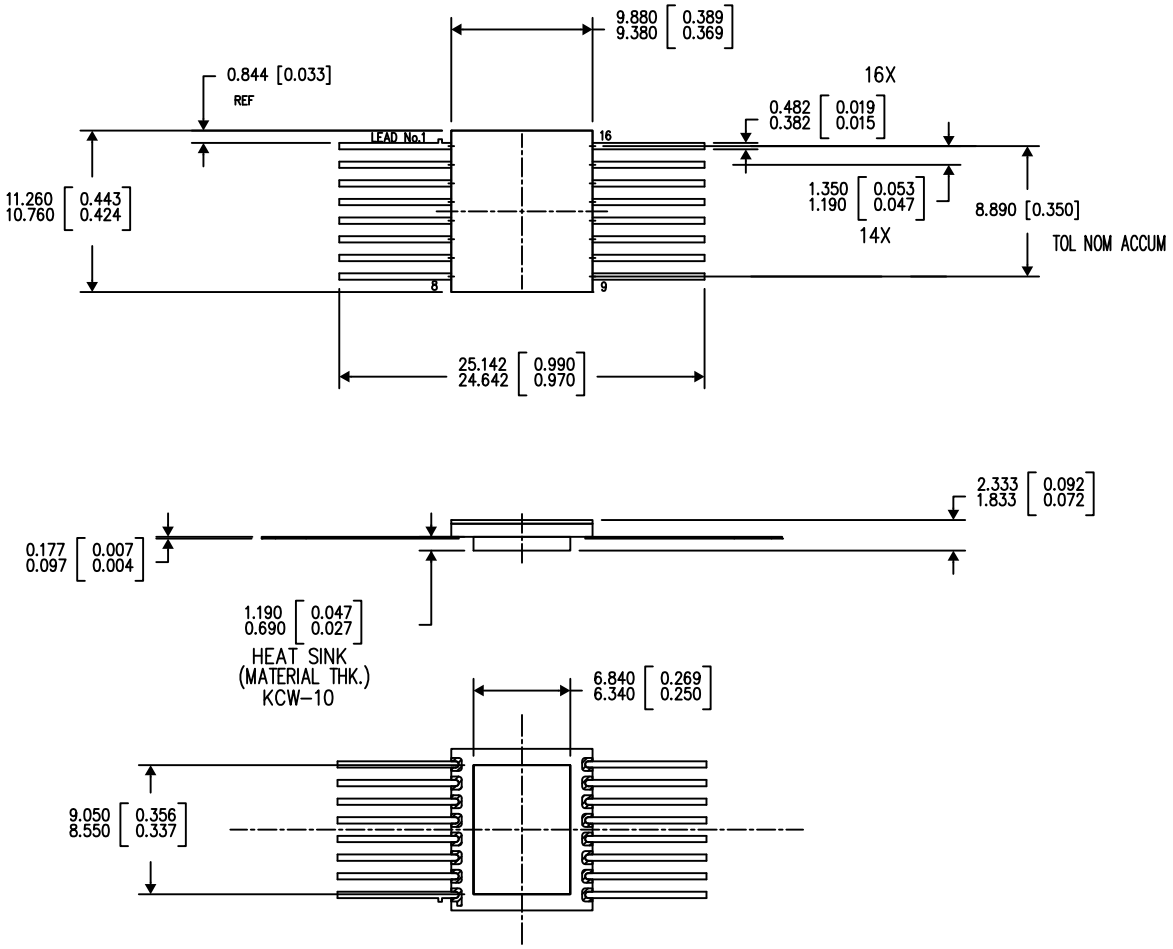
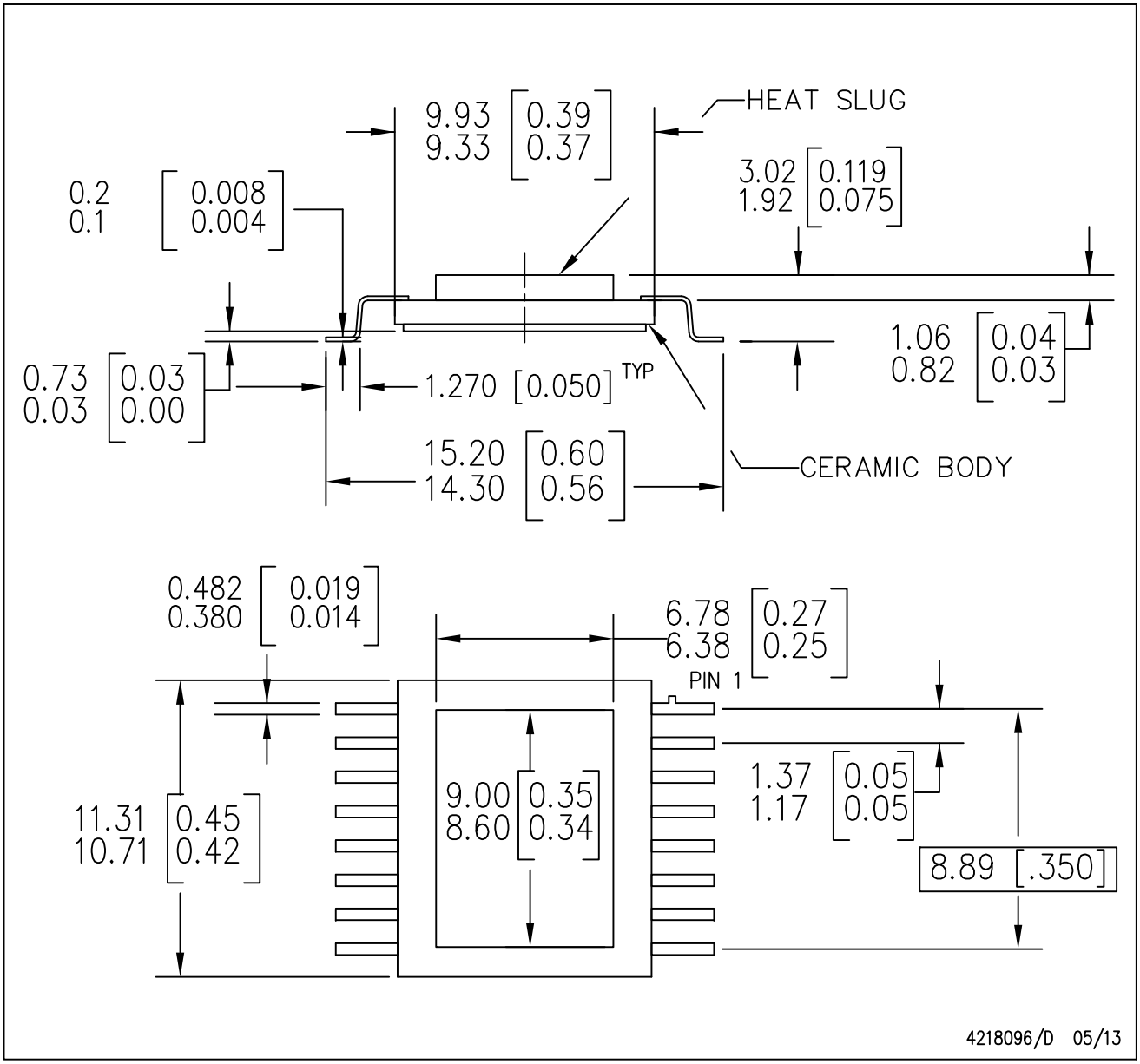


NOTES:
A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid. Lid and heat slug are connected to pin 8 (Gnd).
D. The terminals will be gold plated.

HKS (R–CDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Pin 8 is connected to lid and heat slug.

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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