Choosing Loop Bandwidth for PLLs

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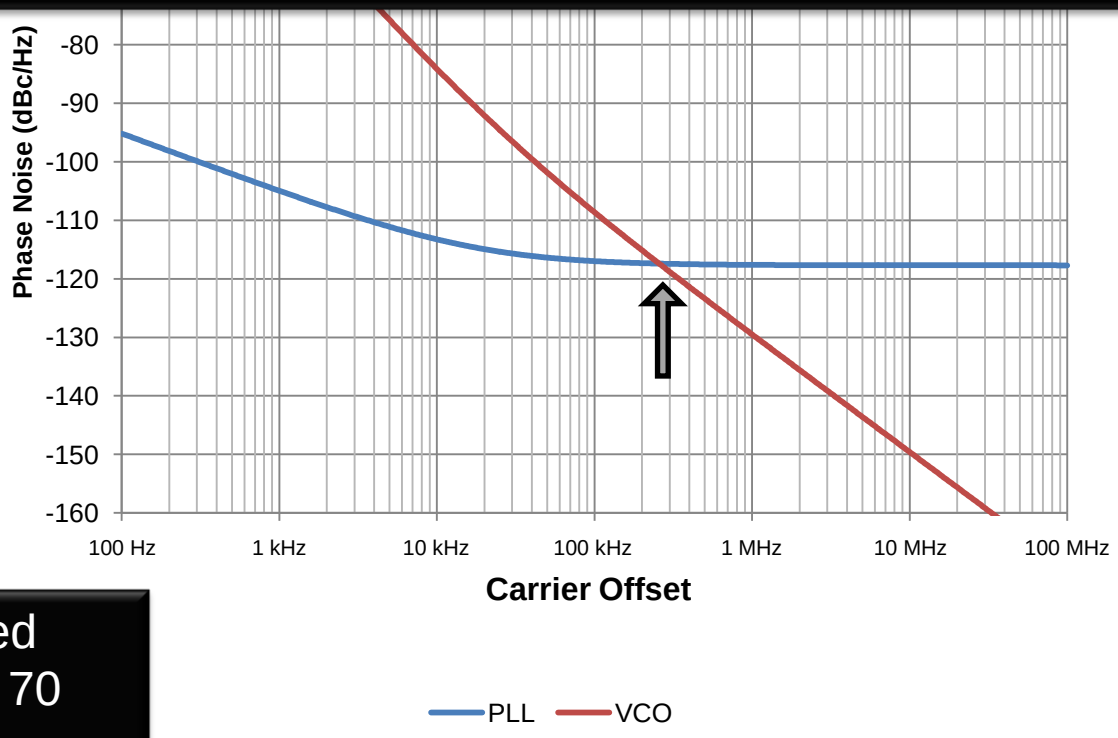
Choosing a PLL/VCO Optimized Loop Bandwidth

Starting point for setting the loop bandwidth is the offset at which the open loop VCO phase noise intercepts the open loop PLL phase noise, normalized to the VCO frequency. Keep in mind, the reference noise is included in the PLL noise.

A margin of 20% can be added to accommodate the non-ideal response of the filter.

VCO
Jitter = 28 ps rms
(100 Hz to 100 MHz)

PLL
Jitter = 980 fs rms
(100 Hz to 100 MHz)



Phase Margin for an optimized PLL/VCO loop filter is typical 70 degrees. Even higher phase margin may slightly improve jitter.

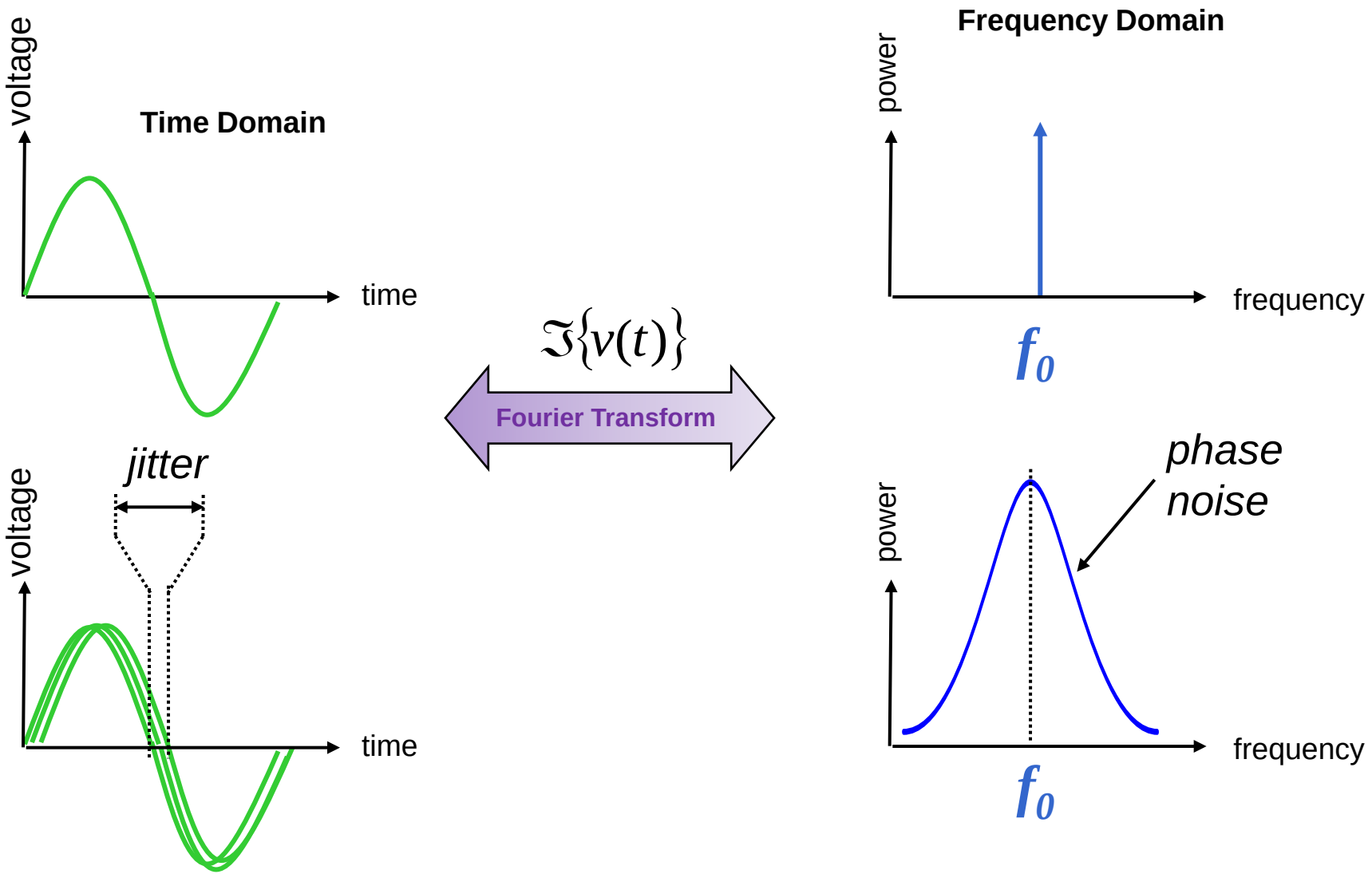
Overview

1. Noise Theory
   - Phase noise & Jitter
2. PLL Theory
   - Why a PLL?
3. Choosing PLL Loop Bandwidth
   - Optimizing noise
4. Dual Loop or Cascaded Loop Architecture
   - How dual loops help “clean jitter”
5. Determining Integration Range for Jitter Based on Customer Requirements
6. Lock time of PLL and Loop Bandwidth
   - How digital calibration impacts lock time

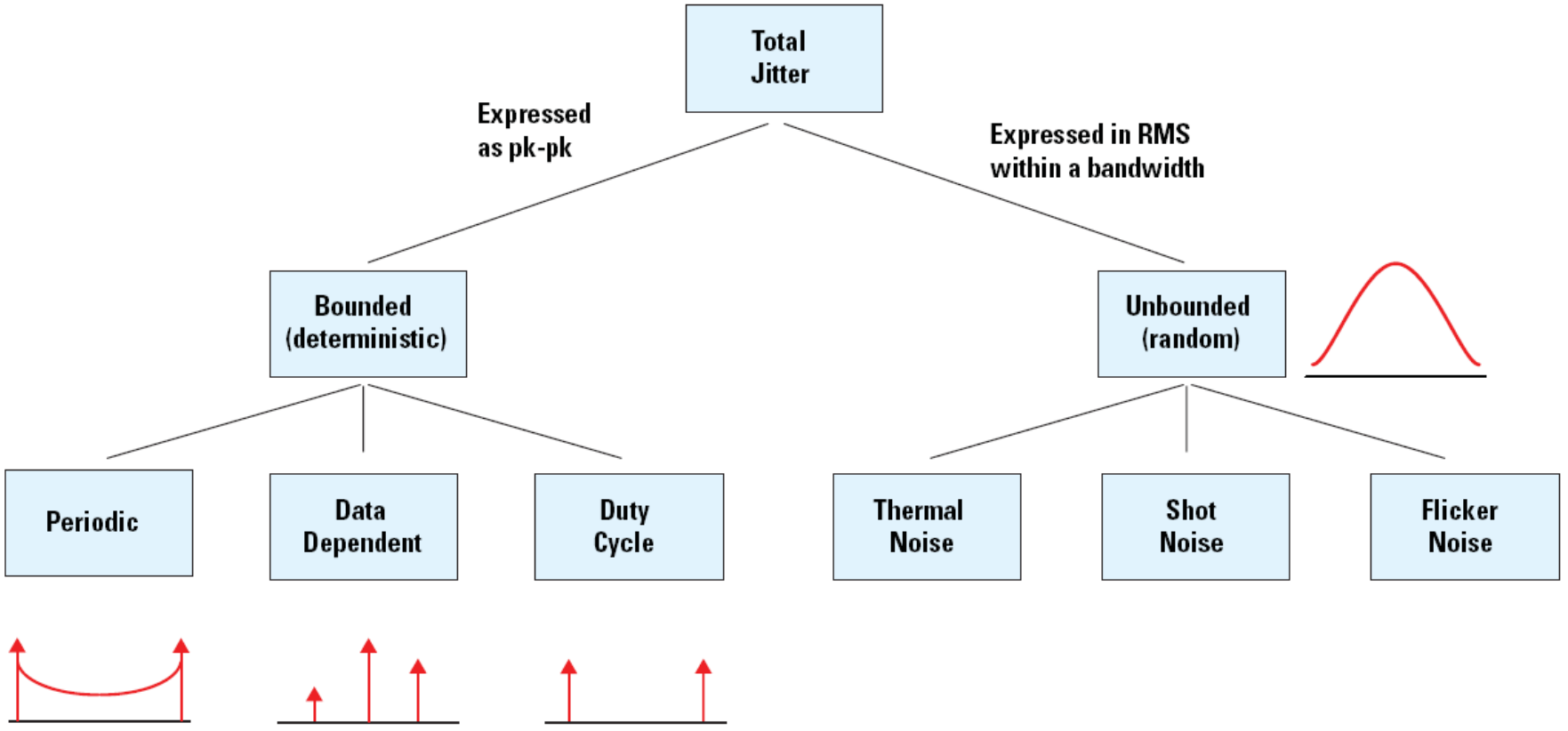
Noise Theory

- **Phase Noise**
- **Jitter**

Noise in Time and Frequency Domain



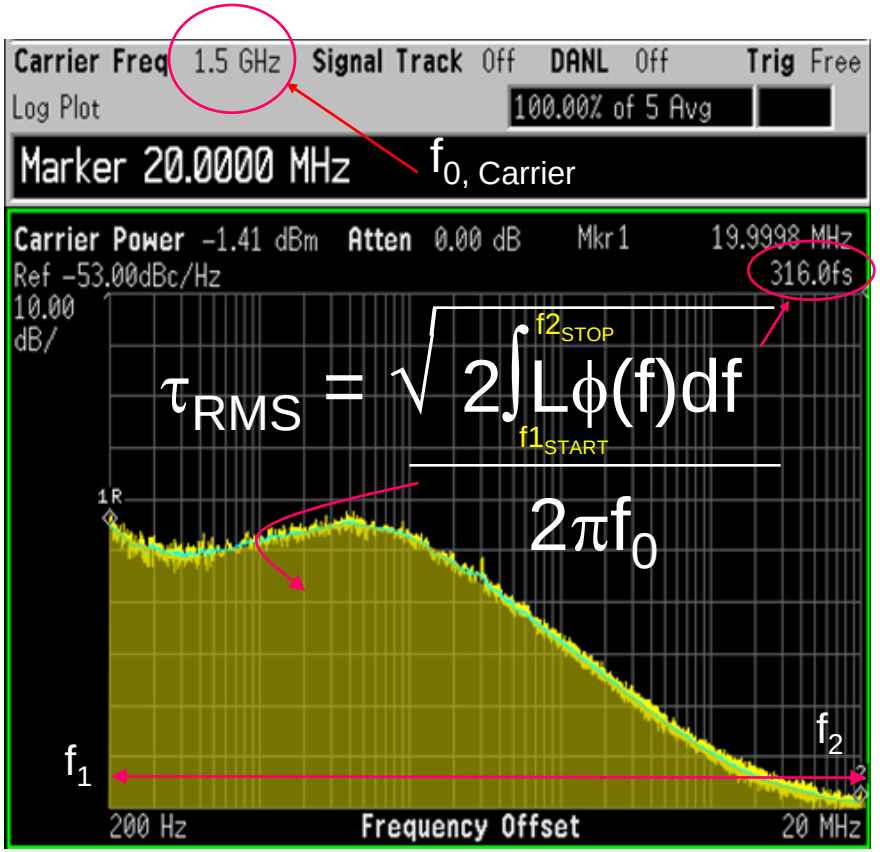
The Jitter Family Tree



Understand what type of jitter is important to the customer

Measuring Phase Noise and Jitter

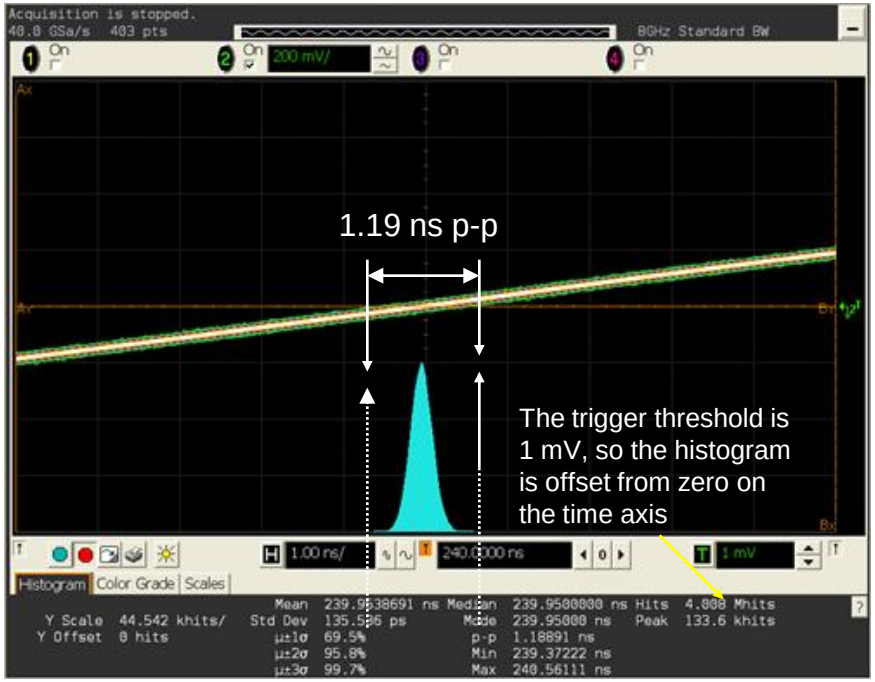
Frequency Domain Jitter Measurement



Time Domain Jitter Measurement

Not good for < 1 ps rms jitter measurements

Measurement of peak-to-peak jitter of RMS noise is a function of time.



Even 40 GS oscilloscope is not recommended for measuring 316 fs of random jitter!

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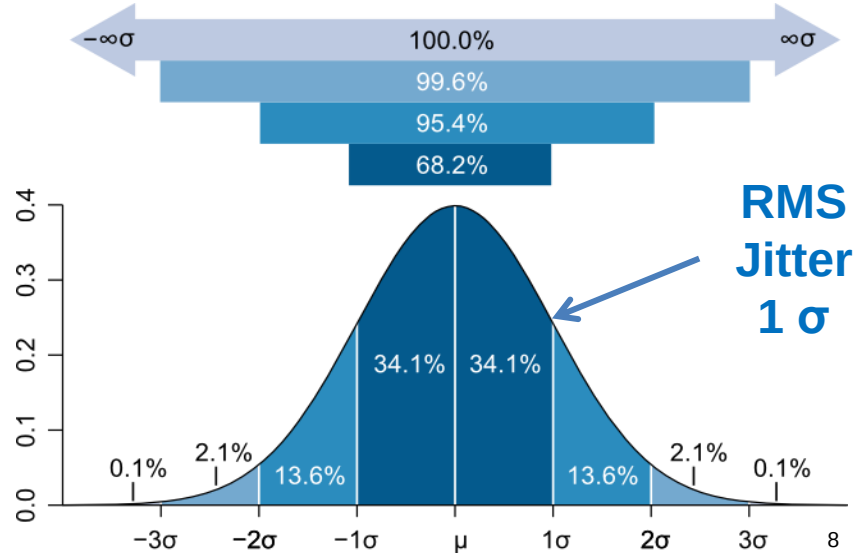
Converting from peak to peak jitter to RMS jitter or vice-versa (rule of thumb)

- Multiplier is how many standard deviations are included on a standard distribution
- (400 fs RMS) • (14.059) = 5.6 ps p-p jitter
  - The probability that the instantaneous jitter is within ± 2.8 ps is = $1 - 10^{-12}$
- If we want to specify a clock with probability ($1-10^{-15}$) that the instantaneous jitter is ≤10 ps p-p, the required RMS jitter is:

10 ps/15.883 = 630 fs RMS jitter

BER	Multiplier
$1:10^{4}$	7.438
$1:10^{6}$	9.507
$1:10^{9}$	11.996
$1:10^{11}$	13.412
$1:10^{12}$	**14.069**
$1:10^{15}$	15.883



Noise Theory – Take Aways

- From Phase Noise we can calculate Jitter, but not the other way around.

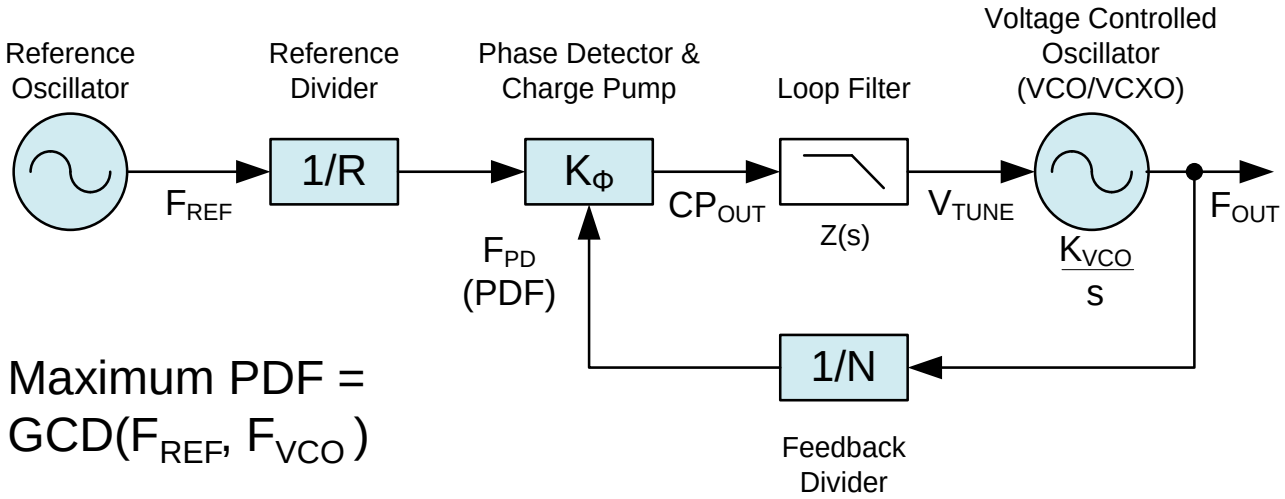
- Phase Noise quantifies noise in the frequency domain.
- Jitter quantifies noise in the time domain.
  - **An integration bandwidth must be defined for an RMS jitter measurement!**
  - Never walk away from a customer with only RMS jitter requirement and no integration bandwidth.
  - Peak to peak jitter of random noise source will increase with measurement time.

Phase Lock Loop (PLL) Theory

- Classical PLL
- Why PLL?
  - Frequency Multiplication
  - Noise Shaping
- PLL Performance

PLL Architecture

- The purpose of a PLL is to phase-lock or frequency lock two oscillators that may be operating at different frequencies.
  - Why? Frequency Accuracy. Jitter Cleaning.
- The classic PLL architecture includes:
  - Reference clock
  - Voltage controlled oscillator (VCO) with gain K_{VCO}/s
  - Reference and Feedback dividers
  - Phase detector and charge pump with gain K_ϕ
  - Loop filter [Z(s)]



Maximum PDF = GCD(F_{REF}, F_{VCO})

$$F_{PD} = \frac{F_{REF}}{R} = \frac{F_{OUT}}{N}$$

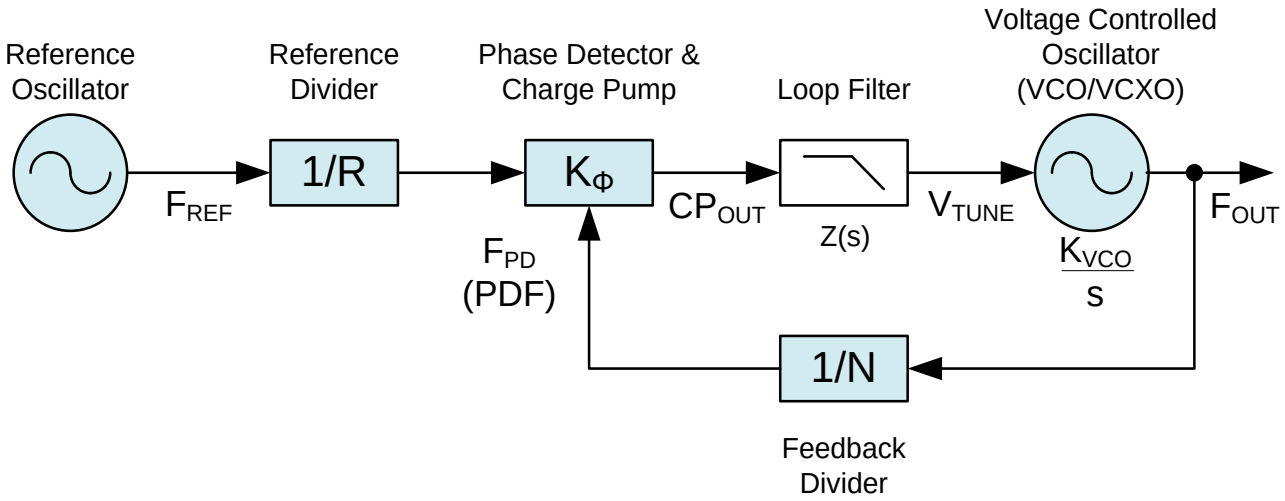
$$\therefore F_{out} = \frac{N \cdot F_{REF}}{R}$$

and

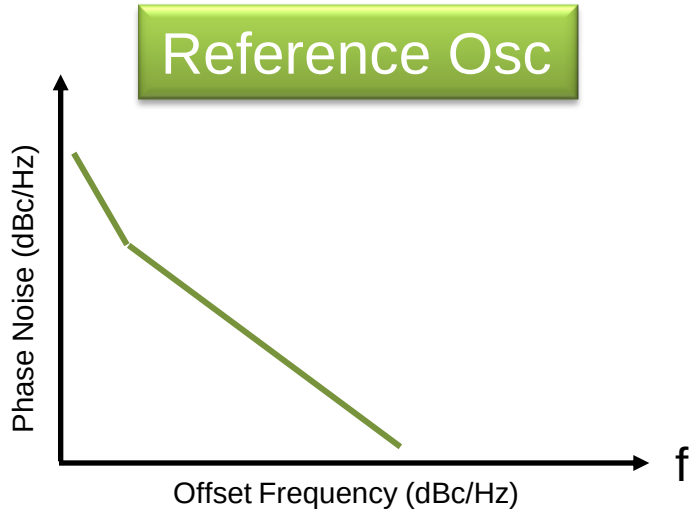
$$\frac{F_{OUT}}{F_{REF}} = \frac{N}{R}$$

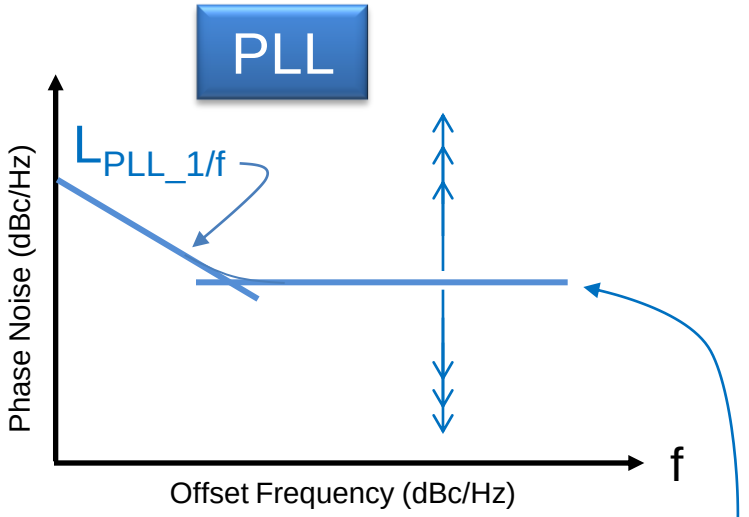
Why VCO or VCXO

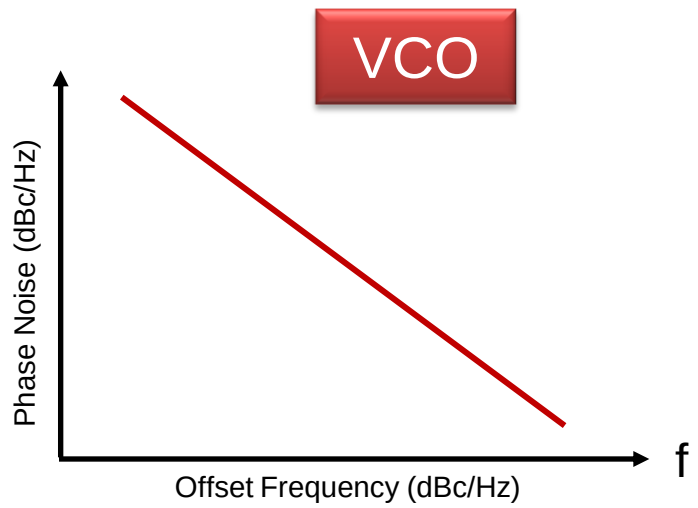
- VCO
  - Wide-band tuning
  - Poor frequency accuracy
  - High frequencies allow frequency multiplication for achieving many customer output frequencies.
- VCXO (Voltage Controlled Crystal Oscillator)
  - Very Low Noise
  - Not available at high frequencies
  - Cost increases with frequency



Open Loop Frequency Responses of Noise Sources







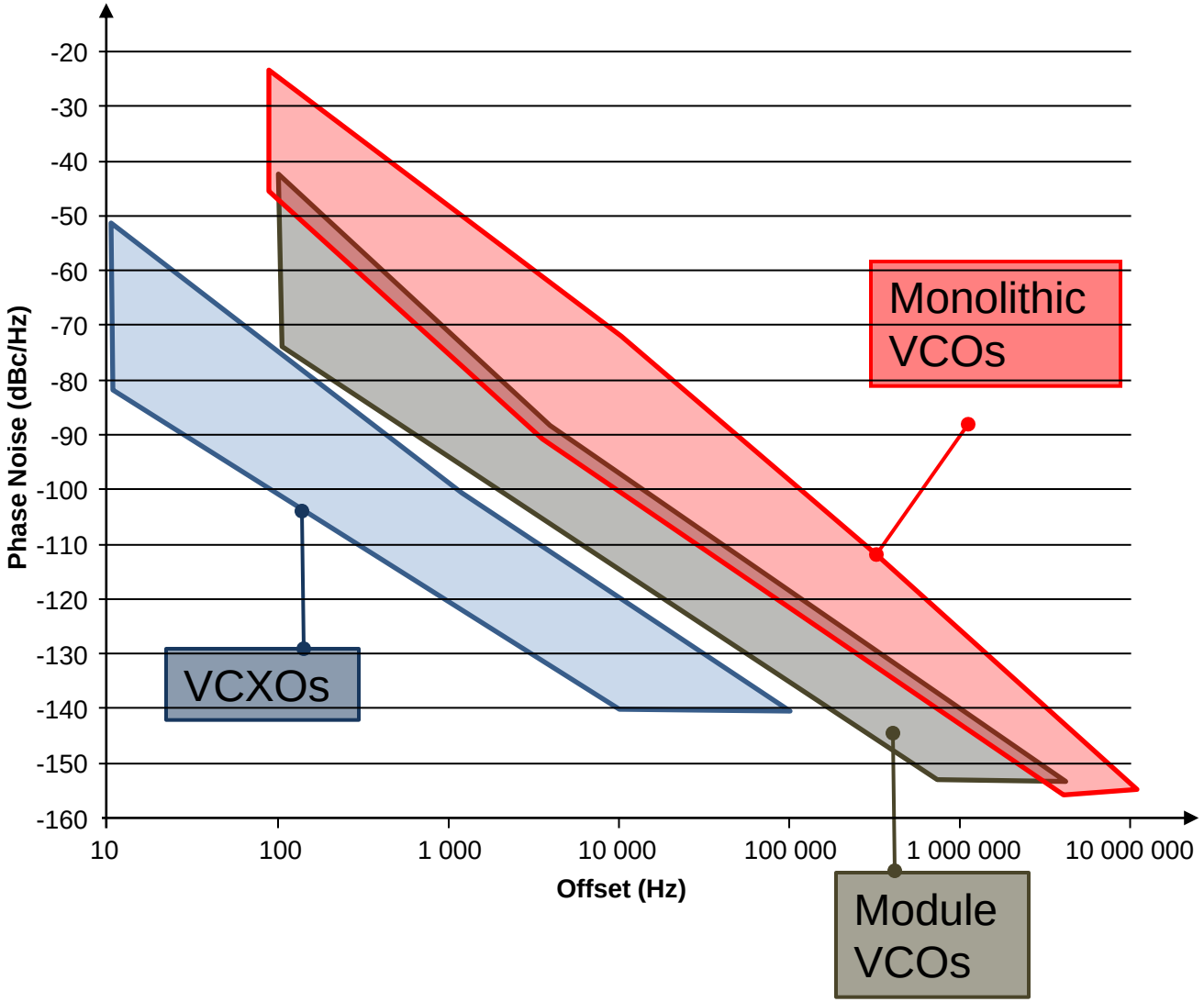
$$L_{PLL\_flat}(f) = PN1Hz + 20 \cdot \log_{10}(N) + 10 \cdot \log_{10}(PDF)$$

PN1Hz decreases for high charge pump current

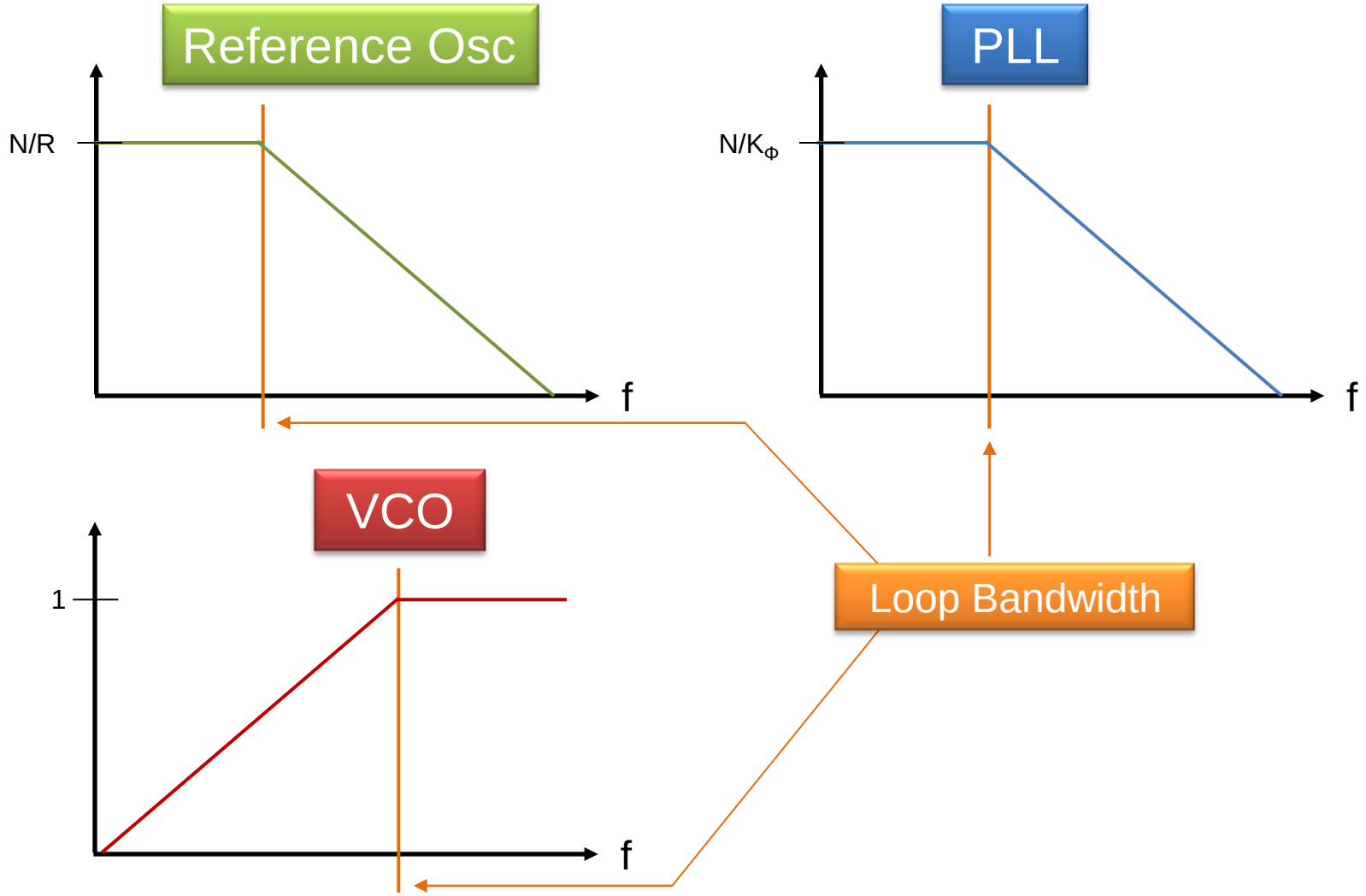
VCO/VCXO Phase Noise Profiles

(Normalized to 1 GHz)

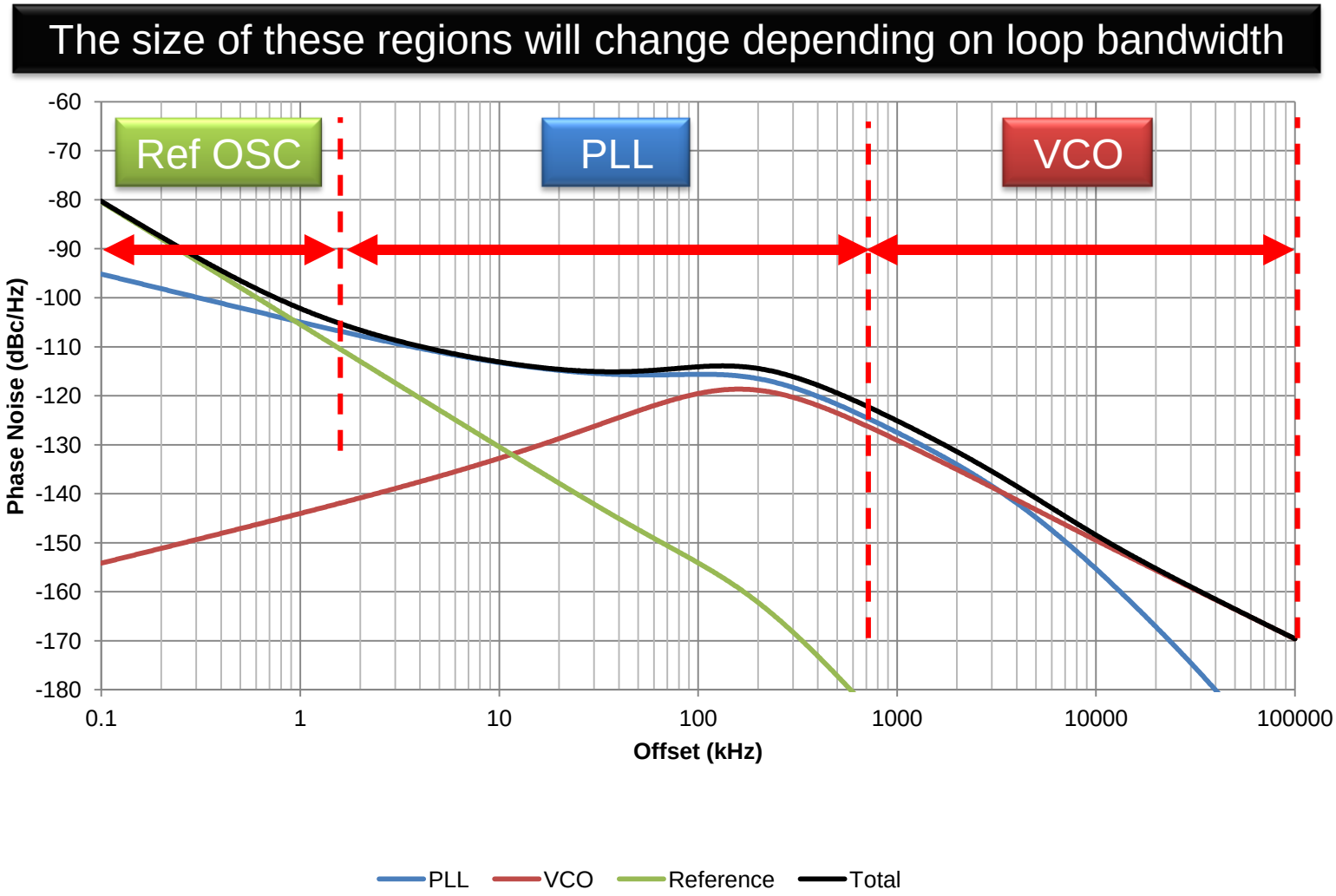
$$L_{NEW} = L_{OLD} + 20*\log_{10}(F_{NEW}/F_{OLD})$$



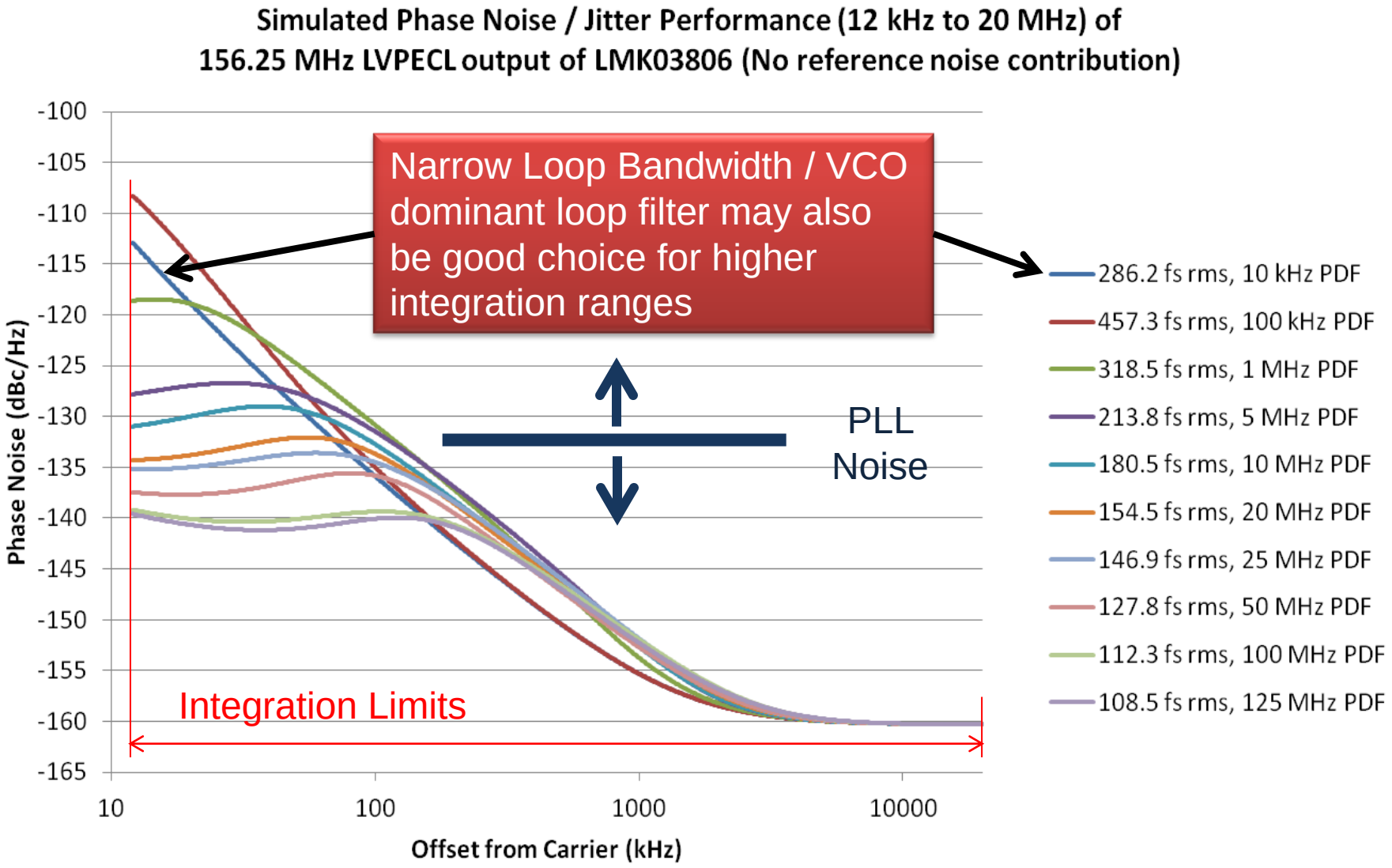
Frequency Responses of Noise Sources to Loop Filter



Sources of Closed Loop Noise



LMK03806 Impact of PDF & N on PLL Noise
(Simulation)



PLL Theory – Take Aways

- Why a use a PLL to set tunable oscillator frequency, like a VCO?
- Feedback is necessary to achieve frequency accuracy from input to output.
- PLL noise performance varies upon configuration…

  - Phase Detector Frequency is of primary significance for PLL noise performance. (Maximize for best performance)
    - Maximum PDF = GCD(F_{REF}, F_{VCO})
      - » 12.288 MHz reference → 2500 MHz VCO results in 32 kHz PDF
      - » 10 MHz reference → 2500 MHz VCO results in 10 MHz PDF (312.5x)

  - Charge Pump Current. (Maximize for best performance)

- VCO/VCXO performance is fixed. If better "VCO" noise is required, pick better VCO or VCXO.

Choosing PLL Loop Bandwidth

- How to chose PLL Loop Bandwidth
- When is a PLL serving as a jitter cleaner?
- What part of the PLL does the jitter cleaning?

Two Different Case Scenarios for Loop Bandwidth

- CASE 1) To optimize jitter between PLL and VCO.
  - Integration bandwidth will include the frequency offset of the loop bandwidth.
  - A PLL/VCO optimized loop filter

- CASE 2) When you want the VCO/VCXO noise to be dominant only.
  - Narrow as possible.
    - When jitter integration bandwidth will not include the loop bandwidth because loop bandwidth is much less than integration bandwidth low limit.
  - Phase Margin of ~50 degrees.
  - A VCO dominant loop filter

Choosing a PLL/VCO Optimized Loop Bandwidth

Starting point for setting the loop bandwidth is the offset at which the open loop VCO phase noise intercepts the open loop PLL phase noise, normalized to the VCO frequency. Keep in mind, the reference noise is included in the PLL noise.

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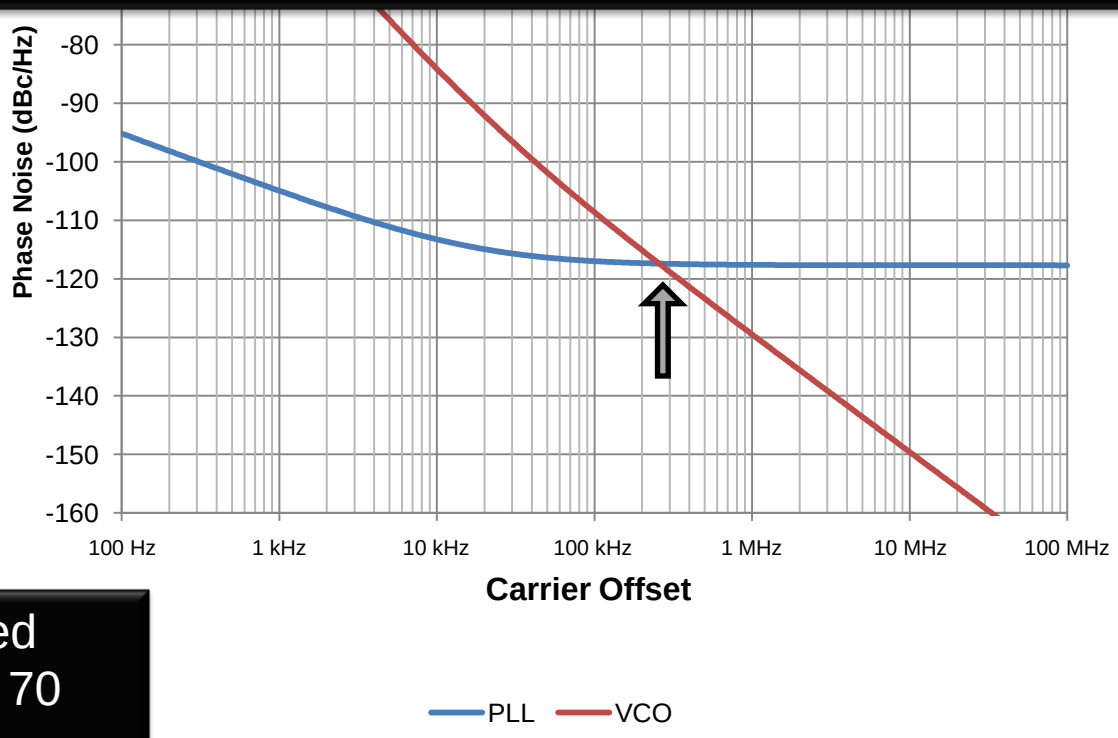
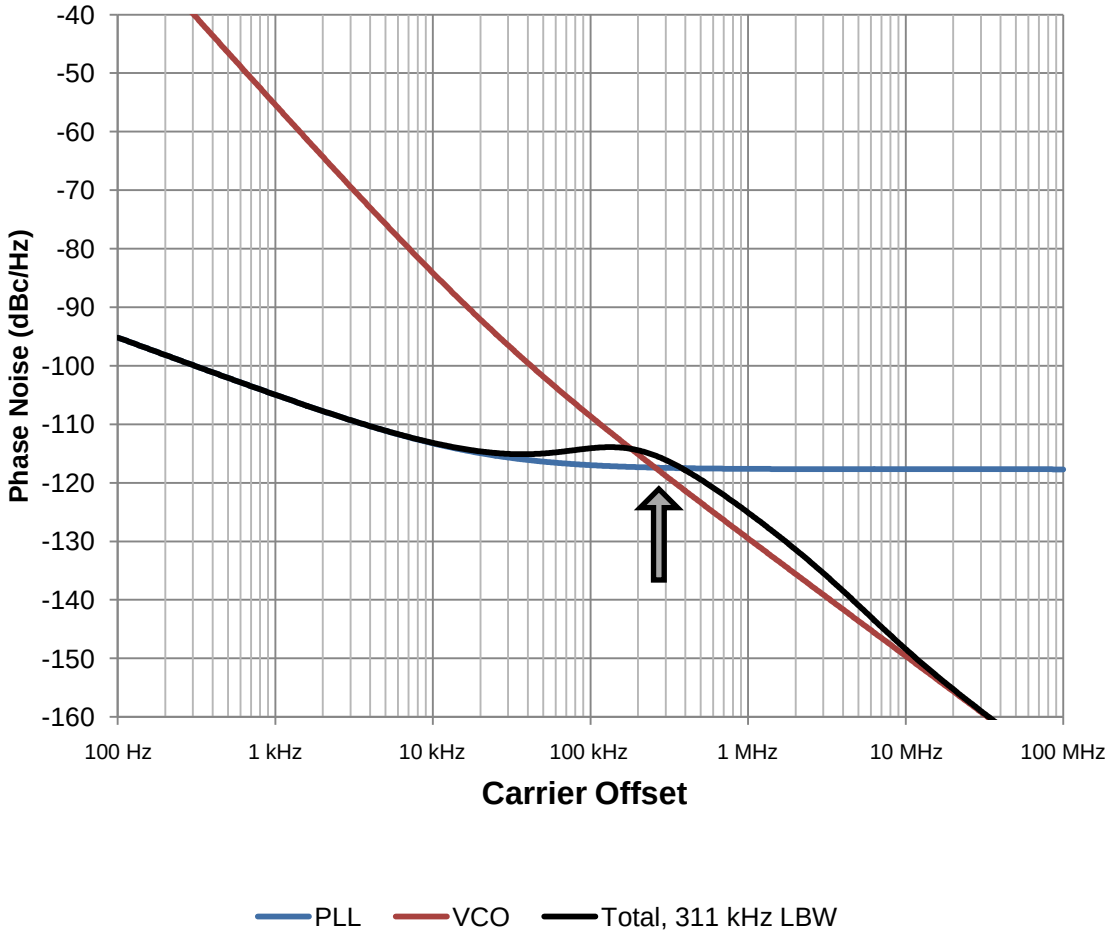


Phase Margin for an optimized PLL/VCO loop filter is typical 70 degrees. Even higher phase margin may slightly improve jitter.

Only PLL & VCO Noise
Integration range includes loop bandwidth

PLL & VCO
Jitter = 107 fs rms
(100 Hz to 100 MHz)

Keep in mind, the reference noise is included in the PLL noise.



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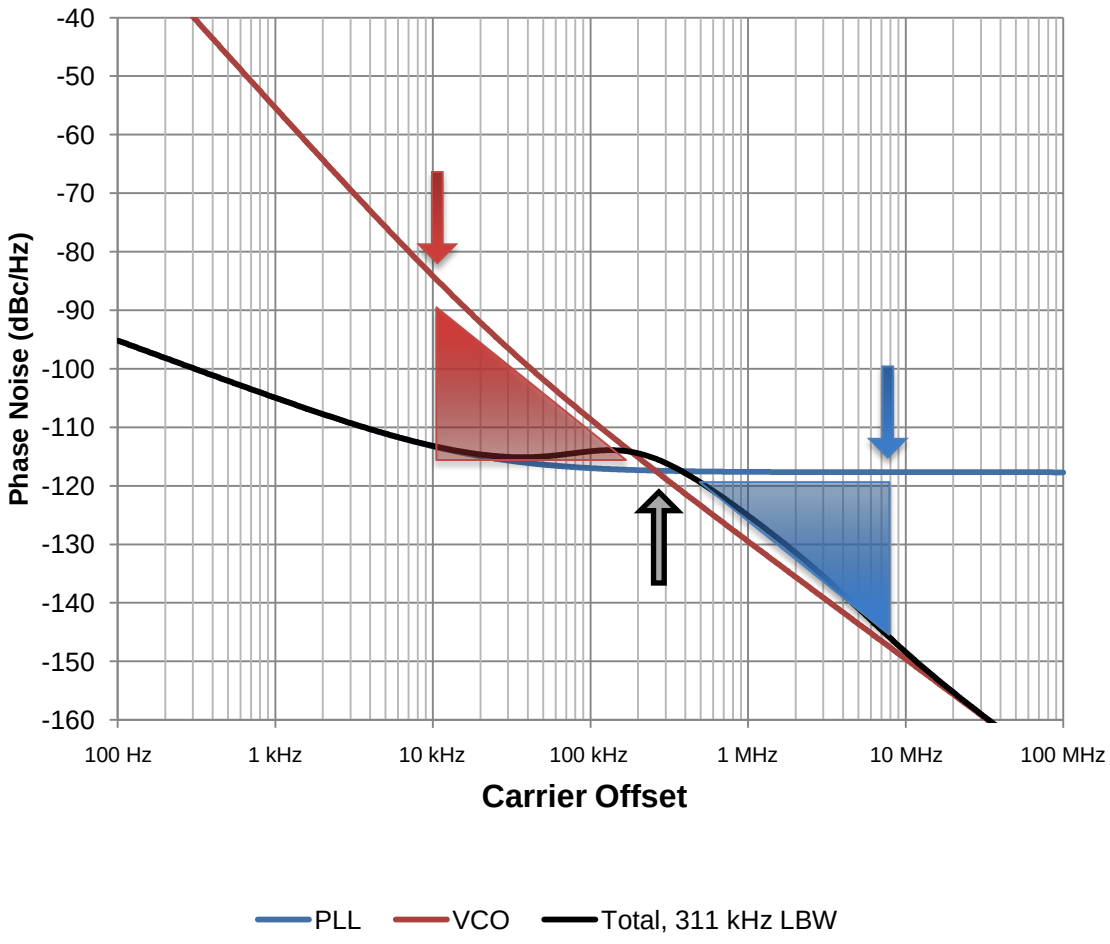
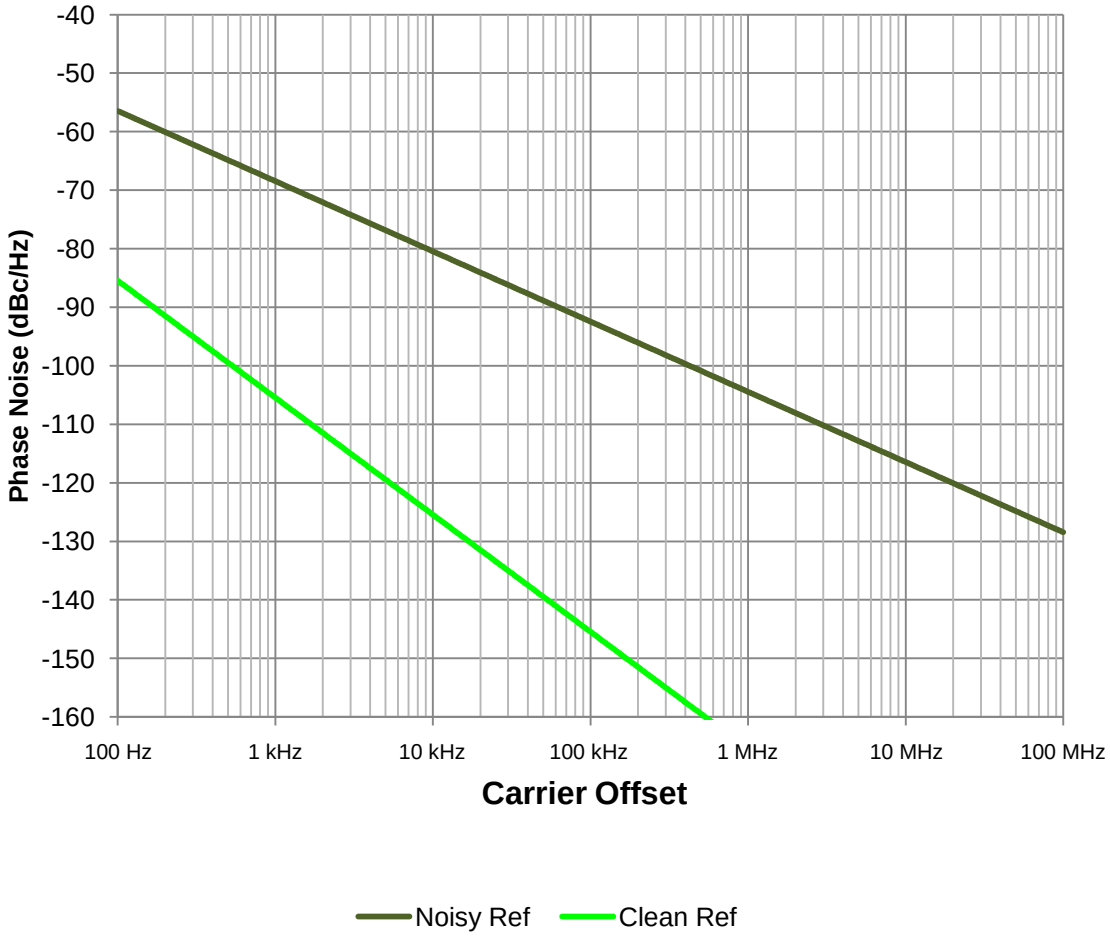


Two References – Noisy or Clean

Noisy Reference
Jitter = 2.4 ps rms
(100 Hz to 100 MHz)

Clean Reference
Jitter = 40 fs rms
(100 Hz to 100 MHz)



References /w PLL & VCO Noise

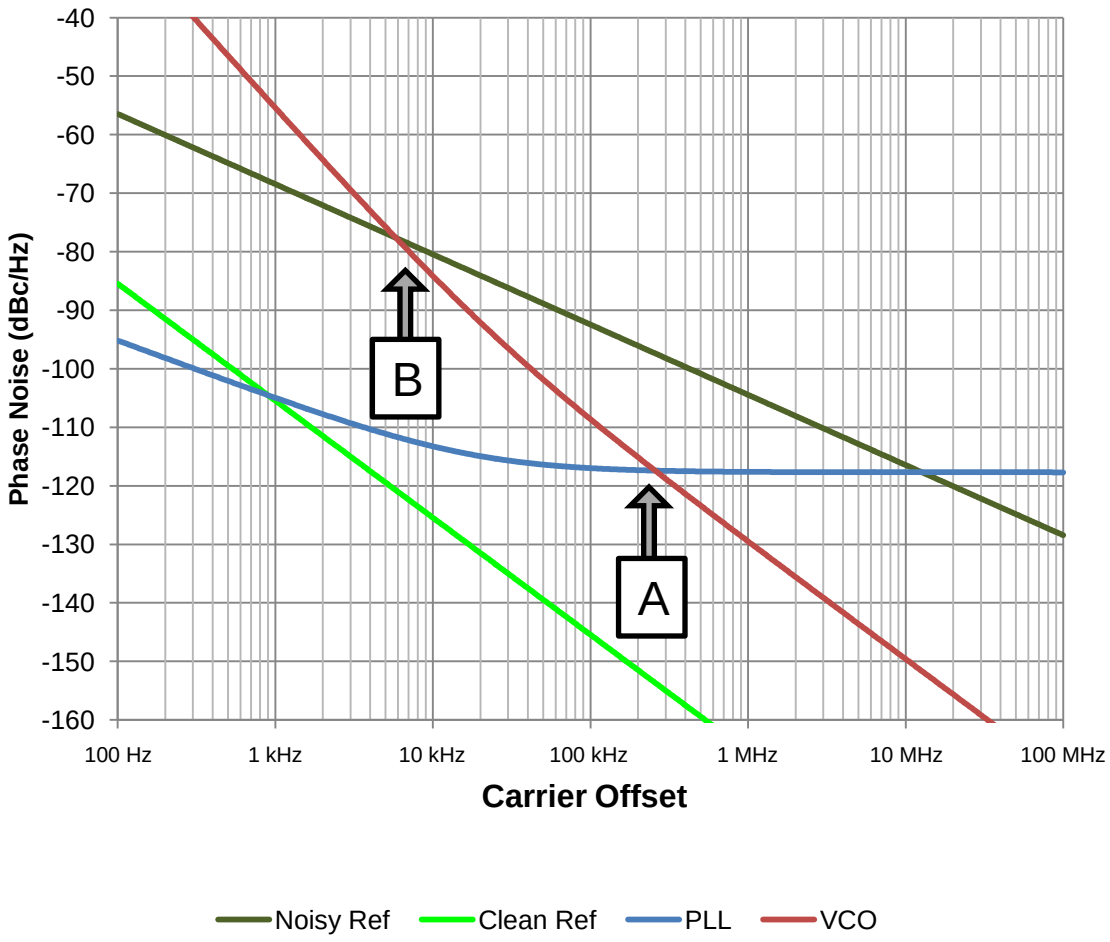
Noisy Reference
Jitter = 2.4 ps rms
(100 Hz to 100 MHz)

Clean Reference
Jitter = 40 fs rms
(100 Hz to 100 MHz)

(A) Total, 311 kHz LBW
Jitter = 115 fs rms
(100 Hz to 100 MHz)

(B) Total, 7 kHz LBW
Jitter = 2.1 ps rms
(100 Hz to 100 MHz)

PLL & VCO
Jitter = 107 fs rms
(100 Hz to 100 MHz)



Clean Reference – No Jitter Cleaning

Clean Reference
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Jitter = 115 fs rms
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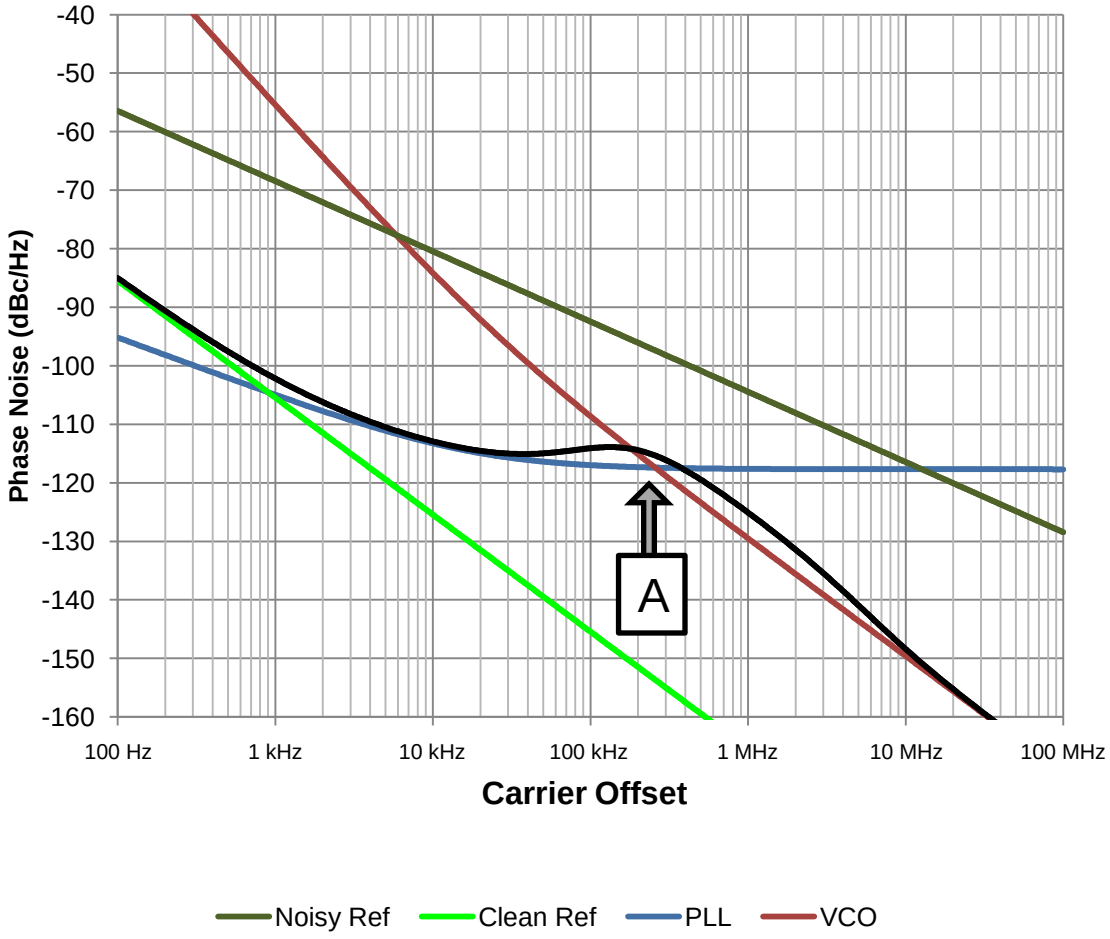
Is any jitter cleaning being performed?



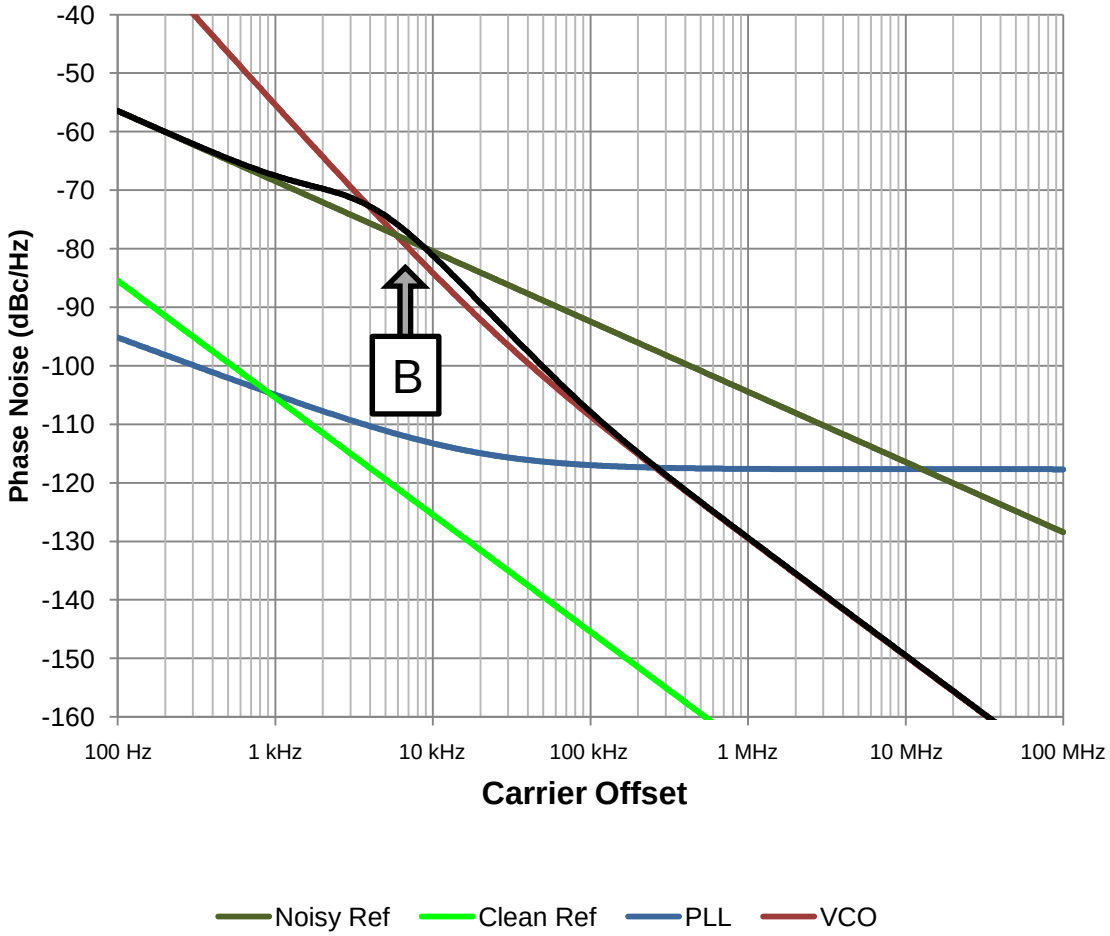
Noisy Reference – Jitter Cleaning

Noisy Reference
Jitter = 2.4 ps rms
(100 Hz to 100 MHz)

(B) Total, 7 kHz LBW
Jitter = 2.1 ps rms
(100 Hz to 100 MHz)

Is any jitter cleaning being performed?

What component is performing the "jitter cleaning?"

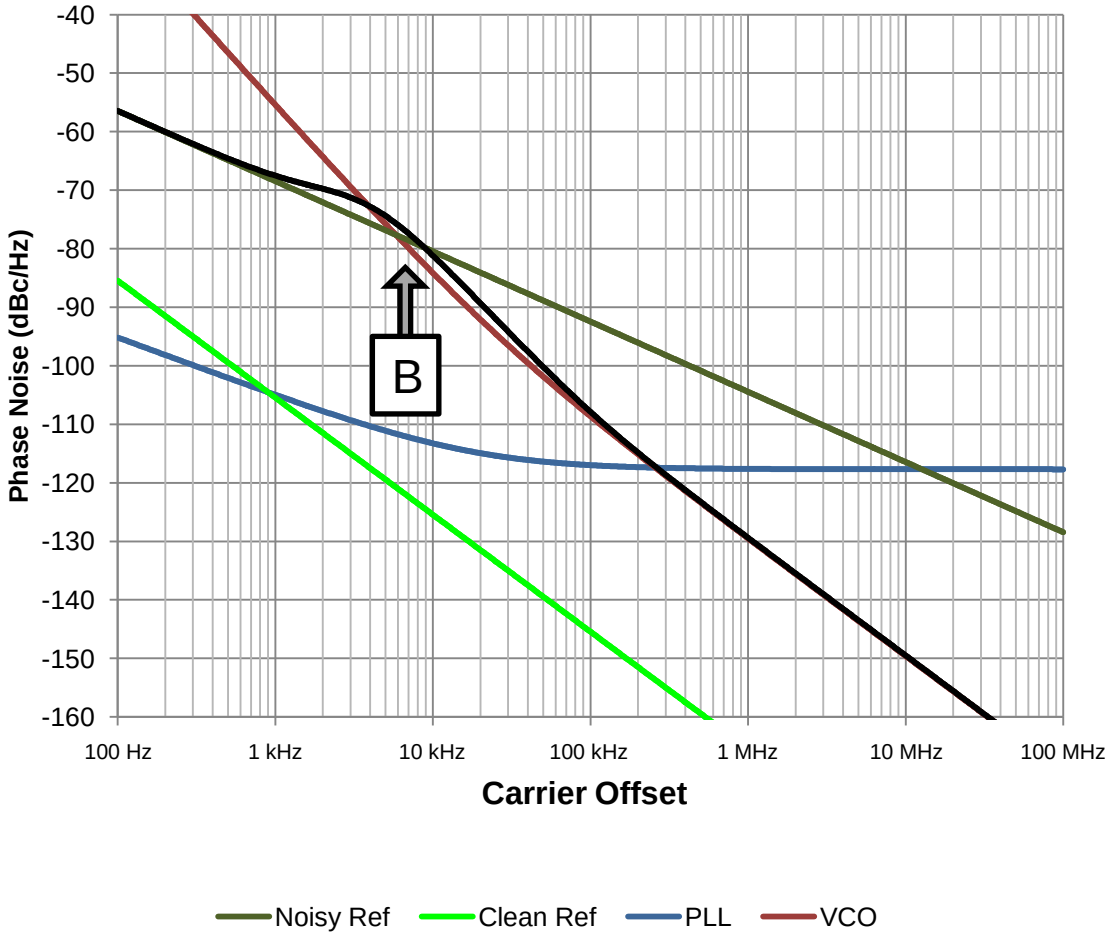


Noisy Reference – Jitter Cleaning

Noisy Reference
Jitter = 2.4 ps rms
(100 Hz to 100 MHz)

(B) Total, 7 kHz LBW
Jitter = 2.1 ps rms
(100 Hz to 100 MHz)

Suppose the clean reference was the performance of a VCXO. What would you design the loop bandwidth to be?



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  - Narrow as possible.
    - When jitter integration bandwidth will not include the loop bandwidth because loop bandwidth is much less than integration bandwidth low limit.
  - Phase Margin of ~50 degrees.
  - A VCO dominant loop filter

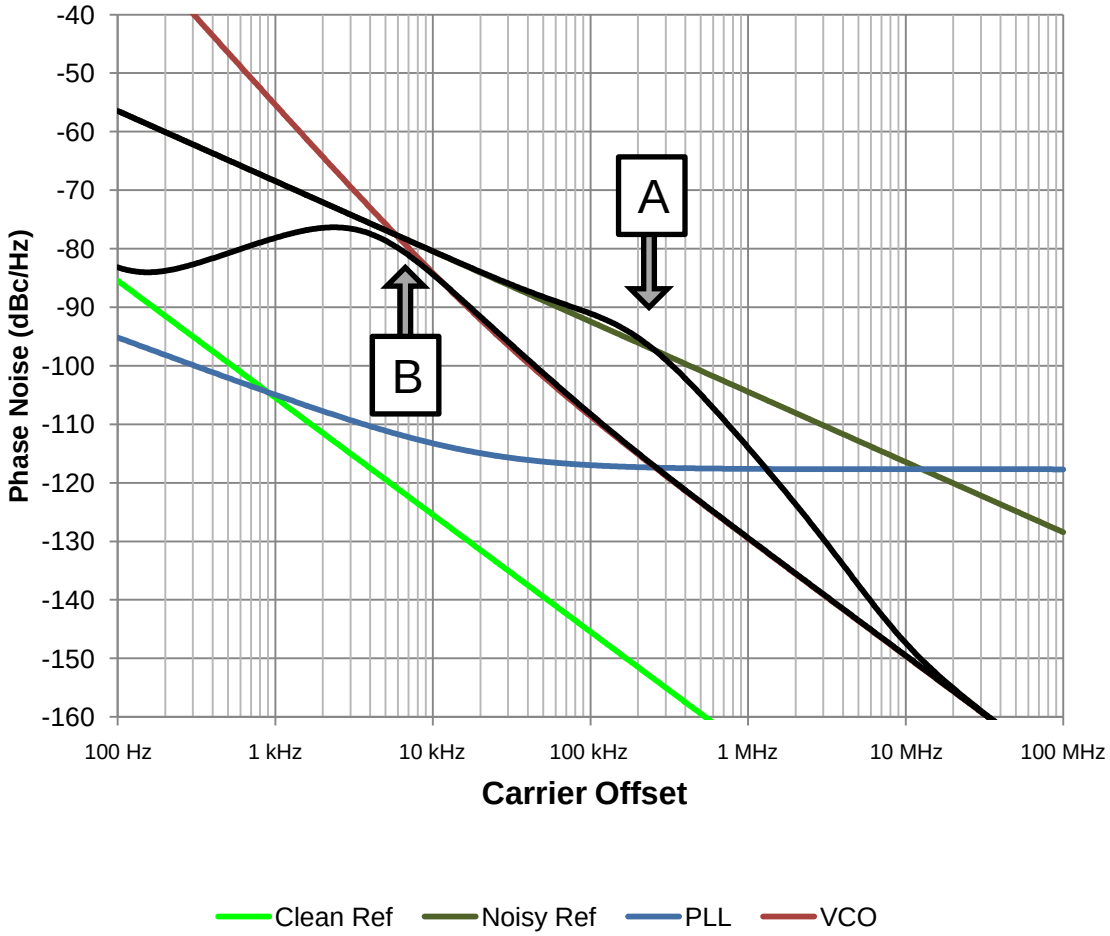
Poor Choices for Loop Bandwidth Result in High Phase Noise Profiles

Noisy Reference
Jitter = 2.4 ps rms
(100 Hz to 100 MHz)

PLL & VCO
Jitter = 107 fs rms
(100 Hz to 100 MHz)

(A) Total, 311 kHz LBW
Jitter = 2.3 ps rms
(100 Hz to 100 MHz)

(B) Total, 7 kHz LBW
Jitter = 919 fs rms
(100 Hz to 100 MHz)



Choosing PLL Loop Bandwidth – Take Aways

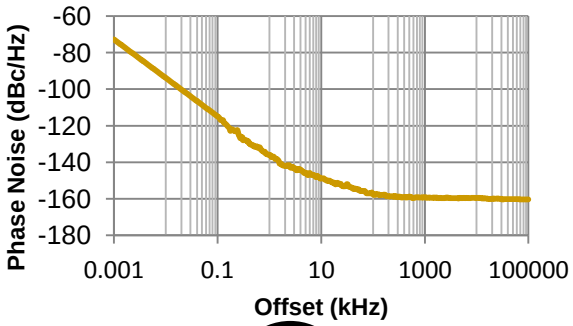
- When jitter integration range includes loop bandwidth, loop filter bandwidth should be 20% greater than PLL & VCO open loop noise crossover point for a PLL/VCO optimized loop filter.
- When jitter integration range is above loop bandwidth, often loop filter bandwidth should be narrow to fully attenuate reference & PLL noise for a VCO dominant loop filter.
- Jitter cleaning is achieved any time the VCO (or VCXO) noise is dominant and below the reference noise.

Dual Loop or Cascaded Loop Architecture

- How does Dual Loop Architecture work?
- When to use a Dual Loop Architecture
- Why not always use a VCXO?

Anatomy of Jitter Cleaning with Cascaded PLLs

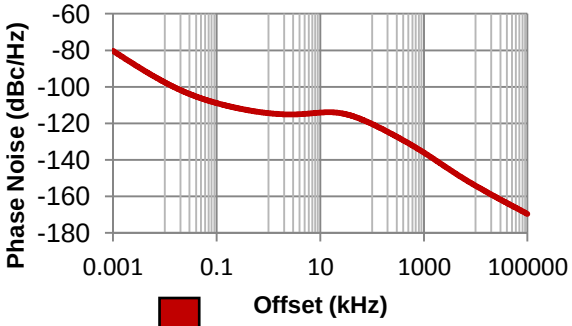
VCXO Phase Noise replaces reference clock phase noise. The VCXO is a low noise reference for PLL2.



122.88 MHz

Ultra-Low noise frequency synthesis/multiplication using PLL2 + VCO.

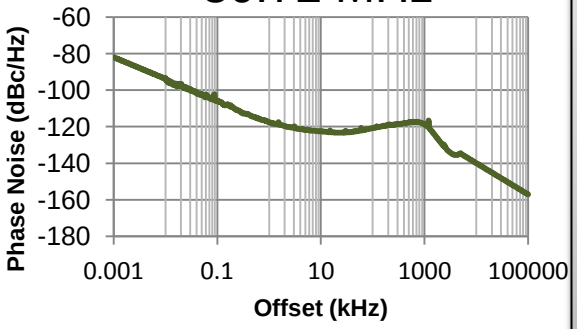
2949.12 MHz

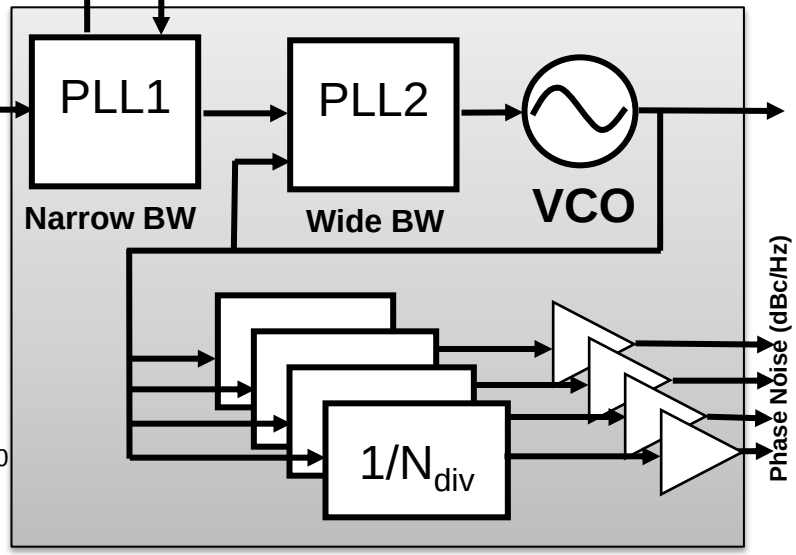


VCXO or Crystal with Varactor

Ref Clock Phase Noise

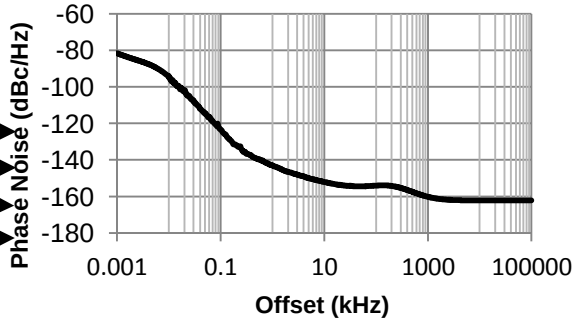
30.72 MHz





CLKout is a cleaned, low jitter replica of the reference clock.

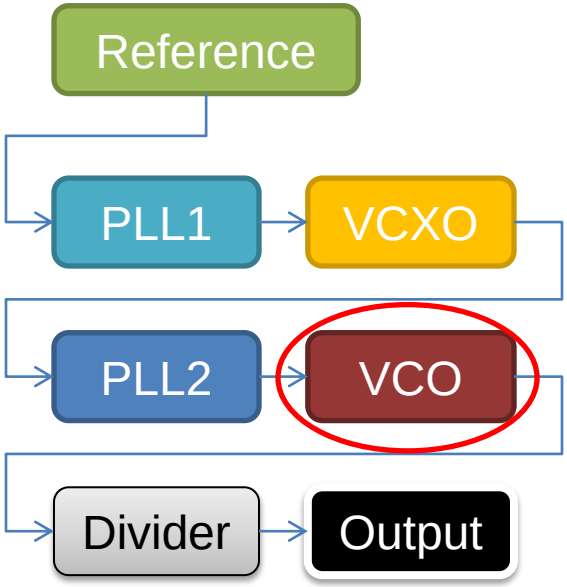
30.72 MHz

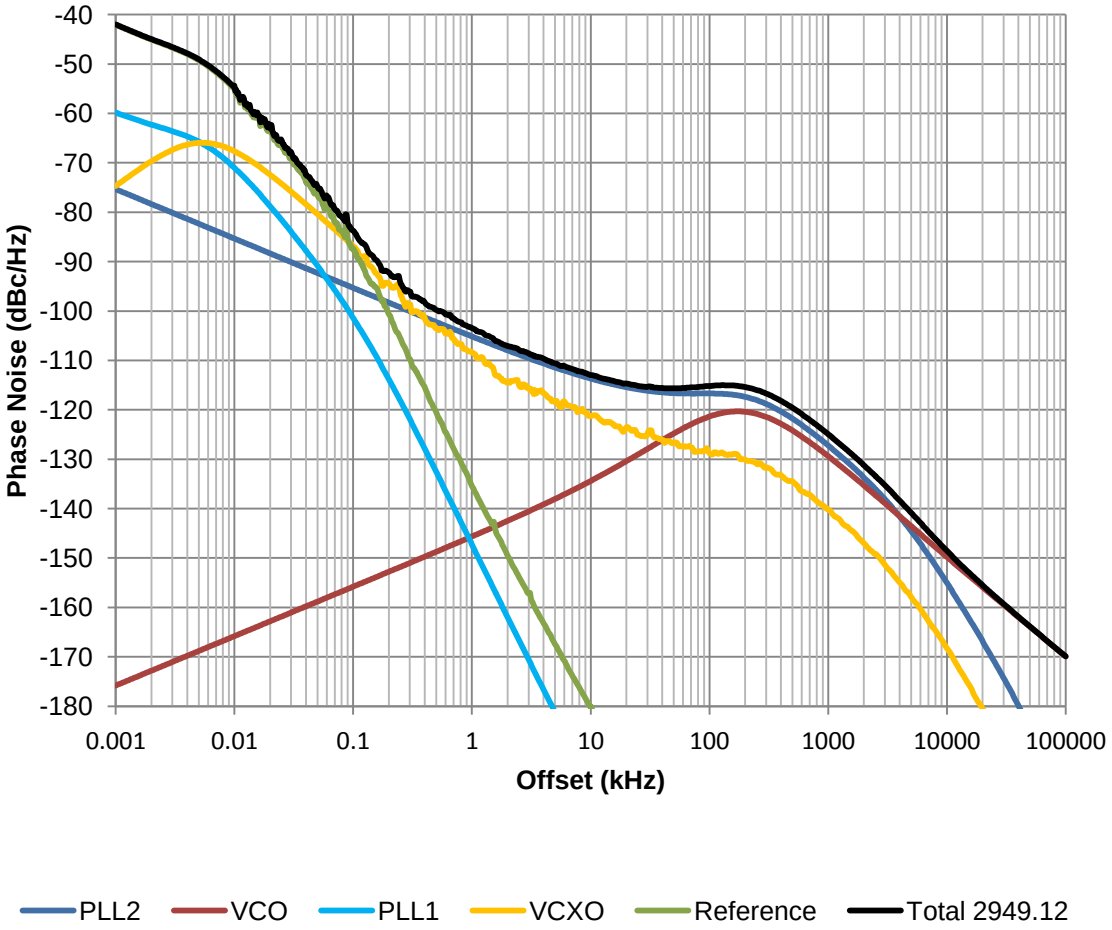


When to use Dual/Cascaded Loop

- When jitter cleaning is required, especially to low frequency offset where VCO does not have good phase noise performance.
  - Recovered clock input
- When input frequency does not relate well with output frequency, and good performance is required at lower offsets where VCO does not have good phase noise performance.
    - » 12.288 MHz reference → 2500 MHz VCO results in 32 kHz PDF
    - » 10 MHz reference → 2500 MHz VCO results in 10 MHz PDF (312.5x) When input frequency is low, and higher phase detector frequency will benefit PLL operation
  - Input of 12.288 MHz vs. input of 122.88 MHz.

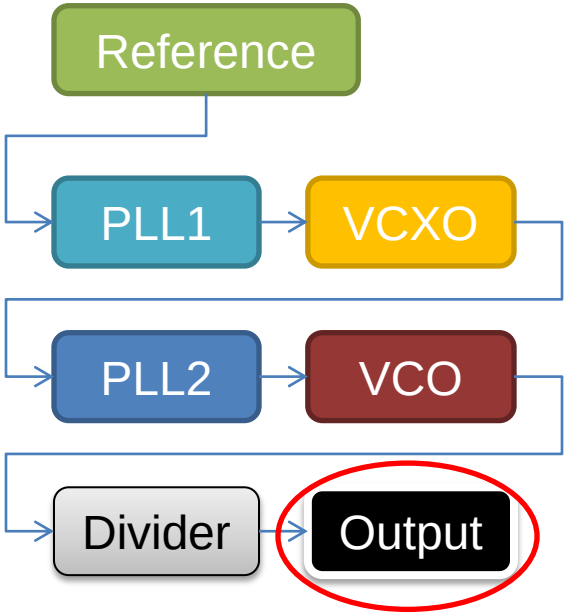
Dual Loop Phase Noise at VCO
(2949.12 MHz)

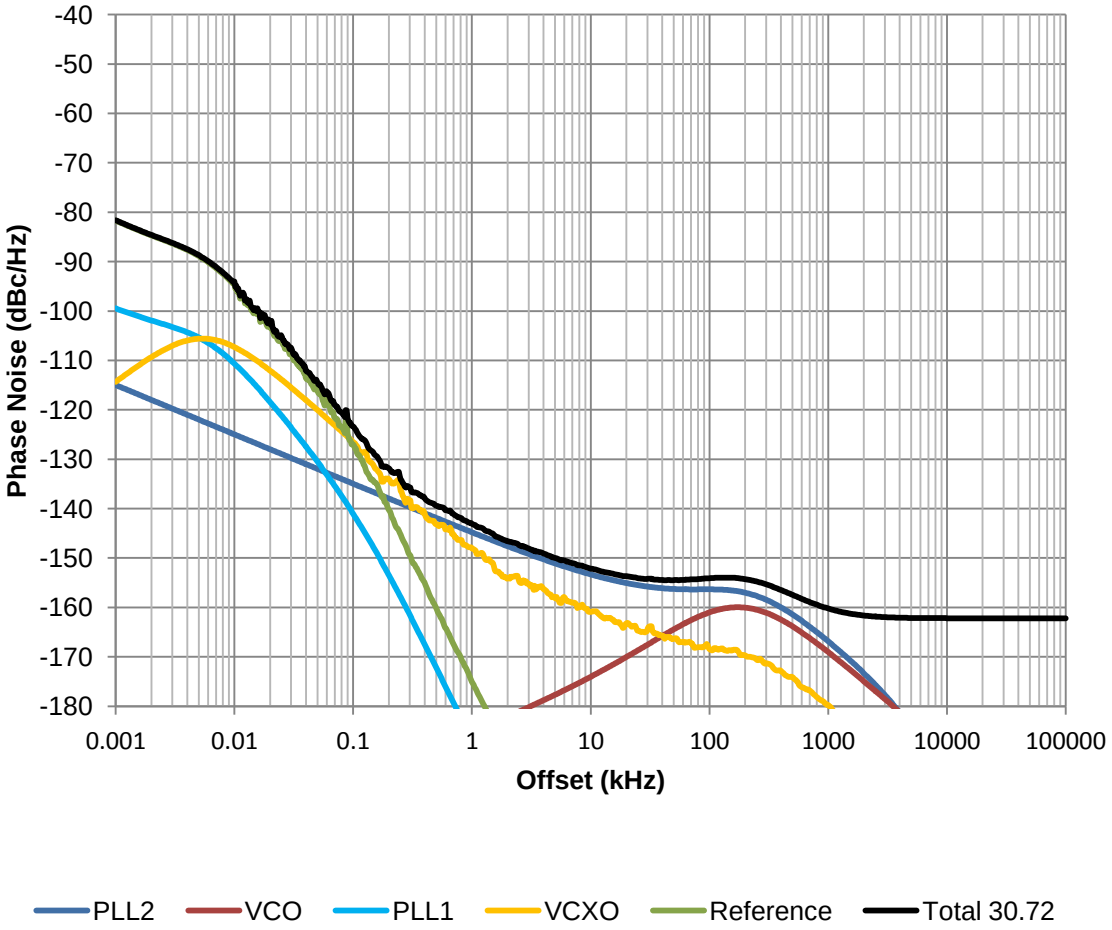




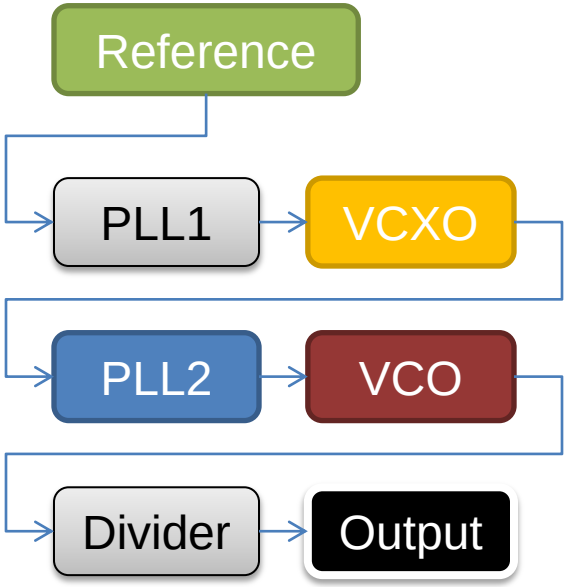
Dual Loop Phase Noise at Output
(30.72 MHz)

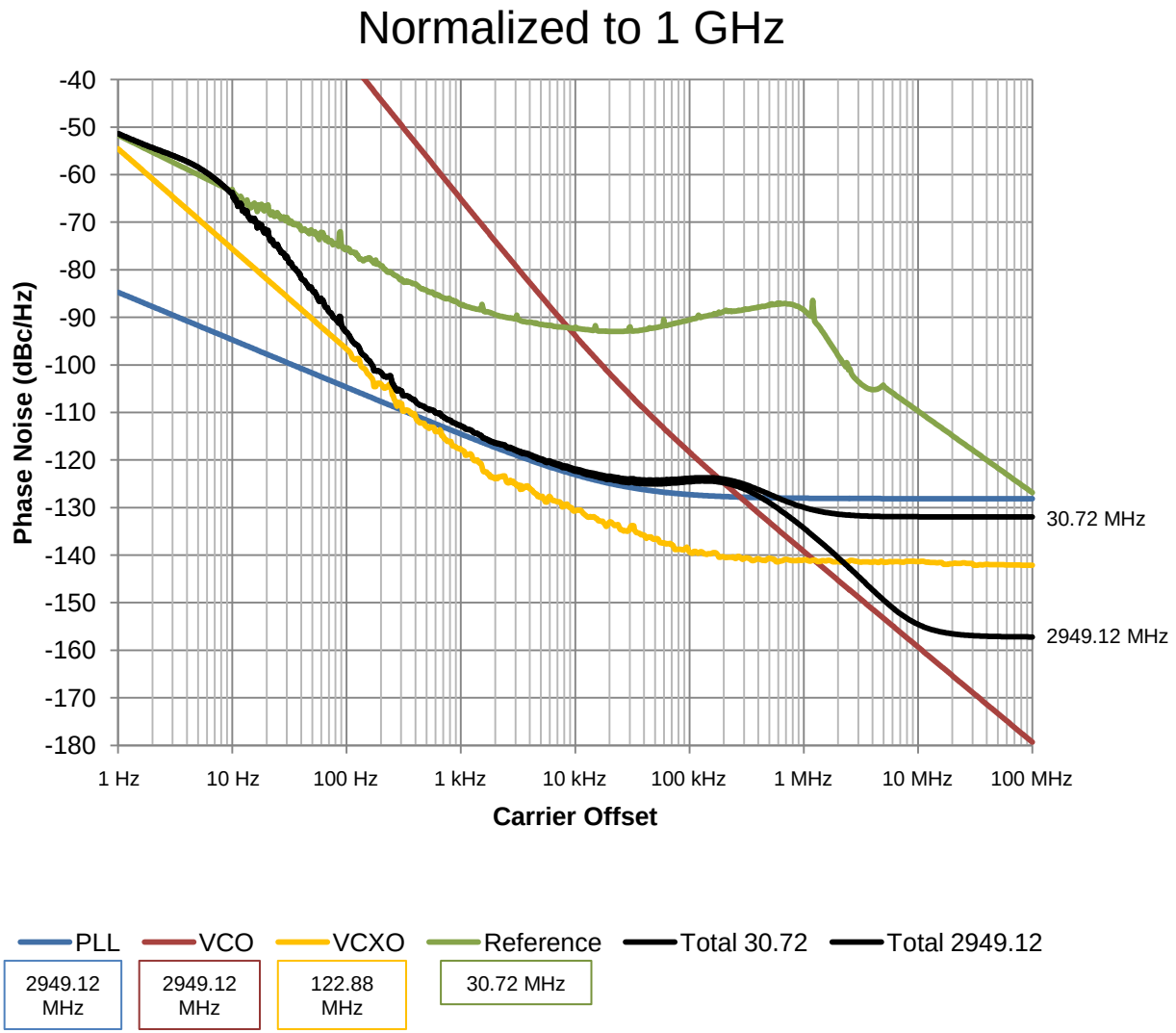
$$L_{NEW} = L_{OLD} + 20*\log_{10}(F_{NEW}/F_{OLD})$$



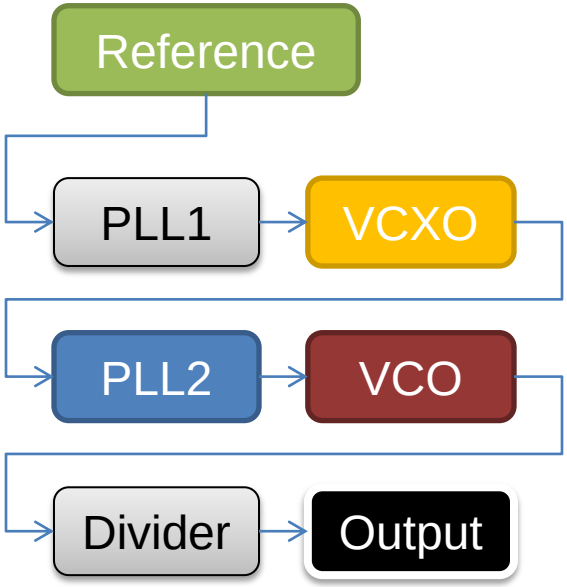


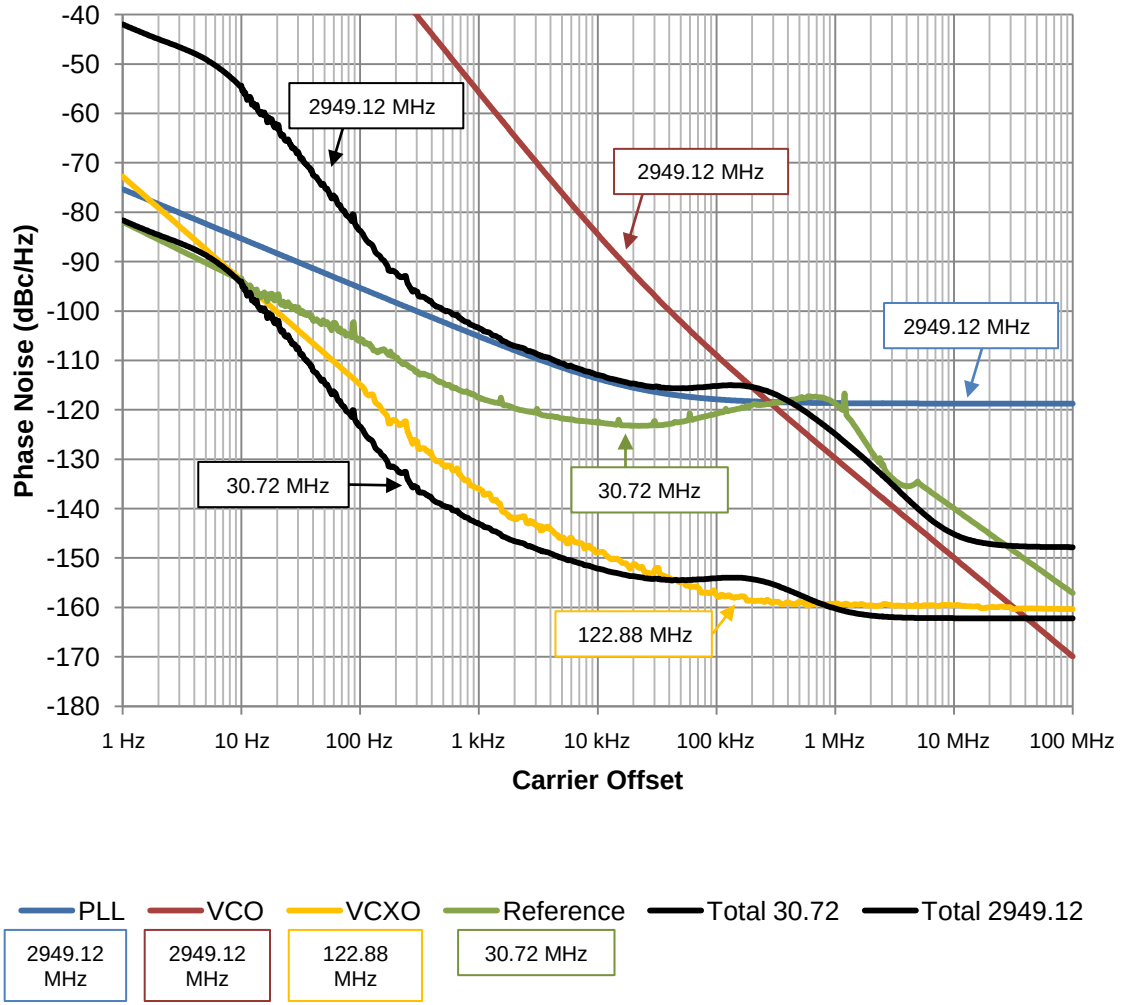
Open Loop Phase Noise of All Clock Elements… Normalized to 1 GHz





Open Loop Phase Noise of All Clock Elements… at specified frequency





Dual Loop Jitter Cleaning Summary

(with Single Loop Comparison)

	Block	100 Hz to 20 MHz	12 kHz to 20 MHz
	Recovered Clock Measured at Input 30.72 MHz	**11,200 fs rms**	**11,200 fs rms**
	VCXO, Open Loop 122.88 MHz	90 fs	85 fs rms
	VCO, Open Loop 2949.12 MHz	27,500 fs rms	318 fs rms
	PLL2, Open Loop 2949.12 MHz	397 fs rms	396 fs rms
Dual Loop	At VCO, Closed Loop 2949.12 MHz	110 fs rms	99 fs rms
Dual Loop	At CLKout, Closed Loop 30.72 MHz	**277 fs rms**	**273 fs rms**
	At CLKout, Closed Loop 30.72 MHz **Single Loop Cleaning**	**1,200 fs rms**	**651 fs rms**

Dual Loop or Cascaded Loop Architecture – Take Aways

- Use for…
  - Jitter cleaning to low offsets with noisy reference inputs,
  - When input and output frequency have poor integer relationship.
  - With low frequency inputs to improve PLL performance.
- First PLL should have a narrow loop bandwidth. Clock design tool may design too wide. Manually re-design narrower or enter a noisy reference.
- Second PLL should have a wide loop bandwidth to take advantage of cleaned (by VCXO/crystal) reference.

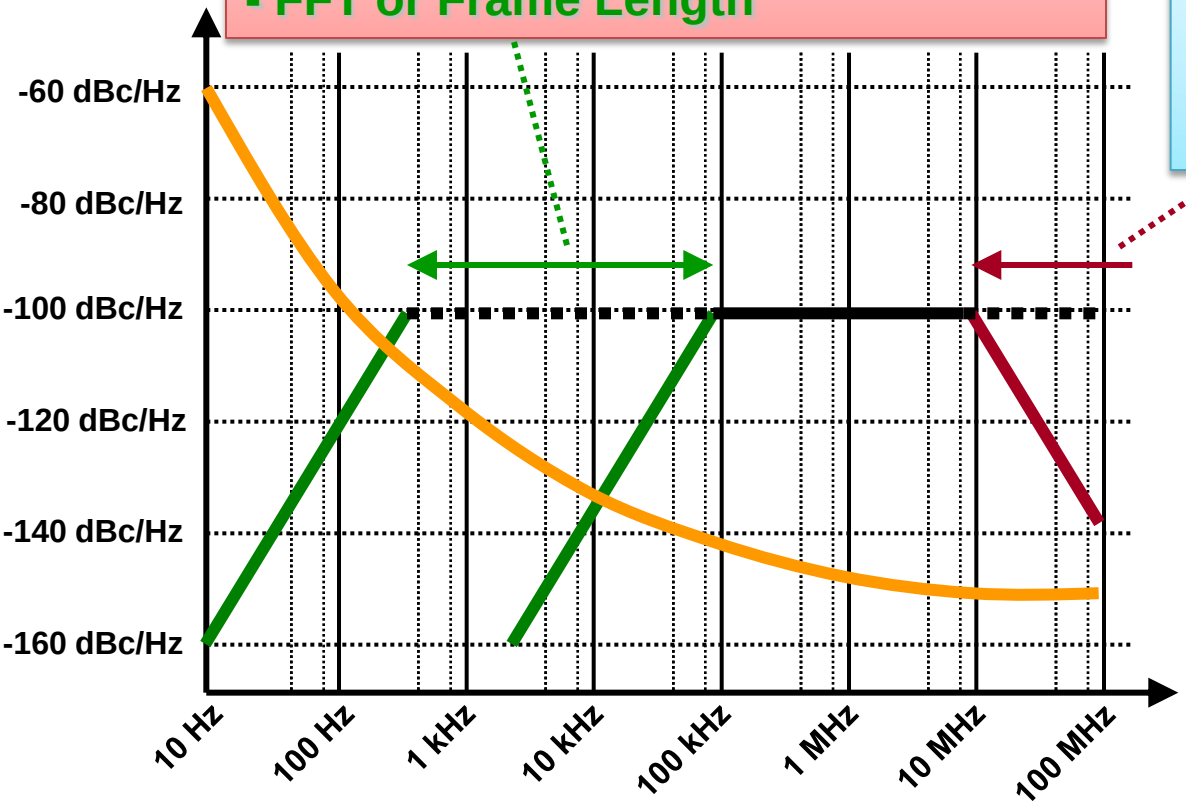
Determining Integration Range for Jitter Based on Customer Requirements

- Understanding the system
- Understanding the specification

Jitter Integration Bandwidth
Determining Factors

Low End of Integration:
- Carrier or Clock Recovery loop BW
- Multi-Path or Doppler
- FFT or Frame Length

High End of Integration:
- ADC sampling rate
- Channel Bandwidth
- $-1/T_{bit}$



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Common Integration Bandwidths

Specification	Low Limit	High Limit	Clock Freq (MHz)	Target Clock RMS Jitter
40 GbE/100 GbE 802.3ba-2008 (Am. 4)	40 kHz	200 MHz	644.53125	193 fs rms
10 GbE (802.3-2008 Sec 4)	1.875 MHz	20 MHz	156.25, 312.5	796 fs rms
1 GbE (802.3-2008 Sec 3)	637 kHz	12.5 MHz	125	1365 fs rms
FibreChannel 16 GFC	637 kHz	10 MHz	106.25, 212.5	228 fs rms
SAS Gen 1-3 (SAS-2 Rev 16)	900 kHz	7.5 MHz	37.5, 75, 120, 150	296 fs rms
PCIe Gen1 (2.5 Gbps)	1.5 MHz	22 MHz	100	711 fs rms
PCIe Gen3 (8 Gbps)	2 MHz	10 MHz	100	163 fs rms
SMPTE				

Determining Integration Range for Jitter Based on Customer Requirements – Take Aways

- Need to know something about the customers application.
- When the customer's application is a standard. Often the standard is specified for the serialized bit stream. Not the clock since the clock is only one contributor of jitter among many blocks.
  - Allows for design trade-offs.

Loop Bandwidth and PLL Lock Time

Analog Lock Time

Monolithic VCO, Digital Calibration Time

Lock time

- For Fixed Frequency Applications Lock time is typically of no real concern.
- PLL Synthesizer Applications:
  - Governed by loop bandwidth
    - Traditional Analog Lock time ~= 4 / LBW
    - Digital Calibration changes this.

LMX2541 Digital Lock Time

- Lock time = 30 µs
  - + 3800 / **CLK**
  - + 0.1 µs/MHz * 10 MHz
  - + 2 µs * (10 MHz / **CLK**)
  - Assume ΔF = 10 MHz

- OSCin = 63 MHz: CLK = 31.5 MHz
  - Lock time = 153 µs
- OSCin = 64 MHz: CLK = 16.0 MHz
  - Lock time = 270 µs

3.10 INTERNAL VCO DIGITAL CALIBRATION TIME

When the LMX2541 is used in full chip mode, the integrated VCO can impact the lock time of the system. This digital calibration chooses the closest VCO frequency band, which typically gets the device within a frequency error 10 MHz or less of the final settling frequency, although this final frequency error can change slightly between the different options of the LMX2541. Once this digital calibration is finished, this remaining frequency error must settle out, and this remaining lock time is dictated by the loop bandwidth.

Based on measured data, this digital calibration time can be approximated by the following formula:

$$LockTime = A + B/CLK + C \cdot \Delta F + D \cdot (\Delta F/CLK)$$

Symbo1	Value	Units
Locktime	Varies	µs
A	30	µs
B	3800	None
C	0.1	us/MHz
D	2	µs
ΔF	Varies	MHz
CLK	f_{OSCIn} / 2 for 0 ≤ OSC_FREQ ≤ 63 f_{OSCIn} / 4 for 64 ≤ OSC_FREQ ≤ 127 f_{OSCIn} / 8 for 128 ≤ OSC_FREQ	None

Loop Bandwidth and Lock time – Take Aways

- For traditional analog VCO, lock time ~= 4 / LBW
- For monolithic VCO, lock time is also a function of digital calibration

Appendix

For Further Reference

- Clock Design Tool
  - http://www.ti.com/tool/clockdesigntool
    - See Training Videos on this page.
  - **Clock Architect Coming**
- Dean's PLL Book
  - www.ti.com/tool/pll_book
- Jitter Cleaning with LMK03000
  - http://www.ti.com/lit/an/snoa508a/snoa508a.pdf
- VCXO Performance with LMK04000
  - http://www.ti.com/litv/pdf/snaa063
- Please search Clocks & Timers forum for "**Training – Choosing Loop BW for PLLs**" for most recent copy of this presentation.

END

Subhead text here